EE 344: Electronics Design Lab

OpenBCI based EEG Acquisition System

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Introduction

EEG is a non-invasive method of capturing brain signals. The device consists of two parts: recording electrodes and data-capturing electronics. The electrodes are placed on the subject's head to record different spatial locations on the brain. Each electrode corresponds to a single of data. For example, the OpenBCI Cyton board provides access to 8 channels of data. The Daisy expansion board offers support for an additional eight channels. The goal is to scale the existing design to accommodate 24 channels for better spatial resolution. The design will be robust to ambient noise (including the 50 Hz power supply interference) and has the potential to be used for a wide variety of applications, including medical diagnosis and brain-computer interfacing. The deliverables of the project will include the following,

1. A custom-designed PCB: The PCB will support 24 EEG channels, provide a Wi-Fi module for communicating with a laptop/computer/phone for real-time streaming, a micro-SD card for local storage, and accelerometer support for removing noise due to head motion
2. An EEG headset with electrodes placed at spatial locations recommended by the 10-20 international standard
3. A laptop/phone application to view the data in real-time

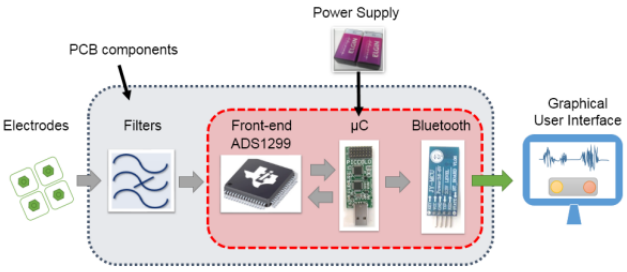


Figure 1: Existing OpenBCI design

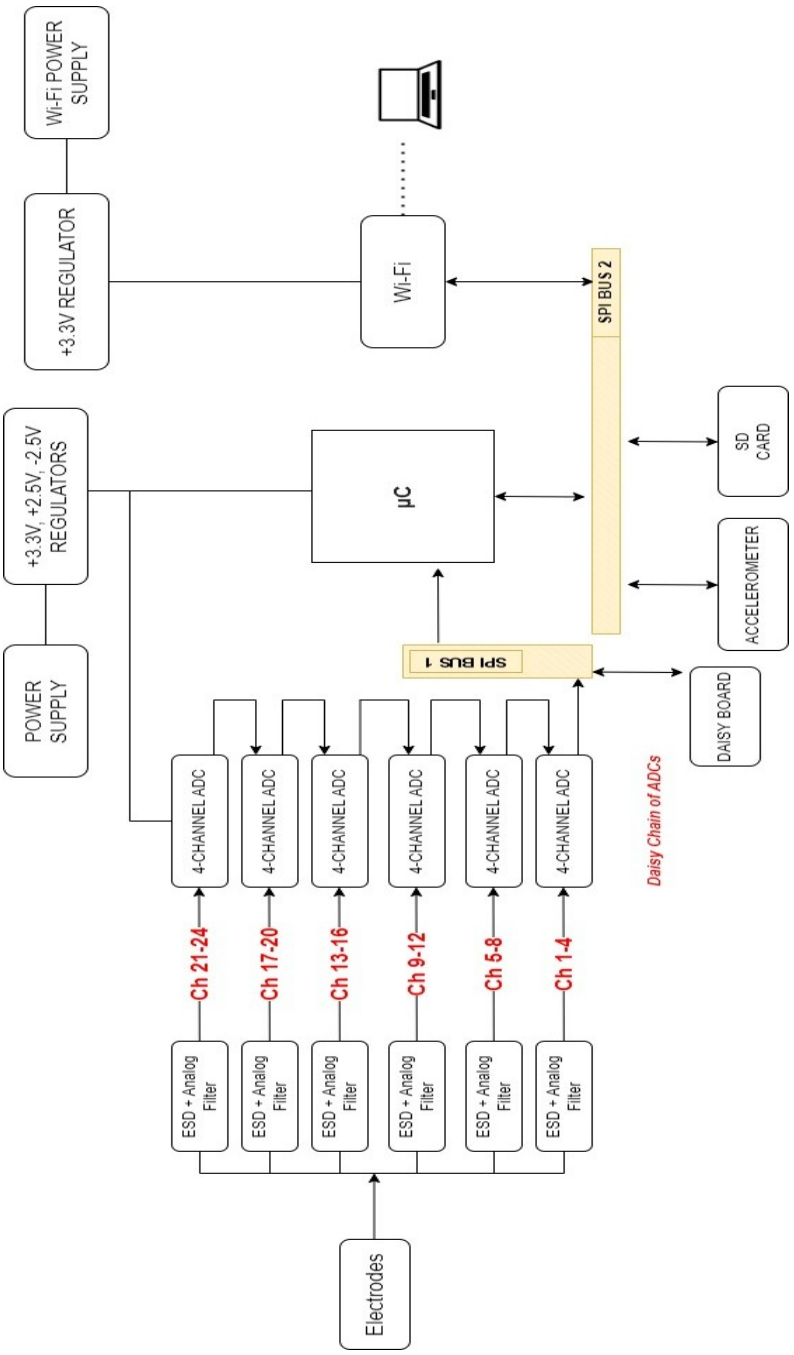


Figure 2: Design Block Diagram

Design Description

The OpenBCI Cyton Board is an 8-channel biosensing board. The existing setup takes in 8 analog inputs from the electrodes and passes them through an 8-channel A/D Converter. The digital output is sent to the microcontroller after which it is passed onto an RFduino Bluetooth Transmitter which transmits the data to a nearby device for viewing.

While scaling up the existing design to meet our requirements, there are multiple factors that we have taken into consideration. Firstly, our targeted 24-channel design would require 6 A/D converters to process the data provided by the electrodes. These devices will peripherally interface with the microcontroller, and therefore, our choice of the microcontroller will have to reflect this additional interfacing. Lastly, limitations on data rate across Bluetooth would impair the performance of our device, especially considering the larger amount of data our module targets to transmit as compared to the original design. To this end, we will look to transmit our data over Wi-Fi for better performance.

A high-level overview of our design is depicted in Figure 2. The subsections that follow give a brief overview of the role and functionality of each module and mention any changes from the existing design that we look to implement.

Electrodes

The EEG electrodes form the analog front end of the EEG processing pipeline and are of different types, including active, passive, dry, and sponge. We will be using the dry spikey and flat electrodes as these have very little preparation time. The electrodes will be mounted on a custom 3D-printed headset, adhering to the 10-20 international standard for electrode placement.

Due to an increased electrode count, specific brain regions can be targeted to study functions like motor function, sensation, and memory. We will specifically target the frontal lobe's motor and visual cortex.

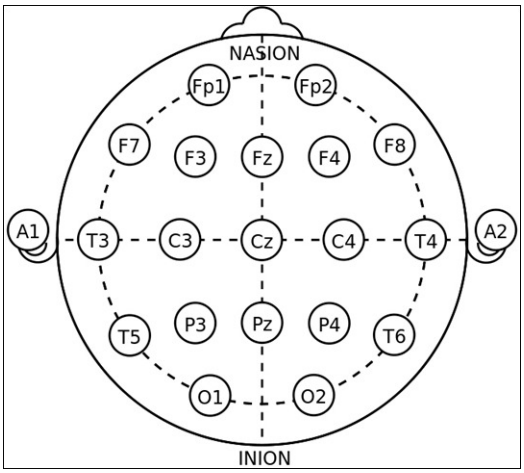


Figure 3: Electrode locations for EEG recording

A/D Converters

The A/D converters are a vital part of the analog front end. In particular, we will use the ADS1194, a low-power, 4-channel, 16-bit analog-to-digital converter for biopotential measurements. One of the major requirements for the A/D converter was the inclusion of amplifiers as the EEG signals are of the order of $10\mu V - 100\mu V$, so we have chosen the ADS1194 which has in-built programmable gain amplifiers.

After being passed through an ESD protection unit, electrode signals from 4 EEG channels are fed into the A/D converter that consists of four simultaneous samplings followed by delta-sigma ($\Delta\Sigma$) converters.

Since the design requires 24 electrodes, 6 A/D converter chips will be on the final PCB. The A/D converters will be connected in the Daisy-chain configuration to ensure synchronisation between them. The output of all the converters is multiplexed into a single stream sent to the microcontroller over a serial interconnect (SPI). The data output sent on the `DOUT` pin consists of 24 control bits followed by 24 sets of 16-bit quantized EEG data.

Microcontroller

The microcontroller at the heart of the system is responsible for gathering data from the A/D Converters and the accelerometer, processing it and passing the final values to the Wi-Fi and SD Card modules for transmission and storage, respectively. The original design for the Cyton board uses a 28-pin PIC32MX250F128B micro-controller, which comes with two I^2S/SPI modules

for codec and serial communication, up to 13 channel 10-bit A/D Converters, and up to 19 I/O pins. Since the microcontroller will now be interfacing with 6 A/D Converters, the SD Card reader, and the Wi-Fi Module, we will be using the PC32MX250F128D micro-controller, which has a larger number of I/O pins (31), which can be reconfigured as chip select lines for the additional A/D Converters.

The microcontroller will be programmed using a chipKIT UDB32-MX2-DIP bootloader, with code written in the Arduino software library.

Power Supply

The components require a Digital Supply Voltage (`DVDD`) of $+3.3V$, an Analog Supply Voltage (`AVDD`) of $+2.5V$ and an Analog Ground Voltage (`AVSS`) of $-2.5V$. AP2112K-3.3TRG1 is a fixed LDO Voltage Regulator used to generate the `DVDD` signal using the input `RAW` signal. This `DVDD` signal is fed into the LM2664 Switched Capacitor Voltage Converter, which generates the `-RAW` signal. This `-RAW` signal is further passed through the TPS72325 Negative-output Linear Regulator to generate the `AVSS` signal. The `AVDD` signal is generated by passing the `DVDD` signal through the AP2112K-2.5TRG1 Voltage Regulator.

Since the Wi-Fi has high current requirements for the Digital supply regulator, we will be using a separate Voltage Regulator (AP2112K-3.3TRG1) to generate the `DVDD` signal using the input `RAW` signal coming from another battery.

The main consideration while choosing the regulators was the required output voltage and the current rating. The Wi-Fi module requires a large amount of current while transmitting data, so we choose the $600mA$-rated AP2112K-3.3TRG1.
We will use two 3-6V DC Batteries, one as the power source for the board and another for the Wi-Fi.

Accelerometer

The LIS3DHHTR is a three-axis accelerometer with digital I^2C/SPI serial interface standard output, capable of 16-bit data output. The purpose of the accelerometer is to remove artifacts in the EEG signal due to head movements. The data returned by the accelerometer is a good baseline to reconstruct what happened in the user's recording session.

The accelerometer can also be used as a marker for different phases of experimentation. Without the accelerometer, one would have to reset the data logging software. With the accelerometer, one can simply tap the board a few times

and the created artifact would be easy to observe in the accelerometer's data stream.

SD Card

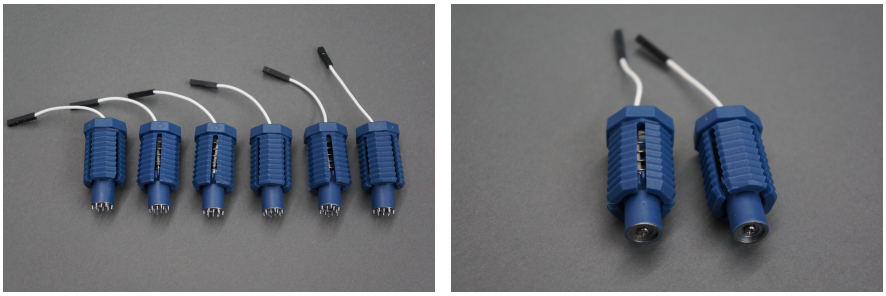
SD card is a necessary provision for logging data to local storage. This is useful in sleep study applications or when it is difficult to make wired connections to the PC. We will be using a Suntech ST-TF-003A SD card holder for the design. The data saved to the SD card is sampled at 250 Hz. This amounts to 3 MB of data per minute and hence, a high-speed SD card with large storage will be used (8 GB, 16 GB, or 32 GB). Data from the A/D converter will be sent to the SD card over an SPI bus.

Wi-Fi Module

Unlike the original design, a BLE module will not be included because of the requirement for frequent firmware updates. Another disadvantage of BLE is that the hardware must support the BLE protocol, which requires data packetization. On the other hand, Wi-Fi is based on a stream protocol which is easier to implement. OpenBCI provides a Wi-Fi shield in addition to the Cyton board, which has been known to suffer from packet losses and cyclical noise. We aim to overcome these defects by providing a reliable data transfer interface using an ESP-12S: ESP8266 Wi-Fi Module, which is Arduino compatible.

Headwear

The Ultracortex Mark IV is a device developed by the OpenBCI company, which allows users to measure and record brain activity (EEG). The following are the main components of the headset: Cables, Spikey units, Flat units, Comfort units, and Ear Clips. Unlike the original design, we have to use 8 more spikey units, i.e., 22 spikey units in total and 2 flat units. In case we also connect the Daisy module, we can use a total of 32 dry electrodes mounted on the headwear frame.



(a) Spikey Units (b) Flat Units

Figure 4: Electrodes used for EEG recording

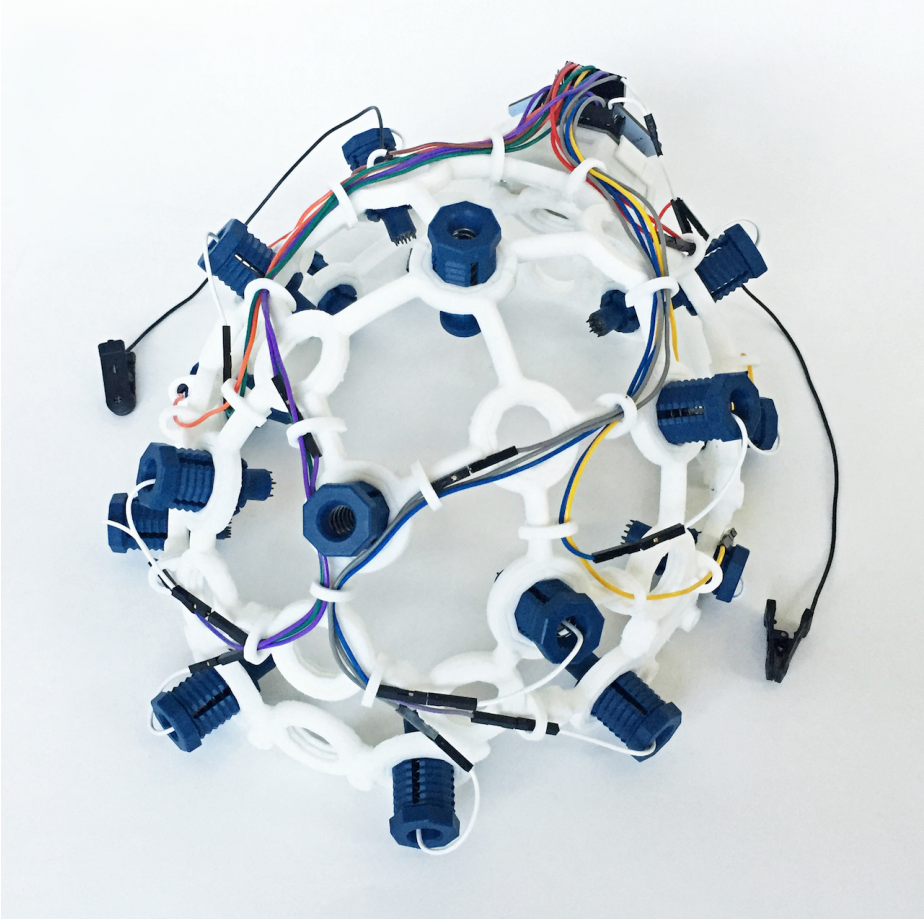


Figure 5: Assembled headwear with electrodes

Principle of Operation

ADC Topology

The original OpenBCI design had each of the ADCs communicate to the microcontroller through a single SPI bus. This was achieved by having each device send its data on the bus by taking turns. In order to implement this, each device had a designated chip select signal, and the microcontroller would selectively turn on a single chip select as needed. However, this scheme has drawbacks in the form of channel data being asynchronous. Furthermore, preliminary analysis of the firmware code suggests that it may be possible to implement a design wherein all the ADCs may be simultaneously selected to transmit their data.

We will look to assemble our ADC subsystem in a **Daisy chain** topology. The Daisy chain is an efficient means to assemble a large number of ADCs in order to obtain high channel counts. In a daisy chain, a single chip select from the microcontroller is shared by all the participating devices. The output of each ADC (D_{OUT}) is connected to the $DAISY_{IN}$ of the succeeding ADC. The result of this chain is that the final ADC in the chain outputs a stream of data corresponding to the outputs of all the preceding ADCs as well as its own data. Therefore, we only require this single ADC to communicate with the microcontroller through an SPI bus.

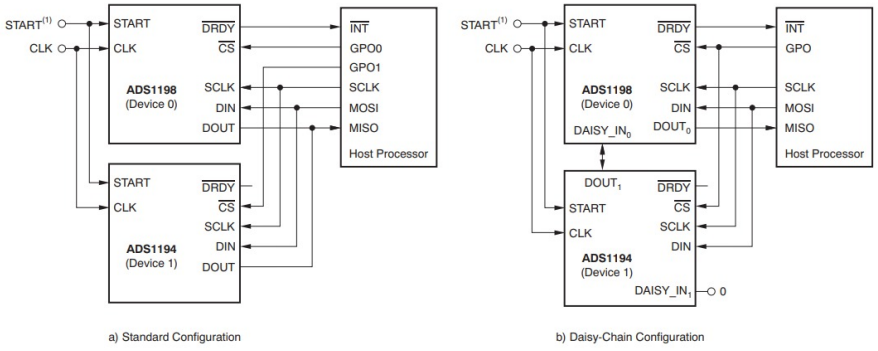


Figure 6: Comparison between standard operation and Daisy operation

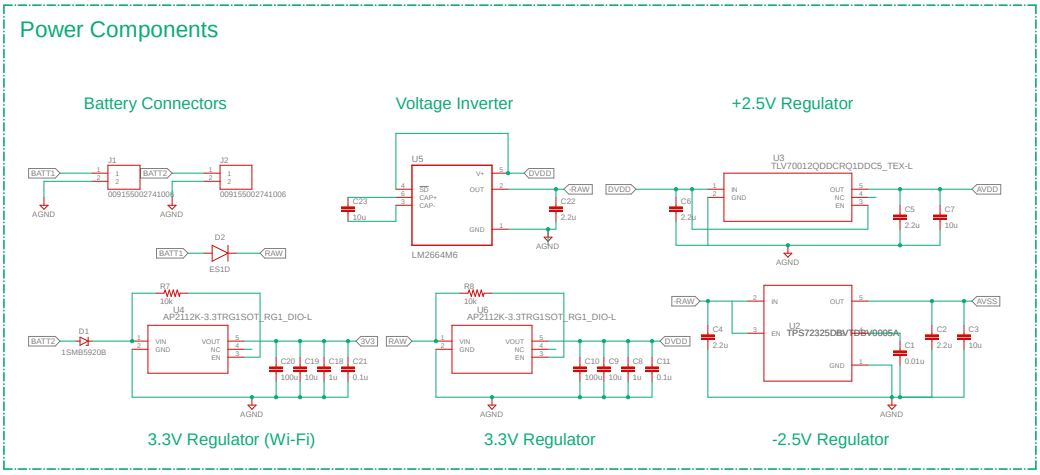
Microprocessor Interfacing

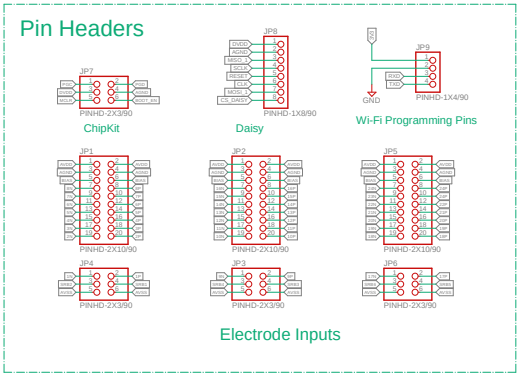
In the current iteration of the design, we have used 6 ADCs, an SD card module, an accelerometer, a WiFi module, and design inclusions for an external Daisy board interfacing. We plan on using four SPI buses for the above mentioned submodules. The breakup of SPI bus resource allocation is as follows-

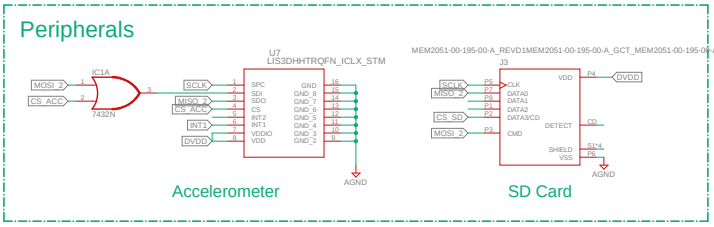
- **First SPI Bus** - For the six daisy-chained ADCs and External Daisy board interfacing
- **Second SPI Bus** - For the Wi-Fi module and peripherals such as SD Card slot and Accelerometer
- **PGEC and PGED** - For debugging (details in risk mitigation)

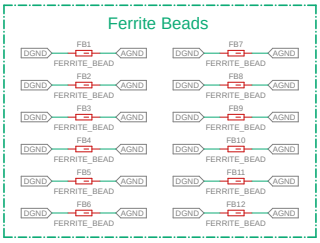
In the current milestone report submission, we have included the complete schematic for the PIC32 microcontroller. There are a certain number of pins that act as reprogrammable pins. The functions of these pins have been decided in the schematic in accordance to the options presented, and these pins will be made to operate in these modes through firmware code.

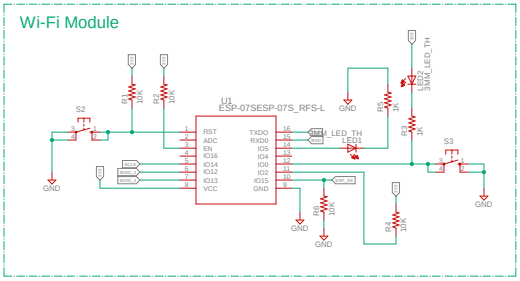
PIC32 Microcontroller


Power Components
Battery Connectors
Voltage Inverter
+2.5V Regulator
3.3V Regulator (Wi-Fi)
3.3V Regulator
-2.5V Regulator


Pin Headers
ChipKit
Daisy
Wi-Fi Programming Pins
Electrode Inputs

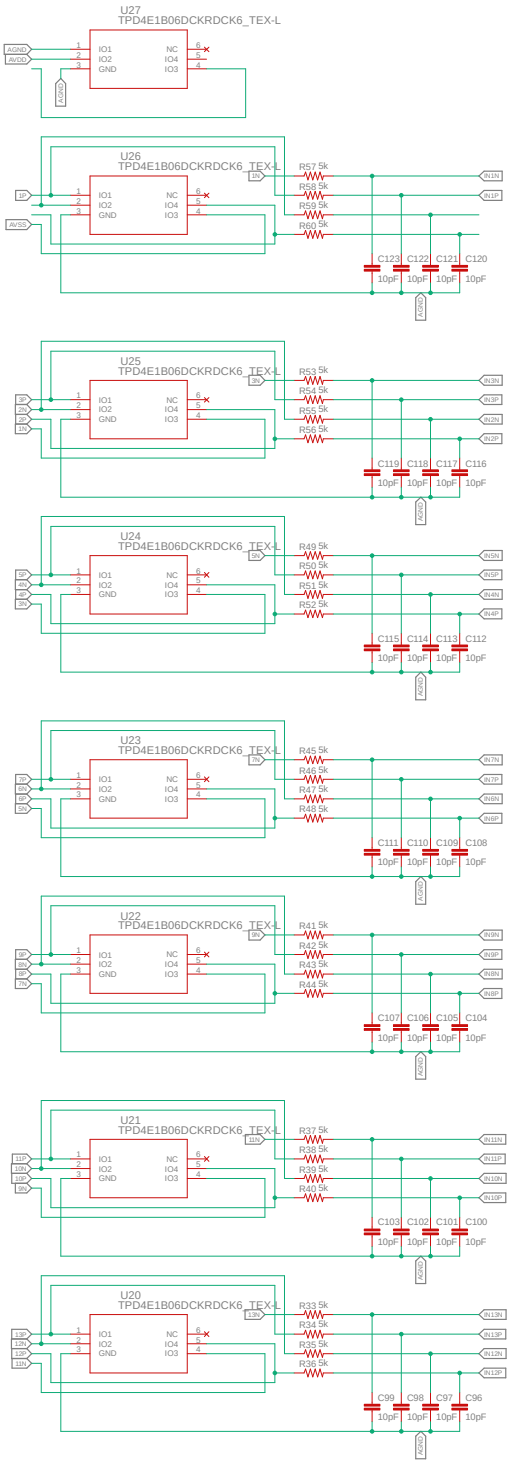

Peripherals
Accelerometer
SD Card


Ferrite Beads

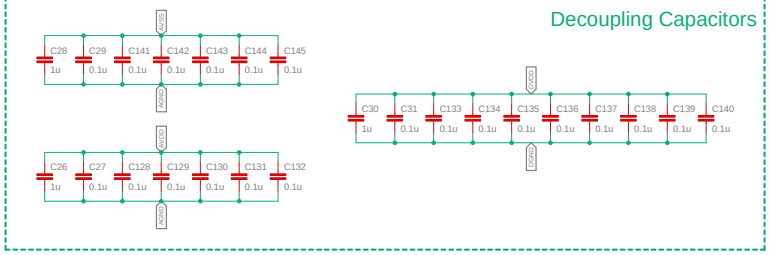

Wi-Fi Module

Daisy-Chain ADCs (Part 1)

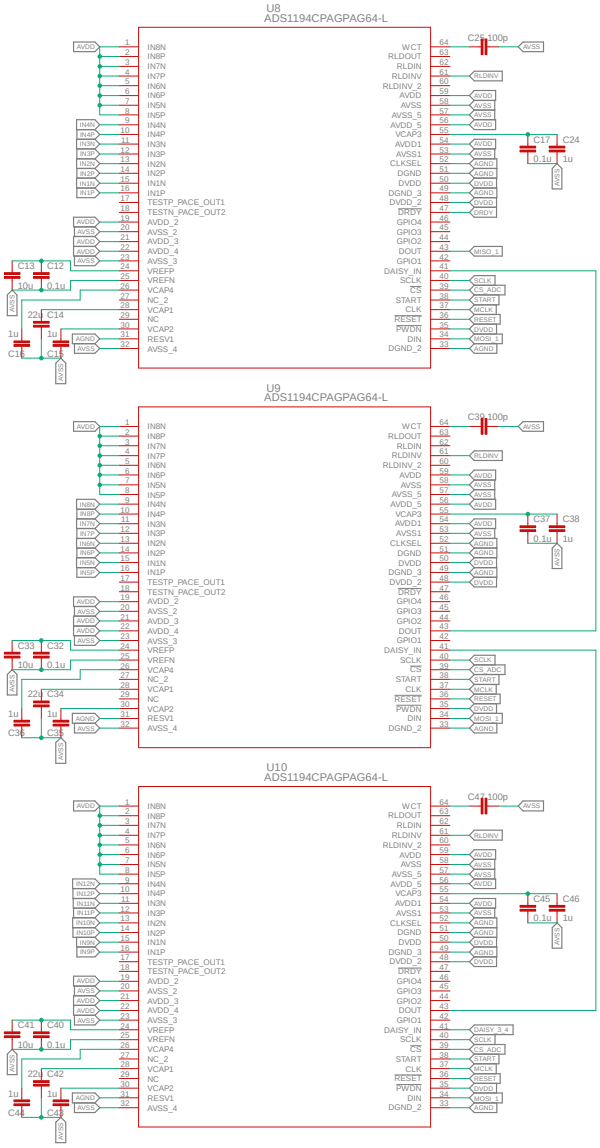
ESD Protection



Decoupling Capacitors

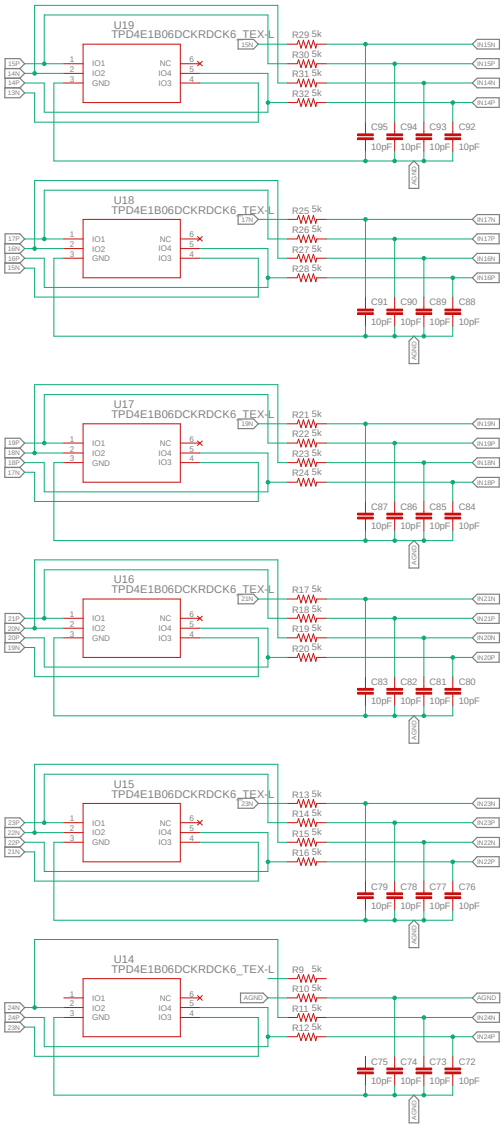


ADS 1194

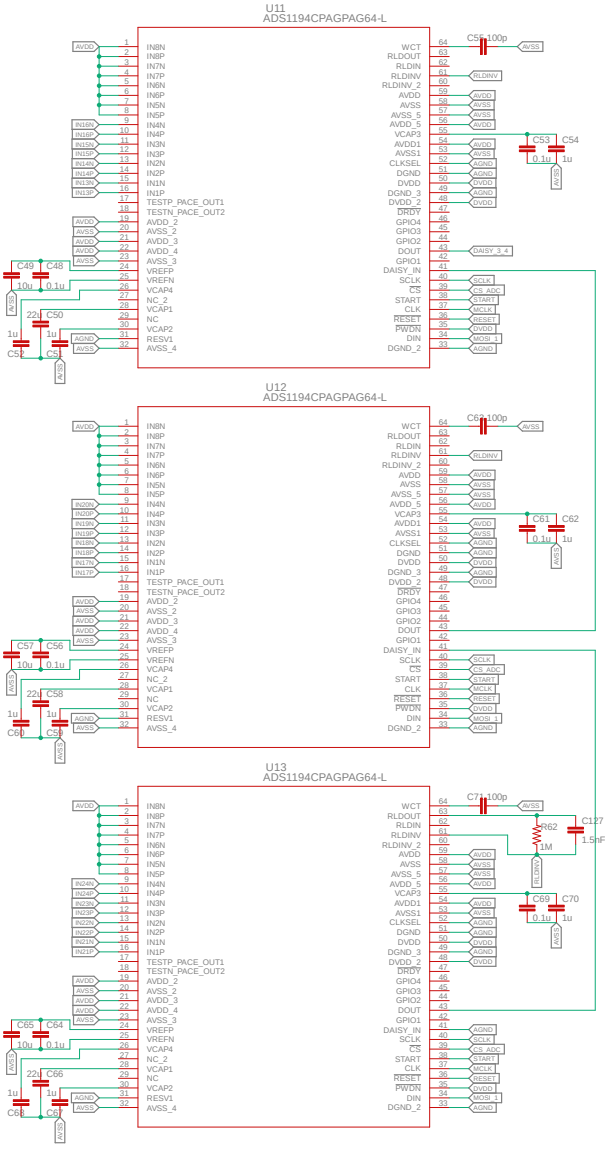


Daisy-Chain ADCs (Part 2)

ESD Protection



ADS 1194



Risk Mitigation

Alternatives for the A/D Converter

The ADS1194 A/D Converter converts the analog input into a digital value of 16 bits. For a reference voltage of $4V$, this leads to a LSB value of about $4V/(2^{15} - 1) \approx 122\mu V$. The Programmable Gain Amplifiers present in the ADS1194 have a maximum gain of 12 and the input EEG signals are in the range of $10\mu V - 100\mu V$. The 16-bit precision of the ADS1194 may be insufficient for representing such small EEG signals. So, we could swap this A/D Converter with the MCP3912, which is a 24-bit 4-channel A/D Converter used in the Ganglion Board by OpenBCI. The MCP3912 offers a much higher precision of $0.3\mu V$ per LSB bit.

Backwards Compatibility with the Daisy Module

The board we are designing is capable of reading from upto 24 electrodes, but we will also be adding the breakout pins and firmware code required to interface with the 8-channel Daisy module by OpenBCI, effectively increasing the total channels to 32. This is done so that in case the onboard A/D Converters fail, we will still have meaningful data coming from the Daisy module.

SPI reserved for programming/debugging

Similar to the original design by OpenBCI, we will be reserving an SPI bus (PGEC-PGED) on the microcontroller for debugging the system and programming the microcontroller. The remaining two SPI buses will be used for interfacing with the A/D Converters, Wi-Fi module, and peripheral components such as Accelerometer, SD Card, and also the Daisy breakout pins.

SD Card storage in case of Wi-Fi failure

The onboard SD Card reader will be retained from the original OpenBCI design so that in case the Wi-Fi transmission fails, we can still look at the data stored on the SD Card.

References

1. OpenBCI Documentation
2. https://arxiv.org/ftp/arxiv/papers/1808/1808.03711.pdf
3. ADS1194 Datasheet
4. PIC32MX250F128B/D Datasheet
5. ESP8266EX Datasheet
6. AP2112 Datasheet
7. LM2664 Datasheet
8. TPS72325 Datasheet
9. TLV700 Datasheet
10. LIS3DHHTR Datasheet
11. TPD4E1B06DCKR Datasheet