EE 344: Electronics Design Lab

OpenBCI based EEG Acquisition System

Group: TUE-18
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0.1 Aim

This project aims to design a pipeline that can be used to extract and process electroencephalography (EEG) data for visualization and analysis purposes. The signals of interest are noisy, small in amplitude, and must be extracted with high fidelity. The design is inspired by OpenBCI, a company that creates open-source tools for biosensing and neuroscience. Our group will be working with Group **TUE-06** to meet our target design.

0.2 Introduction

EEG is a non-invasive method of capturing brain signals. The device consists of two parts: recording electrodes and data-capturing electronics. The electrodes are placed on the subject's head to record different spatial locations on the brain. Each electrode corresponds to a single of data. For example, the OpenBCI Cyton board provides access to 8 channels of data. The Daisy expansion board offers support for an additional eight channels. The goal is to scale the existing design to accommodate 24 channels for better spatial resolution. The design will be robust to ambient noise (including the 50 Hz power supply interference) and has the potential to be used for a wide variety of applications, including medical diagnosis and brain-computer interfacing. The deliverables of the project will include the following,

1. A custom-designed PCB: The PCB will support 24 EEG channels, provide a Wi-Fi module for communicating with a laptop/computer/phone for real-time streaming, a micro-SD card for local storage, and accelerometer support for removing noise due to head motion
2. An EEG headset with electrodes placed at spatial locations recommended by the 10-20 international standard
3. A laptop/phone application to view the data in real-time

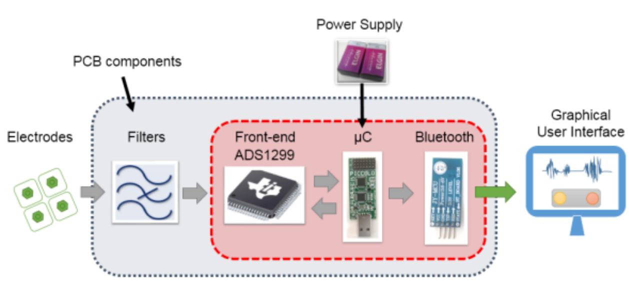

Figure 1: Existing OpenBCI design

0.3 Design Description

The OpenBCI Cyton Board is an 8-channel biosensing board. The existing setup takes in 8 analog inputs from the electrodes and passes them through an 8-channel A/D Converter. The digital output is sent to the microcontroller after which it is passed onto an RFduino Bluetooth Transmitter which transmits the data to a nearby device for viewing.

While scaling up the existing design to meet our requirements, there are multiple factors that we have taken into consideration. Firstly, our targeted 24-channel design would require 3 A/D converters to process the data provided by the electrodes. These devices will peripherally interface with the microcontroller, and therefore, our choice of the microcontroller will have to reflect this additional interfacing. Lastly, limitations on data rate across Bluetooth would impair the performance of our device, especially considering the larger amount of data our module targets to transmit as compared to the original design. To this end, we will look to transmit our data over Wi-Fi for better performance.

A high-level overview of our design is depicted in Figure 2. The subsections that follow give a brief overview of the role and functionality of each module and mention any changes from the existing design that we look to implement.

0.3.1 Electrodes

The EEG electrodes form the analog front end of the EEG processing pipeline and are of different types, including active, passive, dry, and sponge. Gold cup passive electrodes and a ten20 conductive paste will be used to reduce electrode-scalp impedance. The electrodes will be mounted on a custom 3D-printed headset, adhering to the 10-20 international standard for electrode placement.

Due to an increased electrode count, specific brain regions can be targeted to study functions like motor function, sensation, and memory. We will specifically target the frontal lobe's motor and visual cortex.

0.3.2 A/D Converters

The A/D converters are a vital part of the analog front end. In particular, we will be using the AD7768, a low-noise, 4-channel, 24-bit analog-to-digital converter. The AD7768 is a low-noise, fast-settling A/D converter for low bandwidth inputs.

After being passed through an ESD protection unit, electrode signals from 8 EEG channels are fed into the A/D converter that consists of four simultaneous samplings followed by delta-sigma ($\Delta\Sigma$) converters. The device also consists of a digital filter for each channel, capable of performing anti-aliasing operations,

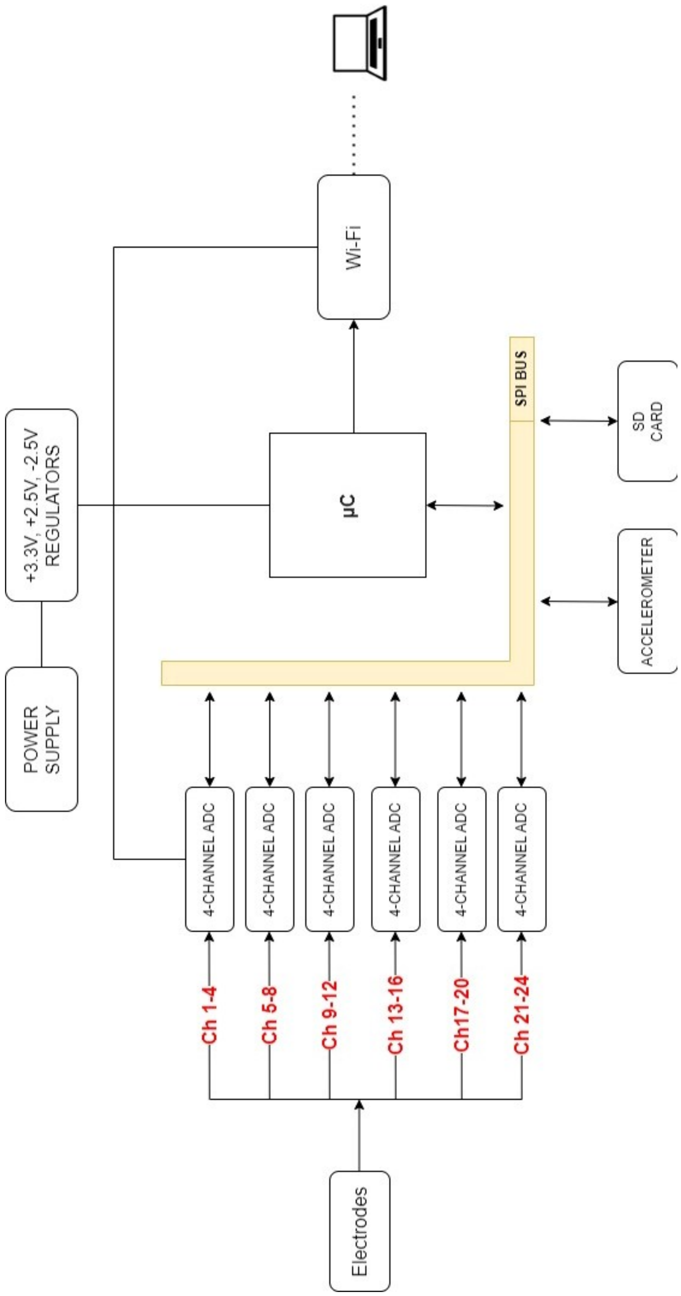

Figure 2: Design Block Diagram

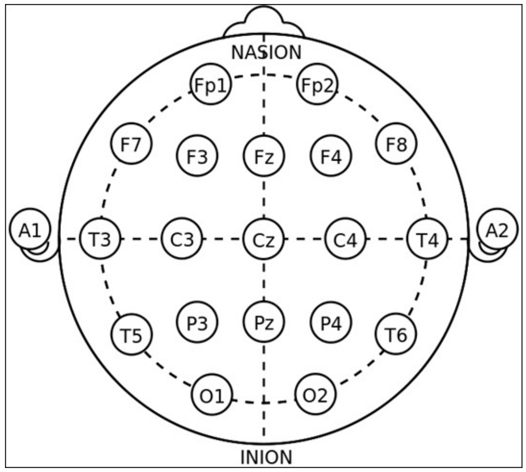

Figure 3: Electrode locations for EEG recording

while acting as a low-pass filter.

The output of the four converters is multiplexed into a single stream sent to the microcontroller over a serial interconnect (SPI). The data output sent on the `DOUT` pin consists of control bits followed by four sets of 24-bit quantized EEG data. Since the design requires 24 electrodes, 6 A/D converter chips will be on the final PCB.

0.3.3 Microcontroller

The microcontroller at the heart of the system is responsible for gathering data from the A/D Converters and the accelerometer, processing it, and passing the final values to the Wi-Fi and SD Card modules for transmission and storage, respectively. The original design for the Cyton board uses a 28-pin PIC32MX250F128B micro-controller, which comes with two I^2S/SPI modules for codec and serial communication, up to 13 channel 10-bit A/D Converters, and up to 19 I/O pins. Since the microcontroller will now be interfacing with 3 A/D Converters, the SD Card reader, and the Wi-Fi Module, we will be using the PC32MX250F128D micro-controller, which has a larger number of I/O pins (31), which can be reconfigured as chip select lines for the additional A/D Converters.

The microcontroller will be programmed using a chipKIT UDB32-MX2-DIP bootloader, with code written in the Arduino software library.

0.3.4 Power Supply

The components require a Digital Supply Voltage (`DVDD`) of $+3.3V$, an Analog Supply Voltage (`AVDD`) of $+2.5V$ and an Analog Ground Voltage (`AVSS`) of $-2.5V$. AP2112K-3.3TRG1 is a fixed LDO Voltage Regulator used to generate the `DVDD` signal using the input `RAW` signal. This `DVDD` signal is fed into the LM2664 Switched Capacitor Voltage Converter, which generates the `-RAW` signal. This `-RAW` signal is further passed through the TPS72325 Negative-output Linear Regulator to generate the `AVSS` signal. The `AVDD` signal is generated by passing the `DVDD` signal through the AP2112K-2.5TRG1 Voltage Regulator.

We will use a 3-6V DC Battery as the only power source for the board.

0.3.5 Accelerometer

The LIS3DHHTR is a three-axis accelerometer with digital I^2C/SPI serial interface standard output, capable of 16-bit data output. The purpose of the accelerometer is to remove artifacts in the EEG signal due to head movements. The data returned by the accelerometer is a good baseline to reconstruct what happened in the user's recording session.

The accelerometer can also be used as a marker for different phases of experimentation. Without the accelerometer, one would have to reset the data logging software. With the accelerometer, one can simply tap the board a few times and the created artifact would be easy to observe in the accelerometer's data stream.

0.3.6 SD Card

SD card is a necessary provision for logging data to local storage. This is useful in sleep study applications or when it is difficult to make wired connections to the PC. We will be using a Suntech ST-TF-003A SD card holder for the design. The data saved to the SD card is sampled at 250 Hz. This amounts to 3 MB of data per minute and hence, a high-speed SD card with large storage will be used (8 GB, 16 GB, or 32 GB). Data from the A/D converter will be sent to the SD card over an SPI bus.

0.3.7 Wi-Fi Module

Unlike the original design, a BLE module will not be included because of the requirement for frequent firmware updates. Another disadvantage of BLE is that the hardware must support the BLE protocol, which requires data packetization. On the other hand, Wi-Fi is based on a stream protocol which is easier to implement. OpenBCI provides a Wi-Fi shield in addition to the Cyton board, which has been known to suffer from packet losses and cyclical noise. We aim to overcome these defects by providing a reliable data transfer interface using an ESP8266 Wi-Fi Module, which is Arduino compatible.

0.3.8 Ultracortex Mark IV(headwear)

The Ultracortex Mark IV is a device developed by the OpenBCI company, which allows users to measure and record brain activity (EEG). The following are the main components of the headset: Cables, Spikey units, Flat units, Comfort units, Ear Clips. Unlike the original design, we have to use 8 more spikey units that are,22 spikey units in total and 2 flat units.

0.4 Project Plan

Duration	Task
T0	Design Review Milestone
T1 = T0 + 1 week	Rough Schematic joining all the components + Understand the existing firmware code + Get started with the 3D printing process for the headgear
T2 = T1 + 1 week	Start testing and assembling components on breadboard + Get started with the PCB Design
T3 = T2 + 1 week	Schematics and preliminary analysis review milestone + Start modifying the firmware code to accommodate additional components
T4 = T3 + MidSem Week	
T5 = T4 + 1 week	Finish the PCB Design for all the layers + Finish the process for the headgear
T6 = T5 + 1 week	Layouts and CAD review milestone
T7 = T6 + 10 days	Soldering the components on the PCB + Initial Subsystem testing review - 1
T8 = T7 + 10 days	Calibrating the board and the headgear in a Faraday cage + Testing the SD Card and Wi-Fi functions + Individual subsystem testing review - 1
T9 = T8 + 1 week	Final demo

0.5 Work Division

We have divided the work required for the project into three distinct but interweaved subdivisions -

- **Hardware** - Testing the hardware, and working with various aspects involved in verification are majorly worked on by our teammates Shivam Patel (TUE-06) and Anubhav Bhatla (TUE-18). Interfacing different devices, and ensuring that the specifics of PCB and firmware are smoothly coordinated will also be ensured by this subdivision.
- **Firmware** - The Firmware subdivision will work on the existing codebase for the OpenBCI Cyton Board. Understanding the implementational details, making necessary modifications, and adjusting the code for meeting

our design requirements will be handled by Aditya Sriram (TUE-06) and Ankith R. (TUE-18).

- **PCB Design** - The task of comprehending the existing PCB design of the Cyton Board and adjusting it will be looked over by the PCB Design subdivision. Emulating and extending the PCB layout to accommodate 24 channels will be the responsibility of Aayush Rajesh (TUE-06) and Nithish S. (TUE-18). New schematics and a layout plan will be developed for the novel 24-channel board.

The work distribution amongst teammates is subject to revision and proliferation, depending on the project advancement and necessities.

Subdivision	**TUE-06 Group**	**TUE-18 Group**
Hardware	Shivam Patel	Anubhav Bhatla
Firmware	Aditya Sriram	Ankith R.
PCB Design	Aayush Rajesh	Nithish S.

0.6 Bill of Materials

Device Code	Generic Name	Quantity	Link
AD7768-4BSTZ	ADC	8	Digikey
PIC32MX250F128D-50I/PT	PIC Microprocessor	2	Mouser
PICKIT3	PIC Programmer	1	Robu / ElecComp
ESP8266	Wifi Module	2	ElecComp
AP2112K-3.3TRG1	DVDD Voltage Regulator	4	Digikey
LM2664	Switched Cap V Regulator	2	Digikey
TPS72325	Neg. O/P Linear Regulator	2	Mouser
TLV70012QDDCRQ1	AVDD Voltage Regulator	2	Mouser
LIS3DHHTR	Accelerometer	2	Digikey
Sandisk 128GB MicroSD Class 10	SD Card	1	Amazon
TPD4E1B06DCKR	ESD Protection Devices	25	Digikey
CAY16-2201F4LF	Resistor Array	20	Digikey
Gold Cup Passive Electrodes (10x)	Conducting Electrodes	4	OpenBCI
Ten 20 Conductive Paste (8 oz.)	Conducting Paste	1	OpenBCI
Micro SD Card Port	MicroSD port	2	RoboticsDNA
Passive Components			Sheets

0.7 References

1. OpenBCI Documentation
2. https://arxiv.org/ftp/arxiv/papers/1808/1808.03711.pdf
3. AD7768 Datasheet

4. PIC32MX250F128B/D Datasheet
5. ESP8266EX Datasheet
6. AP2112 Datasheet
7. LM2664 Datasheet
8. TPS72325 Datasheet
9. TLV700 Datasheet
10. LIS3DHHTR Datasheet
11. TPD4E1B06DCKR Datasheet