

A Textbook on Basic Electronics Engineering

Insights on

BASIC

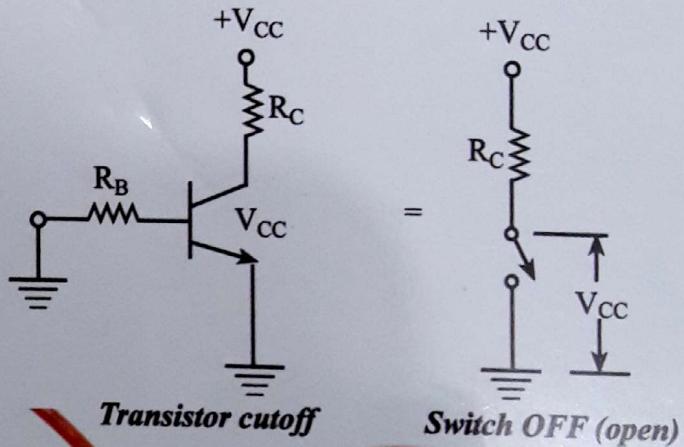
**ELECTRONICS
ENGINEERING**

TU, PU, PoU, KU

features

- A textbook with **INSTANT NOTES**
- Solution to large number of **numericals**
- Solution to past questions of **IOE exams.**

Fifth Edition

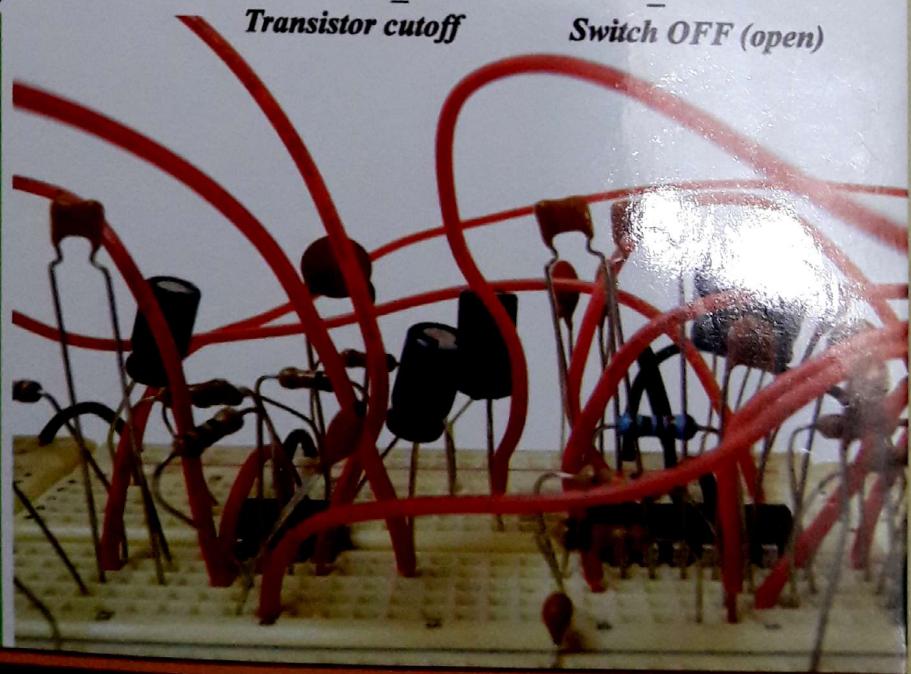


Written by:

- Er. Shyam Dahal
- Er. Santosh Poudel
- Er. Reshma Maharjan
- Er. Rajib Rimal

Edited by:

- Er. Rajan Lama
- Er. Kunjan Amatya
- Er. Shree Krishna Sulu



Apruba Porpharel
73013

INSIGHTS ON

BASIC ELECTRONICS ENGINEERING

Written by

Er. Shyam Dahal
Lecturer, KEC, Kalimati

Er. Santosh Poudel
Lecturer, KEC, Dhapakhel

Er. Reshma Maharjan
Lecturer, KEC, Kalimati

Er. Rajib Rimal
Lecturer, Kathford International College

Edited by

Er. Rajan Lama
Senior Lecturer, KEC, Kalimati

Er. Kunjan Amatya
Senior Lecturer, KEC, Kalimati

Er. Shree Krishna Sulu
Senior Lecturer, KEC, Kalimati

SYSTEM INCEPTION

Koteshwor, Kathmandu

Ripple VOLTAGE of capacitor filter when connected across a rectifier	86
Zener voltage regulator	89
<i>Answers to some questions</i>	96

Chapter 3

TRANSISTORS

Introduction	98
Construction and operation of NPN BJT	98
Beta (β) and alpha (α)	100
BJT biasing	101
BJT configuration	105
BJT switch and logic circuits	111
Transistor modeling	116
The hybrid- π model	118
The T model	119
Differential amplifier	120
Field-effect transistors	122
MOSFET	123
Enhancement-type MOSFET	123
Depletion-type MOSFET	127
Complementary MOS or CMOS	131
<i>Answers to some questions</i>	134

Chapter 4

THE OPERATIONAL AMPLIFIER AND OSCILLATOR

Introduction	147
Internal block diagram OF AN OP – AMP	147
The ideal OP- AMP	147
Some basic terms	148
Virtual ground	150
Virtual short	151
Applications of OP-AMPS	152
1. Inverting amplifier	152
2. Non- inverting amplifier	153
3. Adder	154
4. Subtractor	155
5. Integrator	156
6. Differentiator	157
Feedback	159
Positive feedback	159

• Negative feedback	160
• Oscillator	160
• Feedback oscillators	161
• Barkhausen criteria	161
• Square wave generator (Astable multivibrator)	163
• Triangular wave generator	165
• Wien-bridge oscillator	166

Chapter 5

COMMUNICATION SYSTEM

• Introduction	169
• Analog and digital signals	170
• Modulation	170
• Analog modulation techniques	170
• Amplitude modulation (AM)	170
• Angle modulation	171
- Phase modulation (PM)	171
- Frequency modulation (FM)	172
• Digital modulation techniques	173
• Digital communication system	173
• Optical fibre communication	176
• Electromagnetic wave	179
• Antennas	181
• Broadcasting and communication	182
• Wired & wireless communication	184
• Internet & intranet	185
<i>Answers to some questions</i>	187

Chapter 6

DIGITAL ELECTRONICS

• Introduction	190
• Number systems	190
• Logic gates	199
• De Morgan's first law	201
• De Morgan's second law	201
• Universal gates	202
• NOR gate	202
• NAND gate	202
• Boolean algebra	203
• Combinational circuit	203
• Adder	204

Subtractor	206
Binary Adder-Subtractor	208
Decoders	209
Encoder	210
Multiplexers	211
Demultiplexers	213
Binary arithmetic	216
Complements	219
Canonical and standard forms	222
Karnaugh map or K - map	224
Sequential circuits	235
Flip- flop	236
Latches	236
Some latches	237
Some flip-flops	239
Characteristic table of different flip-flops	243
Registers	244
Counters	244
Shift registers	244
Duality principle	244
<i>Answers to some questions</i>	247
	248

Chapter 7

APPLICATION OF ELECTRONIC SYSTEM

Introduction	250
Transducers and sensors	250
Transducers	250
Sensors	250
Measurement and instrumentation system	251
Strain gauge	252
Digital multimeter (DMM)	253
Cathode ray oscilloscope (CRO)	255
Regulated power supply (DC power supply)	257
Remote control	259
Character display	260
Clock counter measurement	261
Data logger	262
Audio video system	263
<i>Answers to some questions</i>	264
	267
Appendix	270
Bibliography	272

BASIC CIRCUITS CONCEPT

INTRODUCTION

Electric circuits, which are collections of circuit elements connected together, are the most fundamental structures of electrical engineering. A circuit is an interconnection of simple electrical devices that have at least one closed path in which current may flow. Circuits are important because they process electrical signals, which carry energy and information. An electric circuit, as we will discuss, is an idealized mathematical model of some physical circuit or phenomenon. The ideal circuit elements are the resistor, the inductor, the capacitor, and the voltage and current sources. The ideal circuit model helps us to predict, mathematically, the approximate behavior of the actual event. The models also provide insights into how to design a physical electrical circuit to perform a desired task.

ACTIVE AND PASSIVE COMPONENTS

Active device is a device that exhibits gain (current or voltage, or both) and has a directional electronic function. Transistors are active devices. On the other hand, passive device or component is a device that exhibits no gain and no directional function. Resistors, capacitors, and inductors are passive components. Passive components are classified into two groups: Those which dissipate energy (e.g., resistors) and those which store energy (e.g., capacitors, inductors).

RESISTOR AND RESISTANCE

A resistor has been defined as a physical device that limits or regulates the flow of electric current in an electronic circuit. Resistance may be defined as the property of a substance due to which it opposes (or restricts) the flow of electricity through it. The SI unit of resistance is ohm (Ω). Resists + heat due

Types of resistor

There is a wide range of resistor types. Three of the most common methods of construction are:

1. Wire wound resistors
2. Metal oxide resistors
3. Carbon resistors

Resistance in series

When the resistors are joined end-on-end, they are said to be connected in series. Let R_1 , R_2 , and R_3 be the resistances of conductors connected in series.

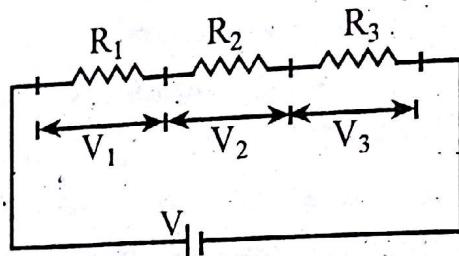


Figure 1.1 Series combination of resistance

The sum of the voltage drops on conductors is equal to the voltage applied.

$$V = V_1 + V_2 + V_3 = I_1 R_1 + I_2 R_2 + I_3 R_3$$

As same amount of current flows through each conductors,

$$I_1 = I_2 = I_3 = I \text{ (say)}$$

$$\therefore V = IR_1 + IR_2 + IR_3 = I(R_1 + R_2 + R_3)$$

Let R be the equivalent resistance that draws current I with same voltage applied. This will make $V = IR$.

$$\text{or, } IR = I(R_1 + R_2 + R_3)$$

$$\therefore R = R_1 + R_2 + R_3$$

For n conductors connected in series,

$$R = R_1 + R_2 + R_3 + \dots + R_n$$

Resistance in parallel

Consider the parallel combination of conductors having resistances R_1 , R_2 , and R_3 as shown in the Figure 1.2.

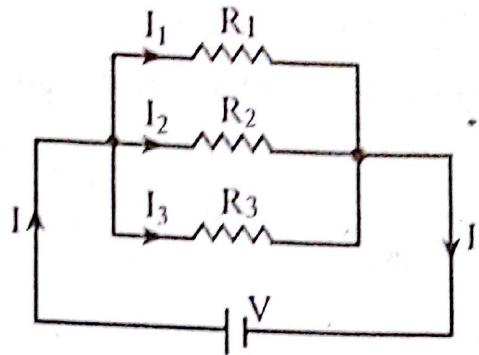


Figure 1.2 Resistance in parallel

The sum of currents through each conductors is equal to the current drawn from the voltage source.

$$I = I_1 + I_2 + I_3 = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

Potential difference across each resistance is same, and is equal to the applied voltage.

$$V_1 = V_2 = V_3 = V$$

$$\text{or, } I = \frac{V}{R_1} + \frac{V}{R_2} + \frac{V}{R_3} = V \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right)$$

$$\text{or, } \frac{I}{V} = \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right) \dots\dots \text{(i)}$$

If R is the equivalent resistance that draws current I when voltage V is applied, then

$$R = \frac{V}{I} \Rightarrow \frac{1}{R} = \frac{I}{V} \dots\dots \text{(ii)}$$

From equations (i) & (ii)

$$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}$$

For n conductors connected in parallel

$$\boxed{\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \dots\dots + \frac{1}{R_n}}$$

Colour coding of a resistor

Carbon and metal oxide resistors are normally marked with colour codes which indicate their value and tolerance. The colour code for fixed resistors is given in the table.

Colour	Significant figures	Multiplier	Tolerance
Silver	—	10^{-2}	$\pm 10\%$
Gold	—	10^{-1}	$\pm 5\%$
Black	0	1	—
Brown	1	10	$\pm 1\%$
Red	2	10^2	$\pm 2\%$
Orange	3	10^3	—
Yellow	4	10^4	—
Green	5	10^5	$\pm 0.5\%$
Blue	6	10^6	$\pm 0.25\%$
Violet	7	10^7	$\pm 0.1\%$
Grey	8	10^8	—
White	9	10^9	—
None	—	—	$\pm 20\%$

Table 1.1 Colour code of fixed resistors

- i. For a **four-band fixed resistor** (i.e., resistance values with two significant figures): Yellow-violet-orange-red indicates $47 \text{ K}\Omega$ with a tolerance of $\pm 2\%$.
(Note that the first band is the one nearest the end of the resistor)
- ii. For a **five-band fixed resistor** (i.e., resistance values with three significant figures): Red-yellow-white-orange-brown indicates $249 \text{ K}\Omega$ with a tolerance of $\pm 1\%$.
(Note that the fifth band is 1.5 to 2 times wider than the other bands)

Problem 1.1

Determine the value and tolerance of a resistor having a colour coding of: orange-orange-silver-brown.

Solution:

The first two bands i.e., orange-orange give 33. The third band, silver indicates a multiplier of 10^{-2} which means that the value of the resistor is $33 \times 10^{-2} = 0.33 \Omega$. The fourth band i.e.,

brown indicates a tolerance of $\pm 1\%$. Hence, a colour coding of orange-orange-silver-brown represents a resistor of $0.33 \pm 1\% \Omega$.

Problem 1.2

Determine the colour coding for a $47 K\Omega$ having a tolerance of $\pm 5\%$

Solution:

$47 K\Omega = 47 \times 10^3$ has a colour coding of yellow-violet-orange. With a tolerance of $\pm 5\%$, the fourth band will be gold. Hence, the required colour coding is yellow-violet-orange-gold.

Problem 1.3

Find the value of resistor from following colour code.

a. Red Orange Green Silver

b. Yellow Black Gold

[2070 Magh]

Solution:

$$(a) R_1 = 23 \times 10^5 \pm 10\% = 2300000 \pm 10\% \Omega$$

$$(b) R_2 = 40 \times 10^{-1} \pm 5\% = 4 \pm 5\% \Omega$$

Remember !

Color	Significant figures	Multiplier	Tolerance
Black (B)	0	1	-
Brown (B)	1	10^1	$\pm 1\%$
Red (R)	2	10^2	$\pm 2\%$
Orange (O)	3	10^3	-
Yellow (Y)	4	10^4	-
Green (G)	5	10^5	$\pm 0.5\%$
Blue (B)	6	10^6	-
Violet (V)	7	10^7	-
Gray (G)	8	10^8	-
White (W)	9	10^9	-
Golden	-	10^{-1}	$\pm 5\%$
Silver	-	10^{-2}	$\pm 10\%$

NOTE: BB ROY Of Great Britain has a Very Good Wife

CAPACITOR AND CAPACITANCE

The capacitor has been defined as a physical device which is capable of storing energy by virtue of voltage existing across it. The voltage applied across the capacitor sets up an electric field within it and the energy is stored is stored in the electric field. A capacitor essentially consists of two conducting surfaces separate by a layer of an insulating medium called dielectric. The capacitance of a capacitor is defined as the amount of charge required to create a unit potential difference between its plates. Mathematically,

$$\text{Capacitance } (C) = \frac{Q}{V}$$

The unit of capacitance is farads (F).

Types of capacitor

According to the material used for their dielectric, the capacitors are of following types:

1. Variable air capacitors
2. Mica capacitors
3. Paper capacitors
4. Ceramic capacitors
5. Plastic capacitors
6. Titanium oxide capacitors
7. Electrolytic capacitors

Capacitance in series

Figure 1.3 below shows three capacitors having the right-hand plate of one connected to the left-hand plate of the next and so on. This arrangement is series connection of capacitors.

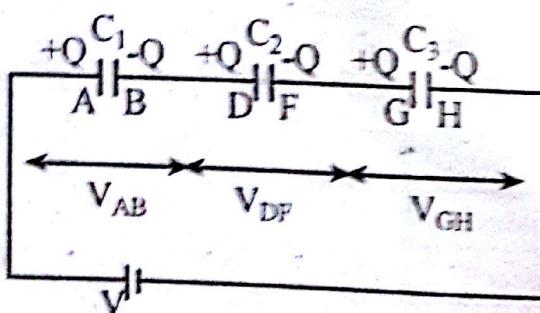


Figure 1.3 Series connection of capacitors

When a cell is connected across the ends of the system, a charge Q is transferred from the plate H to the plate A, a charge $-Q$ being left on H. This charge induces a charge $+Q$ on plate G; similarly, charges appear on all the other capacitor plates, as shown in Fig. The potential differences across the individual capacitors are, therefore given by

$$V_{AB} = \frac{Q}{C_1}, V_{DF} = \frac{Q}{C_2}, V_{GH} = \frac{Q}{C_3}$$

The sum of these is equal to the applied potential difference V .

$$V = V_{AB} + V_{DF} + V_{GH}$$

$$= \frac{Q}{C_1} + \frac{Q}{C_2} + \frac{Q}{C_3} = Q \left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} \right)$$

$$\text{or, } \frac{V}{Q} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} \dots\dots \text{ (i).}$$

The resultant capacitance (C) of the system is the ratio of the charge stored to the applied voltage.

$$C = \frac{Q}{V} \Rightarrow \frac{V}{Q} = \frac{1}{C} \dots\dots \text{ (ii).}$$

From equations (i) & (ii), we have

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$$

For n capacitors in series,

$$\boxed{\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} + \dots\dots\dots + \frac{1}{C_n}}$$

Capacitance in parallel

In the **Figure 1.4** shown below, three capacitors having all their left-hand plates connected together and all their right-hand plates likewise. This arrangement is parallel connection of capacitors.

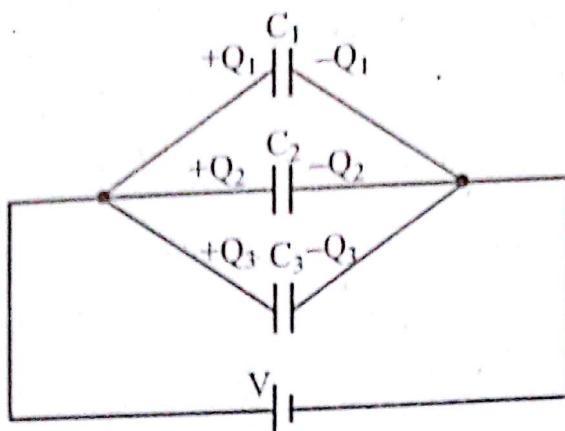


Figure 1.4 Parallel connection of capacitors

As $Q = CV$, the charges on the individual capacitors are respectively

$$Q_1 = C_1 V, Q_2 = C_2 V, Q_3 = C_3 V$$

The total charge on the system of capacitors is

$$Q = Q_1 + Q_2 + Q_3 = (C_1 + C_2 + C_3) V$$

And the system is, therefore, equivalent to a single capacitor of capacitance

$$C = \frac{Q}{V} = \frac{(C_1 + C_2 + C_3)V}{V}$$

$$\therefore C = C_1 + C_2 + C_3$$

For n capacitors in parallel,

$$C = C_1 + C_2 + C_3 + \dots + C_n$$

INDUCTOR AND INDUCTANCE

An inductor has been defined as a physical device which is capable of storing energy by virtue of a current flowing through it. It offers high impedance to ac but very low impedance to dc, that is, it blocks ac signal but passes dc signal. Inductance is a property of opposing the change of current flowing through it. The SI unit of inductance is Henry (H).

Types of inductor

According to the core material, inductors can be classified as

1. Air cored
2. Ferrite cored

3. Ferrite pot cored

4. Iron cored

Inductance in series

There are two methods of combination of inductors in series. If the coils having inductance L_1 and L_2 , are connected in such a way that when the current enters the dot end of coil L_1 and leaves, it must enter L_2 at its dotted end, which results in the addition of fluxes of two coils, then this type of series connection is known as series aiding. But, if they are connected in a manner that when the current enters the dot end of coil L_1 and leaves, it must enter L_2 at its undotted end; which makes fluxes of coils oppose each other, then this type of series connection is known as series opposing.

a. Series aiding

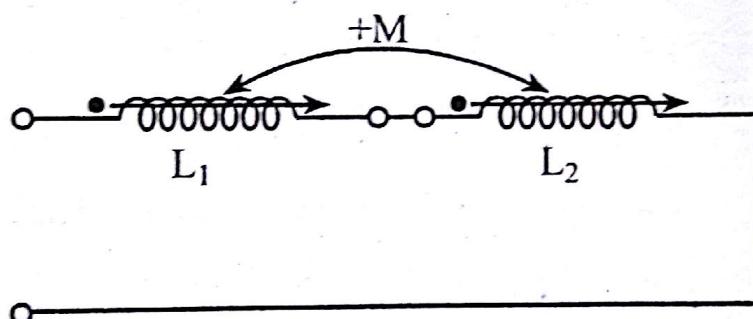


Figure 1.5 Series aiding connection of inductors

For this type of connection, the total emf induced in each of the coils L₁ and L₂ is due to coil's self inductance and the emf induced by the other coil. So,

$$e_1 = L_1 \frac{di}{dt} + M \frac{di}{dt} = (L_1 + M) \frac{di}{dt}$$

where M = coefficient of mutual inductance

$$e_2 = L_2 \frac{di}{dt} + M \frac{di}{dt} = (L_2 + M) \frac{di}{dt}$$

Total emf induced in the circuit is

$$e = e_1 + e_2 = (L_1 + L_2 + 2M) \frac{di}{dt}$$

$$\text{or, } \frac{e}{di} = L_1 + L_2 + 2M$$

or, $L = L_1 + L_2 + 2M$; L = total inductance of the circuit.

$$\therefore L = L_1 + L_2 + 2M$$

b. Series opposing

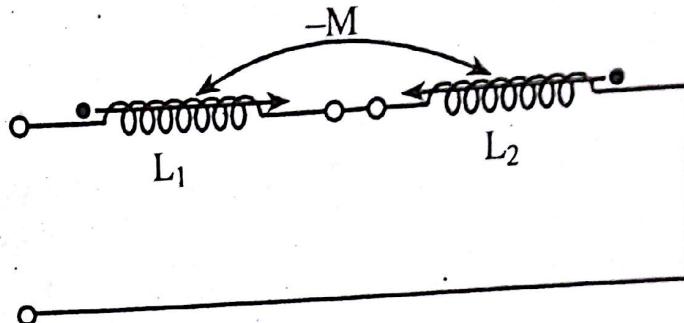


Figure 1.6 Series opposing connection of inductors

For the type of connection, the mutually induced emf opposes the self induced emf. So,

$$e_1 = L_1 \frac{di}{dt} - M \frac{di}{dt} = (L_1 - M) \frac{di}{dt}$$

where M = coefficient of mutual inductance

$$e_2 = L_2 \frac{di}{dt} - M \frac{di}{dt} = (L_2 - M) \frac{di}{dt}$$

Total emf induced in the circuit is

$$e = e_1 + e_2 = (L_1 + L_2 - 2M) \frac{di}{dt}$$

$$\text{or, } \frac{e}{di} = L_1 + L_2 - 2M$$

or, $L = L_1 + L_2 - 2M$; L = total inductance of the circuit.

$$\therefore L = L_1 + L_2 - 2M$$

Inductance in parallel

Consider two coils of inductances L_1 and L_2 connected in parallel as shown in **Figure 1.7**.

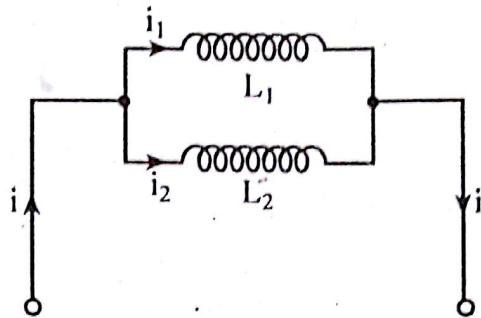


Figure 1.7 Parallel connection of inductors

$$i = i_1 + i_2$$

$$\text{or, } \frac{di}{dt} = \frac{di_1}{dt} + \frac{di_2}{dt} \dots\dots\dots (i)$$

Self induced emf in coil A, $e_{LA} = -L_1 \frac{di_1}{dt}$

Mutually induced emf in coil A due to change of current in coil B is

$$e_{MA} = -M \frac{di_2}{dt}; M = \text{coefficient of mutual inductance}$$

Resultant emf induced in coil A is

$$e_A = e_{LA} + e_{MA} = -L_1 \frac{di_1}{dt} - M \frac{di_2}{dt}$$

Similarly, resultant emf induced in coil B is

$$e_B = -L_2 \frac{di_2}{dt} - M \frac{di_1}{dt}$$

As both coils are connected in parallel, we have

$$e_A = e_B$$

$$\text{or, } -L_1 \frac{di_1}{dt} - M \frac{di_2}{dt} = -L_2 \frac{di_2}{dt} - M \frac{di_1}{dt}$$

$$\text{or, } (L_1 - M) \frac{di_2}{dt} = (L_2 - M) \frac{di_1}{dt}$$

$$\text{or, } \frac{di_1}{dt} = \left(\frac{L_2 - M}{L_1 - M} \right) \frac{di_2}{dt} \dots\dots (ii)$$

$$\text{or, } \frac{di_1}{dt} + \frac{di_2}{dt} = \left(\frac{L_2 - M}{L_1 - M} \right) \frac{di_2}{dt} + \frac{di_2}{dt} = \left[\left(\frac{L_2 - M}{L_1 - M} \right) + 1 \right] \frac{di_2}{dt}$$

$$\text{or, } \frac{di}{dt} = \left(\frac{L_1 + L_1 - 2M}{L_1 - M} \right) \frac{di_2}{dt} \quad \dots \text{ (iii) [using equation (i)]}$$

If L is the equivalent inductance of the combination, then
induced emf = $-L \frac{di}{dt}$

Since induced emf in parallel combination = induced emf in either of the coils, we have

$$L \frac{di}{dt} = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt}$$

$$\text{or, } L = \frac{L_1 \frac{di_1}{dt} + M \frac{di_2}{dt}}{\frac{di}{dt}}$$

Substituting $\frac{di_1}{dt} = \left(\frac{L_2 - M}{L_1 - M} \right) \frac{di_2}{dt}$ from equation (ii) and

$\frac{di}{dt} = \left[\frac{L_1 + L_1 - 2M}{L_1 - M} \right] \frac{di_2}{dt}$ from equation (iii), we get.

$$L = \frac{L_1 \left[\frac{L_2 - M}{L_1 - M} \right] \frac{di_2}{dt} + M \frac{di_2}{dt}}{\left[\frac{L_1 + L_2 - 2M}{L_1 - M} \right] \frac{di_2}{dt}}$$

$$\text{or, } L = \frac{L_1 L_2 - L_1 M + L_1 M - M^2}{L_1 + L_2 - 2M}$$

$\therefore L = \frac{L_1 L_2 - M^2}{L_1 + L_2 - 2M}$ when mutual flux helps individual flux
(aiding combination).

But,

$L = \frac{L_1 L_2 - M^2}{L_1 + L_2 + 2M}$ when mutual flux opposes the individual
flux (opposing combination).

KIRCHHOFF'S LAWS

i. Kirchoff's point law or current law (KCL)

It may be stated as follows:

In any electrical network, the algebraic sum of the currents meeting at a point (or junction) is zero. Put in another way, it simply means that the total current leaving a junction is equal to the total current entering that junction.

In Figure 1.8,

$$(I_1) + (-I_2) + (-I_3) + (+I_4) + (-I_5) = 0$$

$$\text{or, } I_1 + I_4 = I_2 + I_3 + I_5$$

incoming currents = outgoing currents

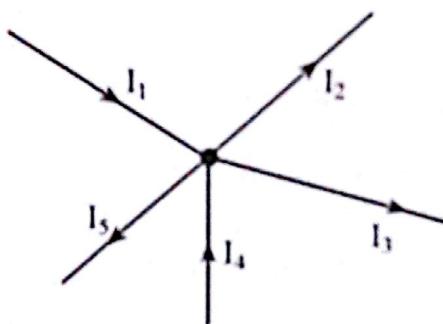


Figure 1.8 For illustrating Kirchoff's current law

ii. Kirchoff's mesh law or voltage law (KVL)

It may be stated as follows:

The algebraic sum of the products of currents and resistances in each of the conductors in any closed path (or mesh) in a network plus the algebraic sum of the emfs in that path is zero.

$$\Sigma IR + \Sigma_{\text{emf}} = 0 \quad \text{round a mesh}$$

It should be noted that algebraic sum is the sum which takes into account the polarities of voltage drops.

LINEARITY

Resistive elements for which the volt-ampere characteristic is a straight line are called linear elements and the electric

Circuits containing them are linear circuits.

circuits containing only linear resistances are called linear circuits.

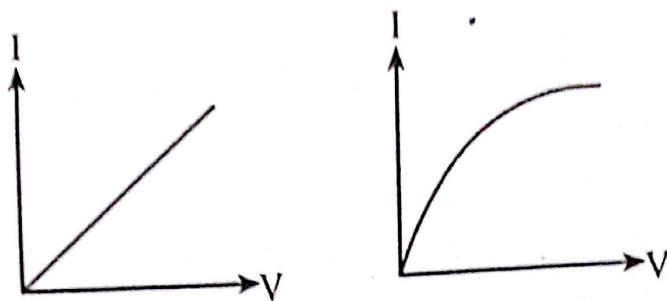


Figure 1.9 Illustration of volt-ampere characteristics

Resistive elements for which the volt-ampere characteristic is other than a straight line are termed nonlinear and the electric circuits containing them are nonlinear circuits. Example of nonlinear elements includes tungsten lamps, vacuum tubes, transistors, etc.

SIGNAL SOURCES

There are two types of sources of electrical energy, the voltage source and the current source. They are two-terminal element either independent or dependent as follows:

A. Independent sources

1. The voltage source

The voltage source is assumed to deliver energy with a terminal voltage.

i. An ideal voltage source

An ideal voltage source is one which maintains a constant terminal voltage $v(t)$ regardless of the value of the current through its terminals.

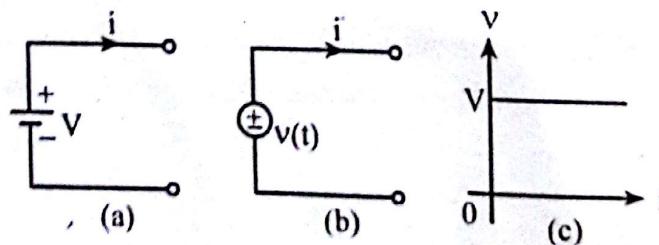


Figure 1.10 (a-b) ideal voltage source (c) It's $v-i$ characteristic

ii. A practical voltage source

A practical voltage source is one in which the voltage across the terminals of the source keeps falling as the current it increases. This behavior can be explained by connecting a resistance r in series with an ideal voltage source. Then, we have the terminal voltage v_1 as

$$v_1 = v - i_1 r$$

where i_1 is the current flowing and r the internal resistance of the ideal voltage source.

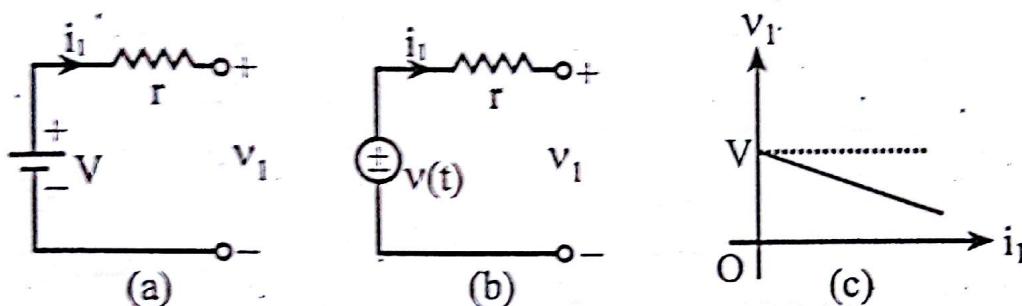


Figure 1.11 (a-b) Practical voltage source (c) It's v - i characteristic

2. The current source

The current source is assumed to deliver energy through its terminals.

i. An ideal current source

An ideal current source is one which maintains a constant current $i(t)$ regardless of the value of the terminal voltage.

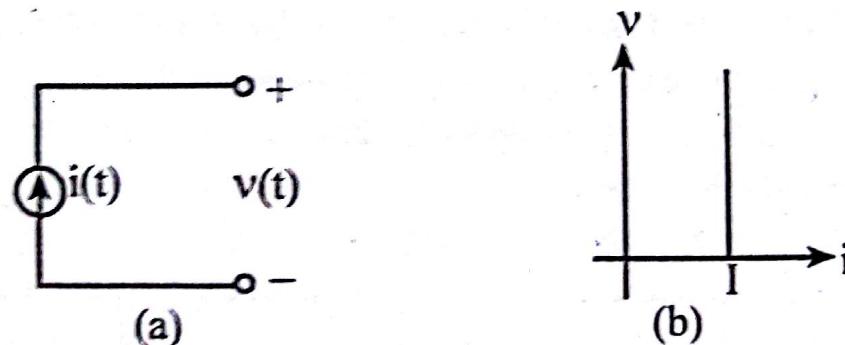


Figure 1.12 (a) Ideal current source (c) It's v - i characteristic

ii. A practical current source

A practical current source is one in which the current through the terminals of the source keeps falling as the terminal voltage across it increases. This behaviour can be explained by connecting a resistance R in parallel with an ideal current source. Then, the terminal current i_1 is :

$$i_1 = i - \frac{v_1}{R}$$

where v_1 is the terminal voltage and R the internal resistance of the ideal current source.

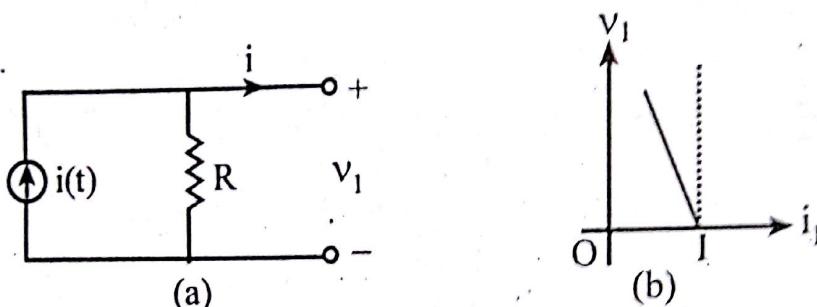


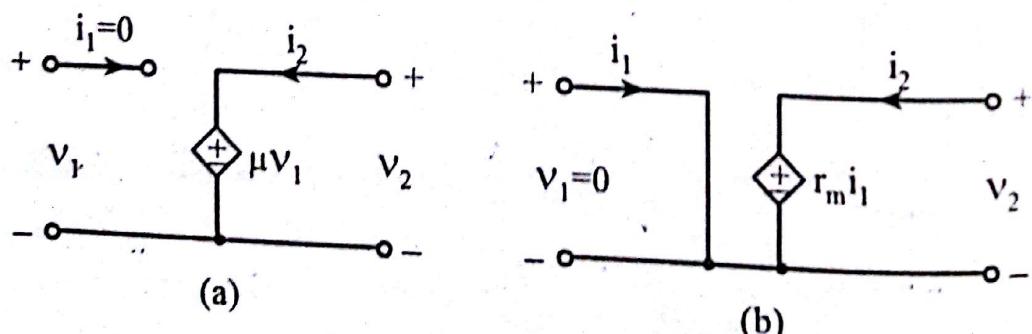
Figure 1.13 (a) Practical current source (c) Its v - i characteristic

B. Dependent or controlled sources

They are of the following types:

- i. Voltage controlled voltage source (VCVS)
- ii. Current controlled voltage source (CCVS)
- iii. Current controlled current source (CCCS)
- iv. Voltage controlled current source (VCCS)

In a dependent or controlled source, the source voltage or current (depending upon the type of source) is not constant but is dependent on a voltage or current at some other location in the network.



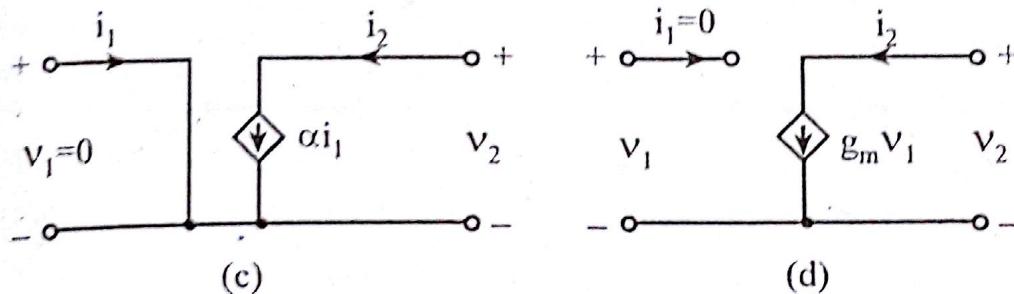


Figure 1.14 (a) VCVS (b) CCVS (c) CCCS (d) VCCS

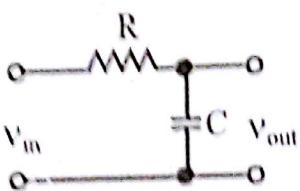
FILTERS

A filter is an electronic network which passes or allows without loss (or gain), transmission of electric signal within certain frequency range but disallows transmission of electric signal outside this frequency range. Therefore, filter is usually a frequency-selective network. Filters can be classified as passive filters and active filters. A passive filter is built with passive components such as resistors, capacitors, and inductors. An active filter is built with transistors or op-amps (providing voltage amplification, and isolation or buffering)-in addition to resistors, and capacitors.

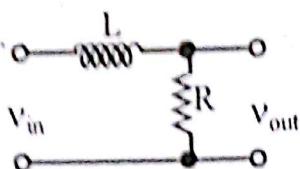
Filter may also be classified as: (i) low-pass, (ii) high-pass, (iii) band-pass (iv) band-stop, and (v) all-pass. A low-pass filter is one in which the passband extends from $f = 0$ to $f = f_c$, where f_c is known as the cutoff frequency. A high-pass filter is the complement of the low-pass filter in that the frequency range from 0 to f_c is the stopband and from f_c to infinity is the pass band. A band-pass filter is one in which the frequencies extending from f_{c1} to f_{c2} are passed, while signals at all other frequencies are stopped. A band-stop filter is the complement of the band-pass filter where signal components at the frequencies from f_{c1} to f_{c2} are stopped and all others are passed. These filters are also sometimes referred to as notch filters because of the "notch" in their transmission characteristic.

The circuit diagrams and transfer characteristics for different types of filters are illustrated by the diagrams that follow.

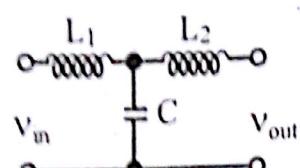
Low pass filter



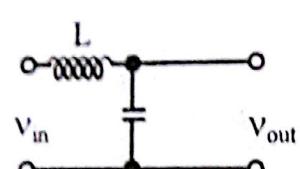
RC type



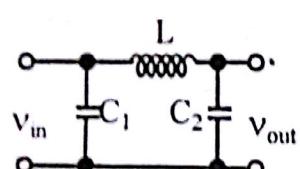
RL type



T type

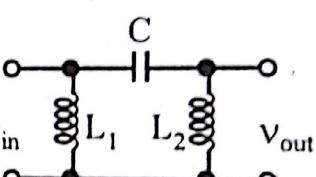
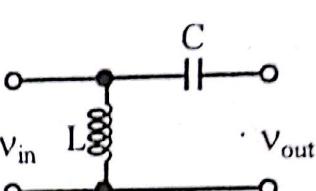
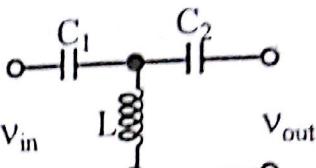
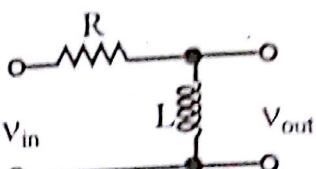
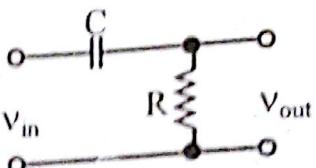


Inverted
L-type

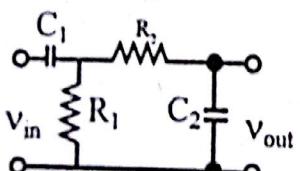


π -type

High pass filter



RC Band pass filter



RC-type

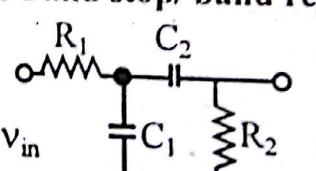
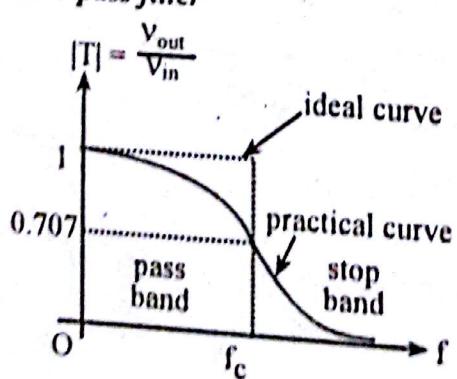
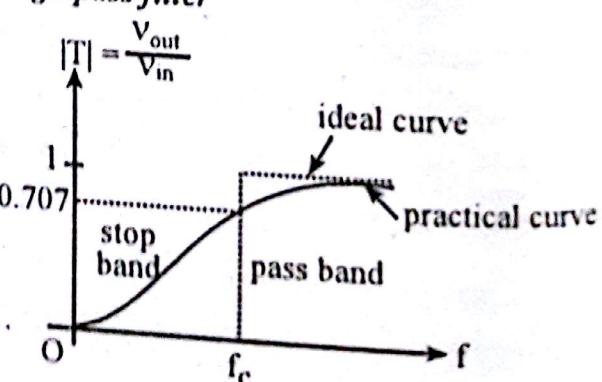


Figure 1.15 Different types of filters

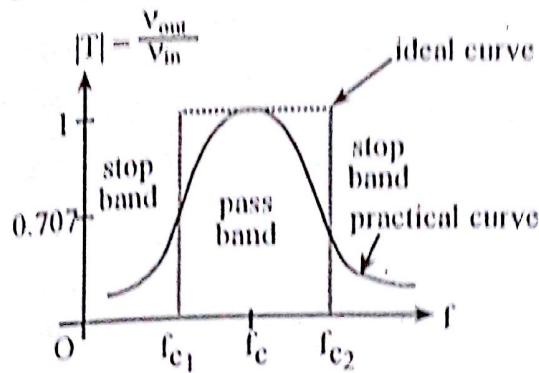
Low pass filter



High pass filter



Band pass filter



Band stop/reject/band eliminated/notch

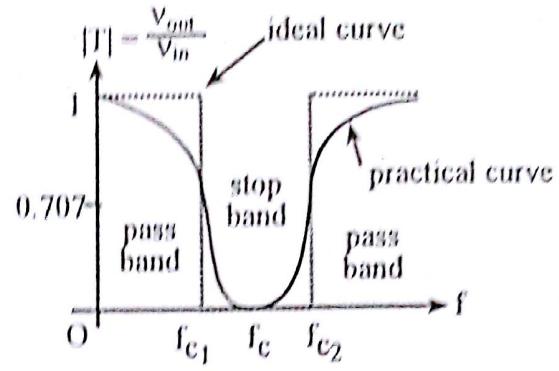
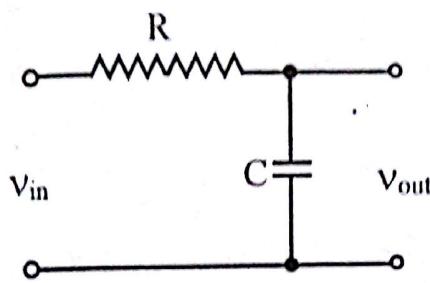
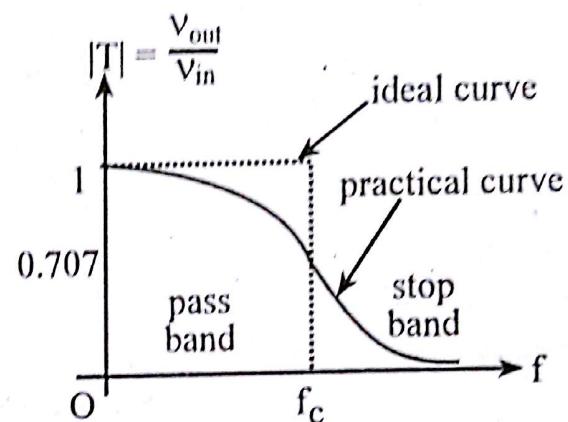


Figure 1.16 Transfer characteristics of different types of filter

RC Low-Pass Filter



(a)



(b)

Figure 1.17 (a) Circuit diagram of RC low-pass filter (b) Transfer characteristics curve

An ideal RC low-pass filter passes all signals upto a specified frequency called cut-off frequency (f_c) and rejects all signals with frequency above f_c . A practical RC low-pass filter, however exhibit the characteristics explained as follows.

In RC low-pass filter, output voltage is taken across the capacitor. The capacitive reactance is given as

$$\chi_C = \frac{1}{\omega C} = \frac{1}{2\pi f C}$$

$$\text{or, } \chi_C \propto \frac{1}{f} \text{ for } C = \text{constant}$$

At $f = 0$, $\chi_C = \infty$. This means the capacitor is replaced by an open circuit and therefore, the output voltage equals the input

voltage. As 'f' increases, the value of ' χ_C ' decreases and hence the output voltage decreases. At $f = f_c$, the output voltage equals 0.707 times the input voltage. At $f \rightarrow \infty$, $\chi_C \rightarrow 0$. This means the capacitor is replaced by a short circuit and therefore, the output voltage will be zero.

RC High-Pass Filter

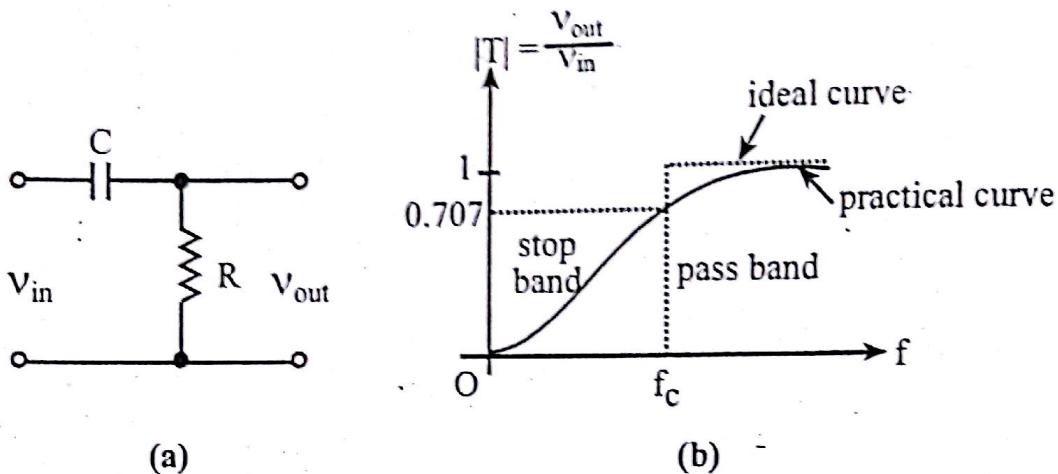


Figure 1.18 (a) Circuit diagram of RC high-pass filter (b) Transfer characteristics curve

An ideal RC high-pass filter passes all signals having frequency greater than or equal to cut-off frequency (f_c) and rejects signals with frequency below f_c . A practical high-pass filter, however exhibit the characteristics explained as follows.

In RC high-pass filter, output voltage is taken across the resistor. At $f = 0$, $\chi_C = \infty$. This means the capacitor is replaced by an open circuit. Since no current flows through R, $v_{out} = 0$. As f increases, the value of χ_C decreases and hence the output voltage increases. At $f = f_c$, the output voltage equals 0.707 times the input voltage. At $f \rightarrow \infty$, $\chi_C \rightarrow 0$. This means the capacitor is replaced by a short circuit and therefore, output voltage approaches input voltage.

CONCEPT OF GAIN, TRANSCONDUCTANCE, AND TRANSIMPEDANCE Gain

Gain is a measure of the ability of a two-port circuit (e.g. amplifier) to increase the power or amplitude of the signal

from the input to the output port. It is usually defined as the ratio of the signal amplitude or power at the output port to the amplitude or power at the input port.

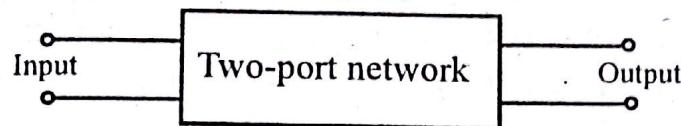


Figure 1.19 Two-port network

$$\text{Voltage gain } (A_v) = \frac{V_{\text{out}}}{V_{\text{in}}}$$

$$\text{Current gain } (A_i) = \frac{I_{\text{out}}}{I_{\text{in}}}$$

$$\text{Power gain } (A_p) = \frac{P_{\text{out}}}{P_{\text{in}}}$$

Transconductance

The word “transconductance” is the contraction of the transfer conductance. It is the ratio of the current variation at the output to the voltage variation at the input in a two-port network. Its unit is Siemens.

$$\text{Transconductance } (g_m) = \frac{\Delta I_{\text{out}}}{\Delta V_{\text{in}}}$$

Transimpedance

The word “transimpedance” is the contraction of the transfer impedance. It is the ratio of the voltage variation at the output to the current variation at the input in a two-port network. Its unit is Ohm.

$$\text{Transimpedance } (r_z) = \frac{\Delta V_{\text{out}}}{\Delta I_{\text{in}}}$$

THEVENIN'S THEOREM

This theorem may be stated as follows:

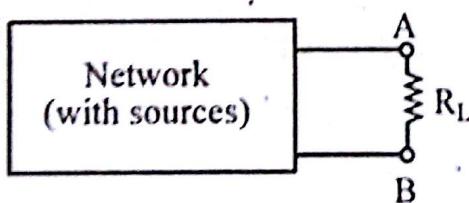
Any two terminal of a network consisting of linear, passive, and active circuit elements may be replaced by an equivalent voltage source (V_{Th}) and an equivalent series resistance (R_{Th}). The equivalent voltage source, V_{Th} is equal to the potential difference measured between the two terminal points with no external element connected to these terminals. The series resistance, R_{Th} is

the equivalent resistance looking into the network from the two terminal points, with all sources within the network made inactive. The voltage source is made inactive by replacing it with a short circuit leaving behind its internal resistance (if any) and the current source is made inactive by replacing it with an open circuit (infinite resistance).

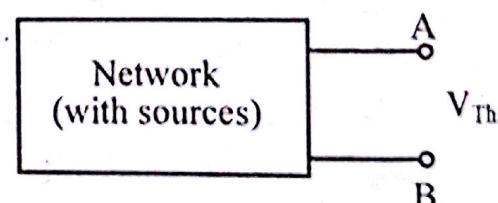
Procedure to thevenize a circuit:

1. Temporarily remove the resistance (called load resistance, R_L) whose current is required.
2. Find the open-circuit voltage, V_{Th} which appears across the two terminals from where resistance has been removed.
3. Calculate the resistance, R_{Th} of the whole network as looked into from these two terminals after all voltage sources have been removed leaving behind their internal resistances (if any) and current sources have been replaced by open circuit (infinite resistance).
4. Replace the entire network by a voltage source, V_{Th} with a series resistance, R_{Th} . Then, connect R_L back to its terminals (A-B) from where it was previously removed.
5. Finally, calculate the current flowing through R_L as

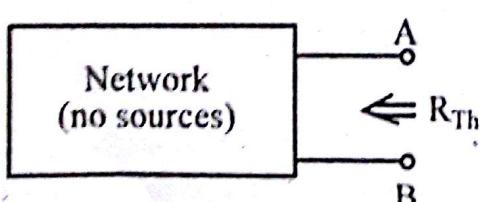
$$I = \frac{V_{Th}}{R_{Th} + R_L}$$



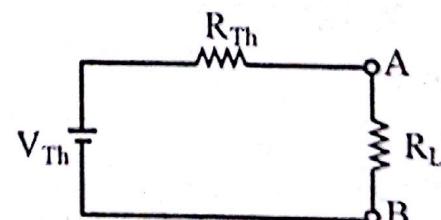
Orginal circuit



Calculation of V_{Th}



Calculation of R_{Th}



Thevenin's equivalent circuit

Figure 1.20 Illustration of steps to draw Thevenin's equivalent circuit

NORTON'S THEOREM

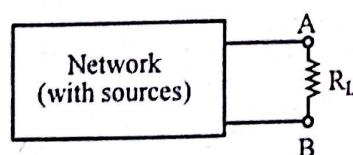
Norton's theorem may be stated as follows:

Any two terminal of a network consisting of linear, passive, and active circuit elements may be replaced by an equivalent constant-current source (I_{SC} or I_N) and an equivalent resistance in parallel (R_N). The constant current source, I_{SC} is equal to the current which would flow in a short-circuit placed across the terminals and parallel resistance, R_N is the resistance of the network when viewed from these open circuited terminals after all voltage and current sources have been removed and replaced by their internal resistances.

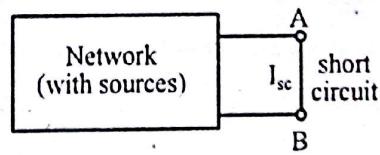
Steps to nortonize a given circuit:

1. Temporarily remove the resistance (if any) across the two given terminals and put a short circuit across them.
2. Find the short circuit current, I_{SC} .
3. Calculate the resistance, R_N of the whole network as looked into from these two terminals after all voltage sources have been removed leaving behind their internal resistances (if any) and current sources have been replaced by open circuits (infinite resistance).
4. Replace the entire network by a constant current source, I_{SC} with a resistance, R_N in parallel. Then, connect back the resistance to its terminals (A-B) from where it was previously removed.
5. Finally, calculate the current flowing through R_L as

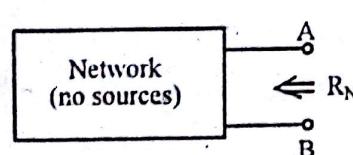
$$I = \left(\frac{R_N}{R_N + R_L} \right) I_{SC}$$



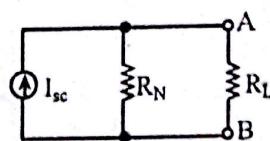
Original circuit



Calculation of I_{SC}



Calculation of R_N



Norton's equivalent circuit

Figure 1.21 Illustration of steps to draw Norton's equivalent circuit

SUPERPOSITION THEOREM

This theorem may be stated as follows:

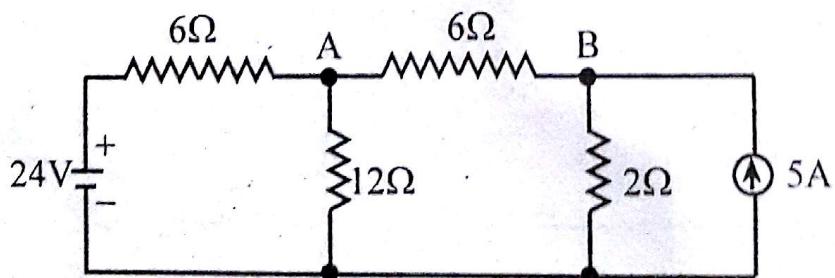
In a network of linear resistances containing more than one generator (or source of emf), the current which flows at any point is the sum of all the currents which would flow at that point if each generator were considered separately and all the other generators made inactive. For this, a voltage source is replaced with a short circuit leaving behind its internal resistance (if any) and a current source is replaced with an open circuit (infinite resistance).

Steps to apply superposition theorem:

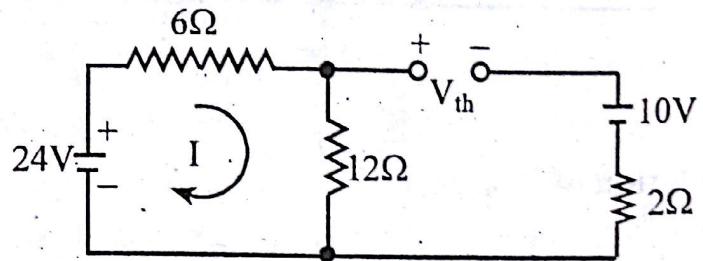
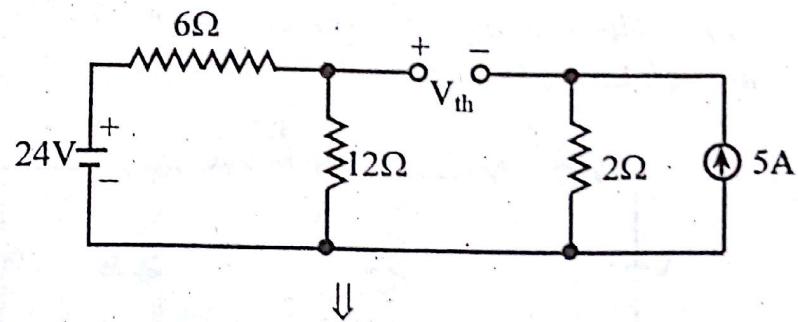
1. All sources except the one under consideration are removed. While removing the voltage sources, their internal resistances (if any) are left behind. While removing current sources, they are replaced by an open circuit since their resistance is infinite.
2. Currents in various resistors and their voltage drops due to this single source are calculated.
3. This process is repeated for other sources, taken one at a time.
4. Algebraic sum of currents and voltage drops over different circuit elements due to different sources is taken. It gives the actual values of the currents and voltage drops over different circuit elements.

Problem 1.4

Find the current flowing through the 6Ω resistor (across A&B) using Thevenin's theorem.



Solution:

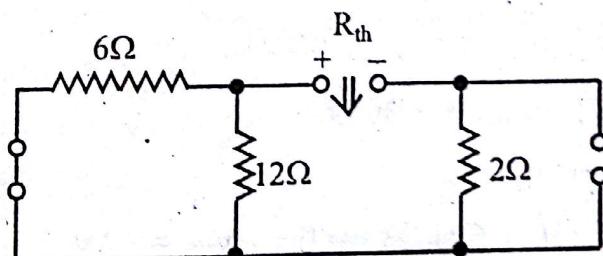


$$V = 5 \times 2 = 10V$$

$$I = \frac{24}{6+12} = \frac{24}{18} = \frac{4}{3} A$$

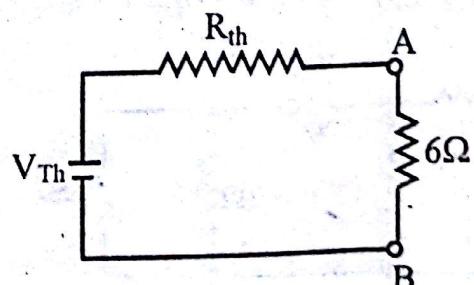
$$\text{Now, } V_{Th} = \frac{4}{3} \times 12 + 10 = 0 \Rightarrow V_{Th} = 6V$$

Calculation of R_{Th}



$$R_{Th} = (6 \parallel 12) + 2 = 4 + 2 = 6\Omega$$

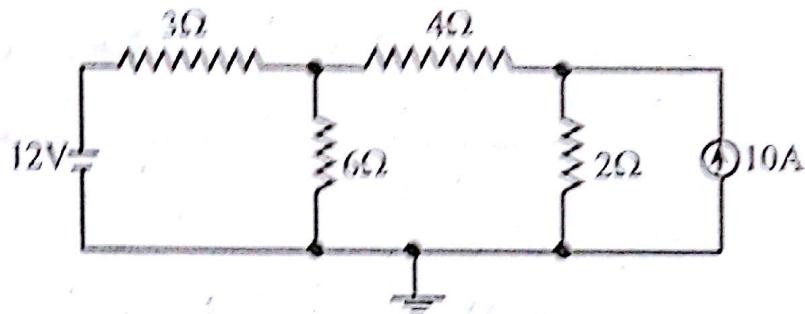
The Thevenin's equivalent circuit is



$$\therefore I_{6\Omega} = \frac{V_{Th}}{R_{Th} + 6} = \frac{6}{6+6} = 0.5 A \text{ (from A to B)}$$

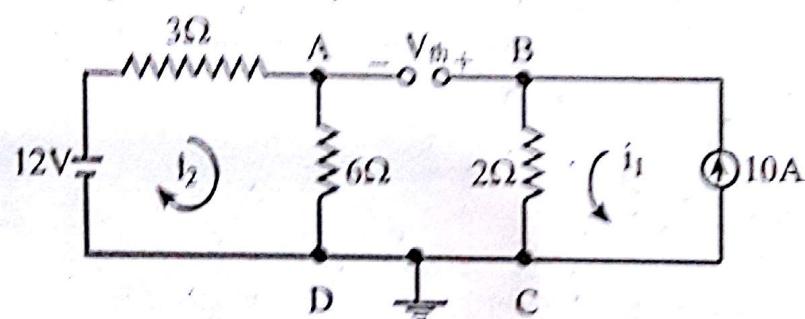
Problem 1.5

Using Thevenin's theorem, calculate the current flowing through the 4Ω resistor.



Solution:

Calculation of V_{Th}



$$i_1 = 10A$$

$$i_2 = \frac{12}{3+6} = \frac{12}{9} = 1.333A$$

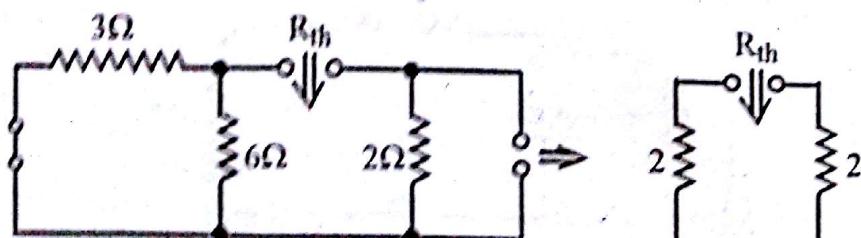
Using KVL in loop ABCD,

$$+V_{Th} - 2i_1 + 6i_2 = 0$$

$$\text{or, } V_{Th} - 2 \times 10 + 6 \times 1.333 = 0 \Rightarrow V_{Th} = 12V.$$

Calculation of R_{Th}

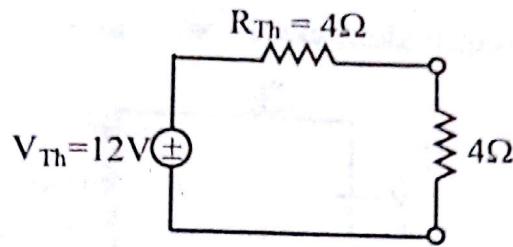
In the circuit, 12 V source and 10 A source are disabled by short-circuiting and open-circuiting respectively.



$$3 \parallel 6 = \frac{3 \times 6}{3+6} = \frac{18}{9} = 2 \Omega$$

$$R_{Th} = 2 + 2 = 4\Omega$$

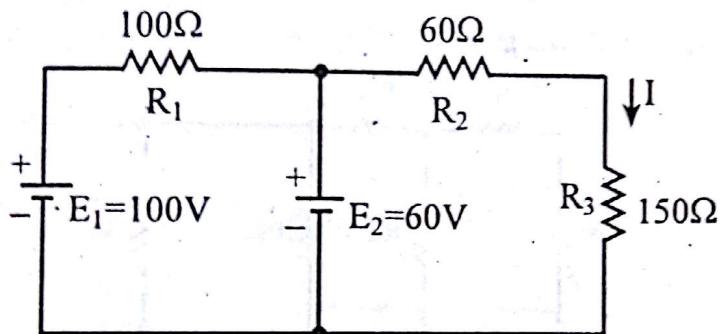
Thevenin's equivalent circuit is



$$\therefore I_{4\Omega} = \frac{V_{Th}}{R_{Th} + 4} = \frac{12}{4+4} = 1.5 \text{ A.}$$

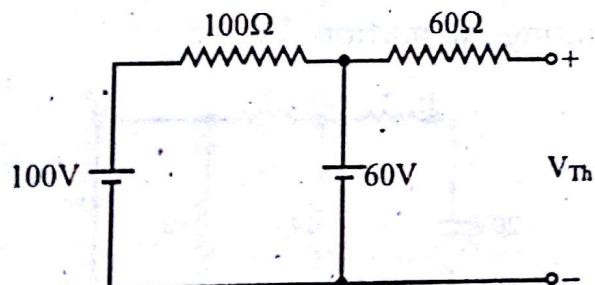
Problem 1.6

Find the current I in R_3 using Thevenin's theorem. [2069 Poush]



Solution:

Calculate of V_{Th}

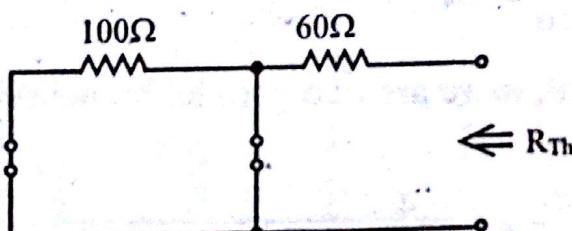


Applying KVL in right loop,

$$V_{Th} - 60 = 0 \Rightarrow V_{Th} = 60 \text{ V}$$

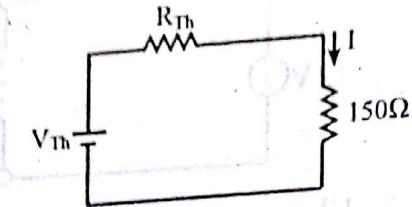
Calculation of R_{Th}

100 V and 60 V sources are replaced by short circuits.



$$R_{Th} = (100 \parallel 0) + 60 = 0 + 60 = 60 \Omega.$$

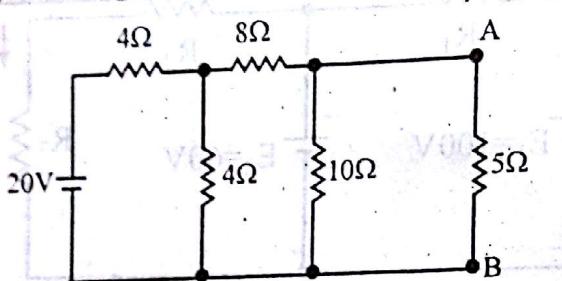
Thevenin's equivalent circuit is



$$I = \frac{V_{Th}}{R_{Th} + 150} = \frac{60}{60+150} = \frac{60}{210} = 0.285 \text{ A}$$

Problem 1.7

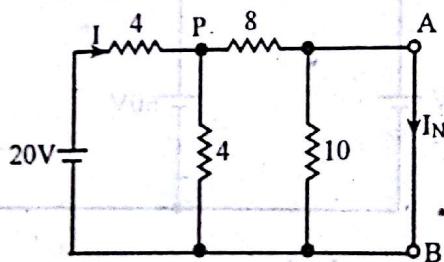
Apply Norton's theorem to calculate current flowing through 5Ω resistor for the given network.



Solution:

Calculation of I_N

Short-circuiting the portion AB,



$$10 \parallel 0 = 0 \Omega$$

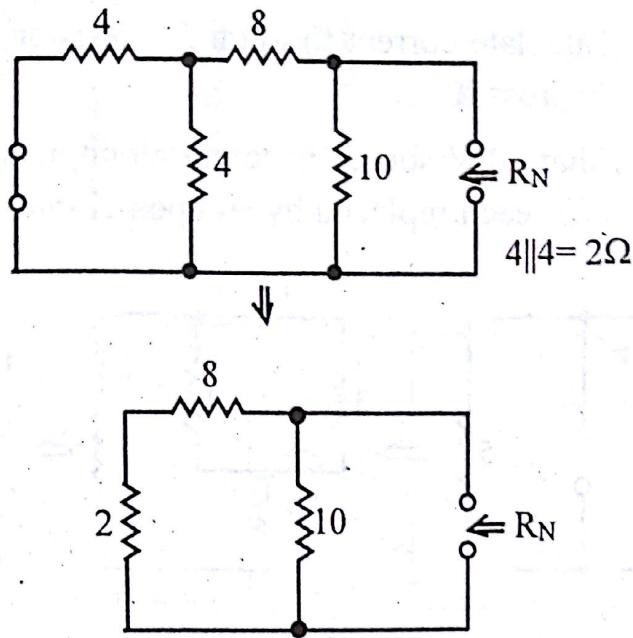
$$R_{eq} = [4 \parallel (8+0)] + 4 = (4 \parallel 8) + 4 = \left(\frac{4 \times 8}{4+8}\right) + 4 = 6.666 \Omega$$

$$\therefore I = \frac{20}{6.666} = 3 \text{ A}$$

At point P, there are two parallel branches of resistance 4Ω & 8Ω .

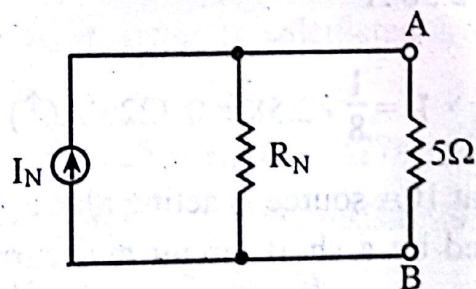
$$\therefore I_N = \frac{4}{4+8} \times I = \frac{4}{12} \times 3 = 1 \text{ A.}$$

Calculation of R_N



$$\therefore R_N = (2+8)\parallel 10 = 10\parallel 10 = 5\Omega$$

Now, the Norton's equivalent circuit is

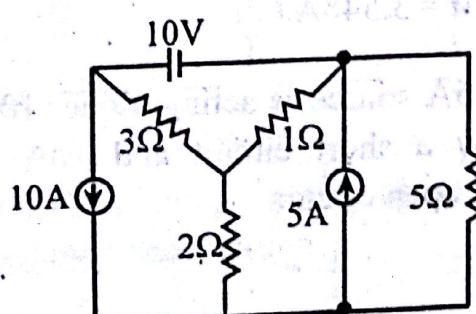


$$I_{AB} = \frac{R_N}{R_N + 5} I_N = \frac{5}{5+5} \times 1 = \frac{5}{10} \times 1 = 0.5 \text{ A}$$

Hence, current through 5Ω resistor is 0.5 A.

Problem 1.8

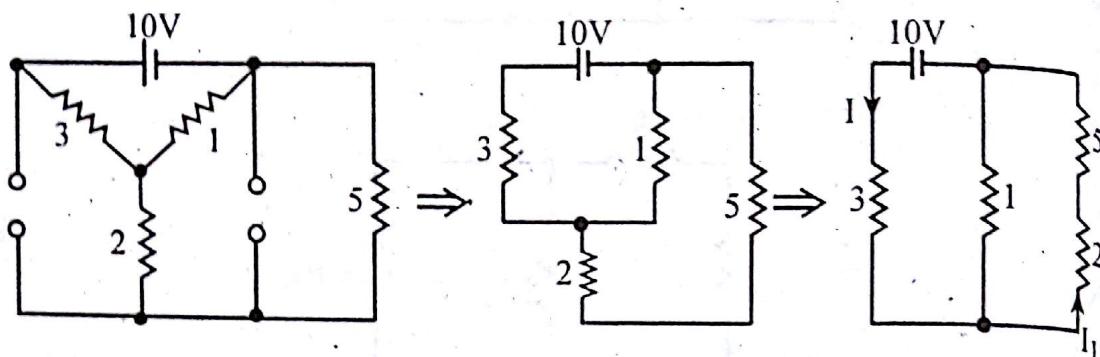
Find the power dissipated in 5Ω resistor for the given network using superposition theorem.



Solution:

First we calculate current through 5Ω resistor and then power dissipated across it.

Consider that 10 V source is acting alone. Current sources 10 A and 5A are each replaced by an open circuit.

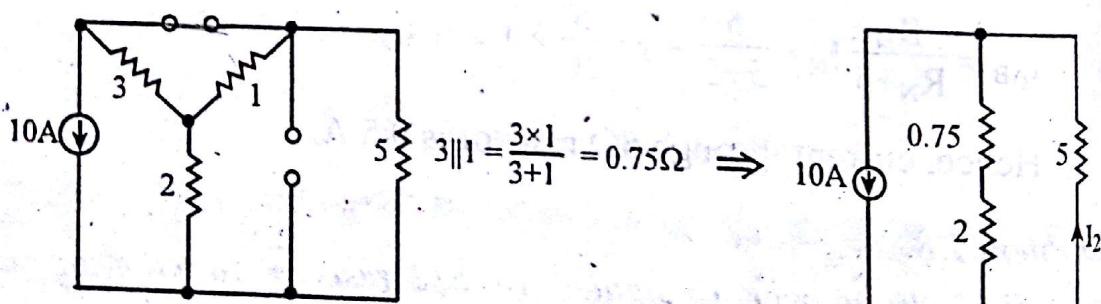


$$\therefore R_{eq} = (1 \parallel 7) + 3 = \left(\frac{1 \times 7}{1+7} \right) + 3 = 3.875 \Omega.$$

$$I = \frac{10}{3.875} = 2.58 \text{ A}$$

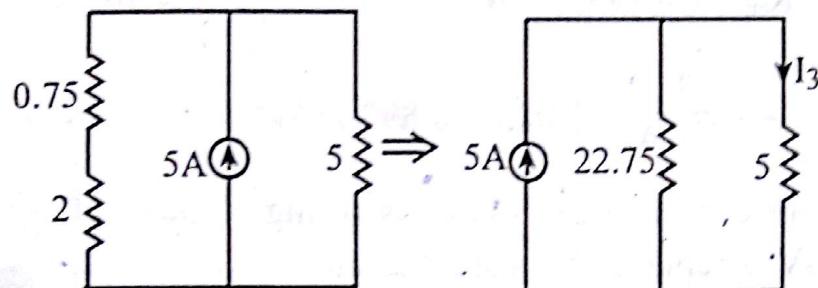
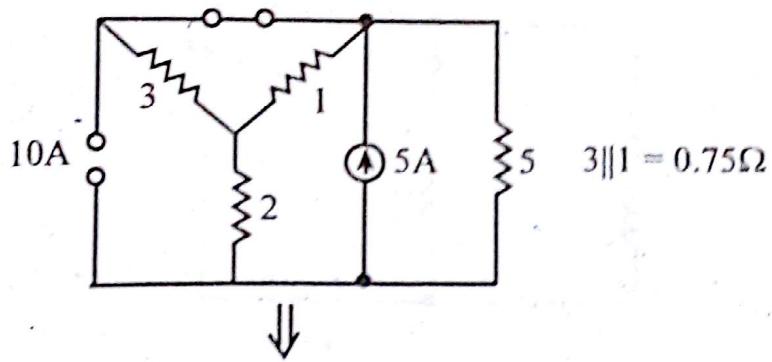
$$\therefore I_1 = \frac{1}{1+7} \times I = \frac{1}{8} \times 2.58 = 0.3225 \text{ A} (\uparrow).$$

Consider that 10A source is acting alone. Voltage source of 10 V is replaced by a short circuit and current source of 5A is replaced by an open circuit.



$$I_2 = \frac{2.75}{2.75+5} \times 10 = 3.548 \text{ A} (\uparrow)$$

Consider that 5A source is acting alone. 10 V voltage source is replaced by a short circuit and 10A current source is replaced by an open circuit.



$$I_3 = \frac{2.75}{2.75+5} \times 5 = 1.774 \text{ A } (\downarrow)$$

Now, when all the electrical sources are acting, the total current through 5Ω resistor is calculated from superposition theorem as

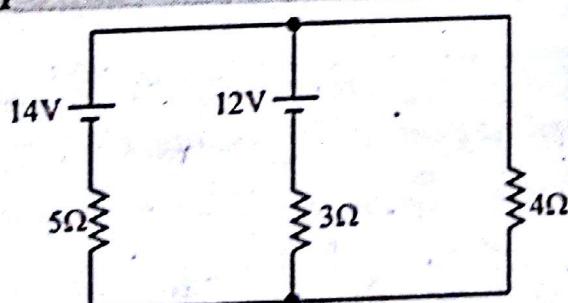
$$I_{5\Omega} = I_1 + I_2 - I_3 = 0.3225 + 3.548 - 1.774 = 2.096 \text{ A } (\uparrow)$$

Hence, power dissipated across 5Ω resistor is given as

$$P = I^2 R = (2.096)^2 \times 5 = 21.966 \text{ W}$$

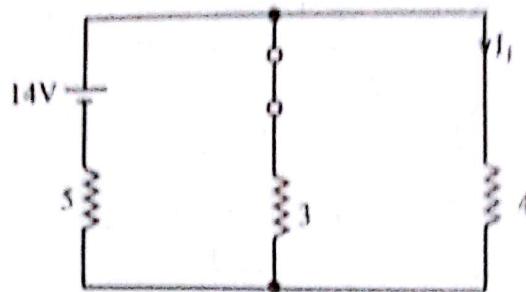
Problem 1.9

In the following figure, find the current flow in 4Ω resistor using superposition theorem. [2070 Bhadra]



Solution:

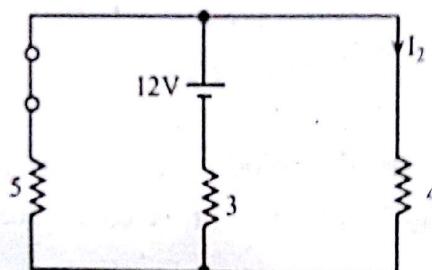
Consider that 14V source is acting alone. Voltage source of 12V is replaced by a short circuit.



$$R_{eq} = (3\parallel 4) + 5 = 6.714, \quad I = \frac{14}{6.714} = 2.085 \text{ A}$$

$$I_1 = \frac{3}{3+4} \times 2.085 = 0.893 \text{ A } (\downarrow)$$

Consider that 12V source is acting alone. Voltage source of 14V is replaced by a short circuit.



$$R_{eq} = (5\parallel 4) + 3 = 5.222, \quad I = \frac{12}{5.222} = 2.297 \text{ A}$$

$$I_2 = \frac{5}{5+4} \times 2.297 = 1.276 \text{ A } (\downarrow)$$

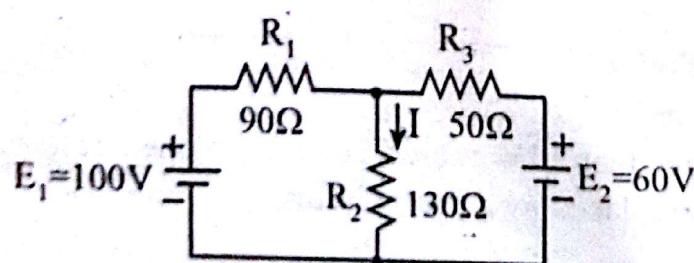
Now, when both voltage sources are acting, the total current through 4Ω resistor is calculated from superposition theorem as

$$I_{4\Omega} = I_1 + I_2 = 0.893 + 1.276 = 2.169 \text{ A } (\downarrow)$$

Problem 1.10

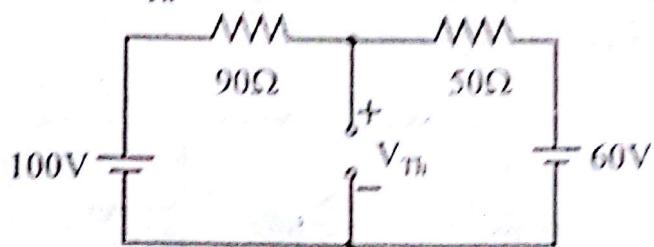
Find the current I through R_2 using Thevenin's theorem.

[2072 Magh]



Solution:

Calculation of V_{Th}



$$I_{90} = I_{50} = \frac{100 - 60}{90 + 50} = \frac{40}{140} = \frac{2}{7} \text{ A}$$

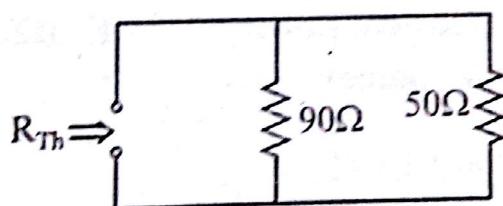
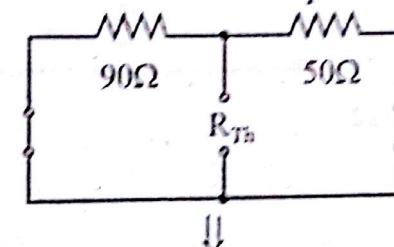
Applying KVL in right loop,

$$V_{Th} - 50 \times \frac{2}{7} - 60 = 0$$

$$\therefore V_{Th} = 74.285 \text{ V}$$

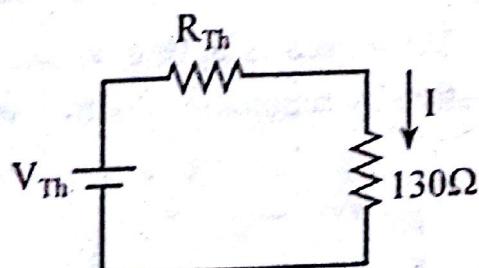
Calculation of R_{Th}

100V and 60V Sources are each replaced by short circuits.



$$R_{Th} = 90//50 = \frac{90 \times 50}{90 + 50} = 32.142 \Omega$$

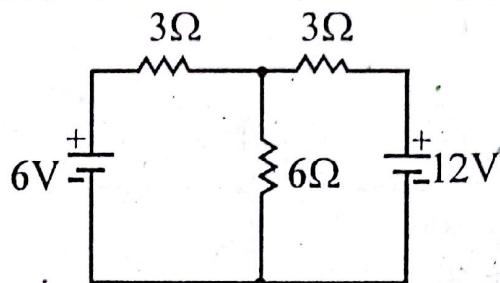
Thevenin's equivalent circuit is



$$I = \frac{V_{Th}}{R_{Th} + 130} = \frac{74.285}{32.142 + 130} = 0.458 \text{ A}$$

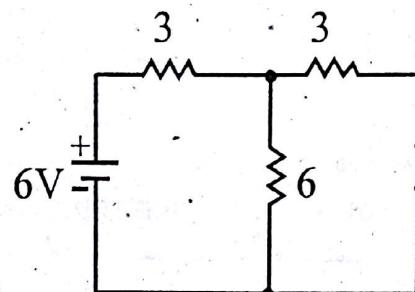
Problem 1.11

Calculate the current flowing in each branch using superposition theorem. [2073 Bhadra]



Solution:

Consider that 6V source is acting alone. Voltage source of 12V is made inactive by replacing it with a short circuit.



$$R_{eq} = (3\parallel 6) + 3 = 5\Omega$$

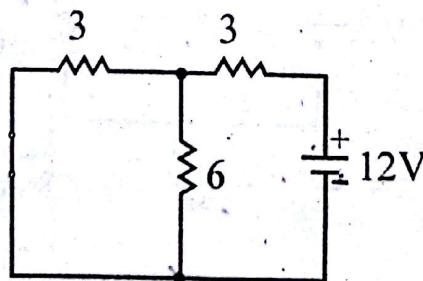
$$I = \frac{6}{5} = 1.2 \text{ A}$$

$I_{32} = 1.2 \text{ A}$ (\rightarrow) (current flowing through 3Ω resistor connected in series with 6V source)

$$I_6 = \frac{3}{3+6} \times 1.2 = 0.4 \text{ A}$$
 (\downarrow)

$I_{31} = \frac{6}{6+3} \times 1.2 = 0.8 \text{ A}$ (\rightarrow) (current flowing through 3Ω resistor connected in series with 12V source)

Consider that 12V source is acting alone. Voltage source of 6V is made inactive by replacing it with a short circuit.



$$R_{eq} = (3\parallel 6) + 3 = 5\Omega$$

$$I = \frac{12}{5} = 2.4A$$

$$I_{31} = 2.4A (\leftarrow)$$

$$I_6 = \frac{3}{3+6} \times 2.4 = 0.8A (\downarrow)$$

$$I_{32} = \frac{6}{6+3} \times 2.4 = 1.6A (\leftarrow)$$

Now, when both sources are acting, the total current through each resistor is calculated from superposition theorem as.

$$I_6 = 0.4 + 0.8 = 1.2A (\downarrow)$$

$$I_{32} = 1.6 - 1.2 = 0.4A (\leftarrow)$$

$$I_{31} = 2.4 - 0.8 = 1.6A (\leftarrow)$$

ANSWERS TO SOME QUESTIONS

1. Define transconductance, voltage gain, and current gain with reference to BJT. [2069 Bhadra]

Transconductance

It is the ratio of output current to input voltage. It decides the extent of amplification by the transistor. Its unit is mho or A/V or Siemens. Mathematically,

$$\text{Transconductance, } g_m = \frac{i_o}{v_i} \mid v_o = 0$$

$$\text{For transistor, } g_m = \frac{i_c}{v_{BE}}$$

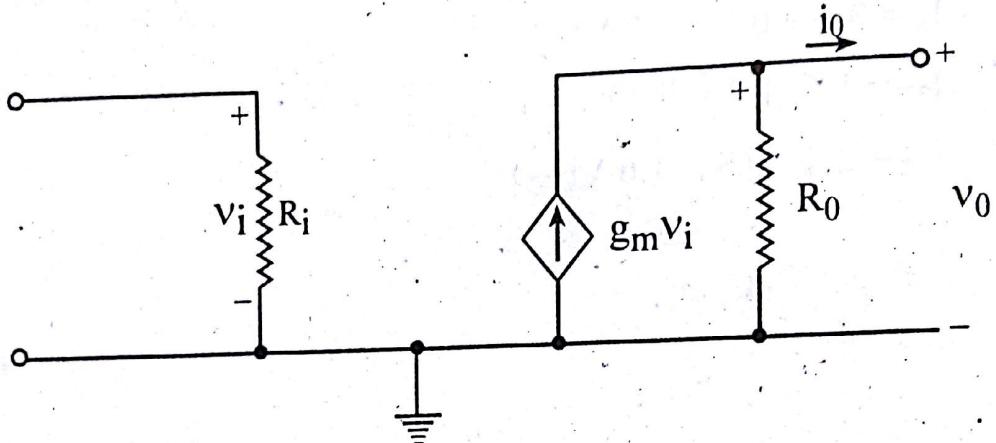


Fig.: Model of current amplifier to show transconductance

Gain

It is the ratio of output quantity to input quantity. Quantity may be voltage or current or power. It is measured in decibel (dB) or Neper.

i. Voltage gain

$$\text{Voltage gain, } A_{vo} = \frac{v_o}{v_i} \mid i_o = 0$$

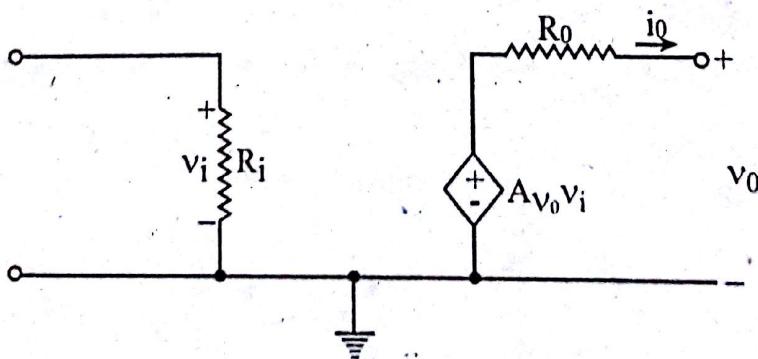


Fig.: Model of voltage amplifier to show voltage gain

For the case of CE configuration of transistor,

$$A_{vo} = \frac{V_{CE}}{V_{BE}}$$

ii. Current gain

Current gain, $A_{is} = \frac{i_o}{i_i} \mid v_o = 0$

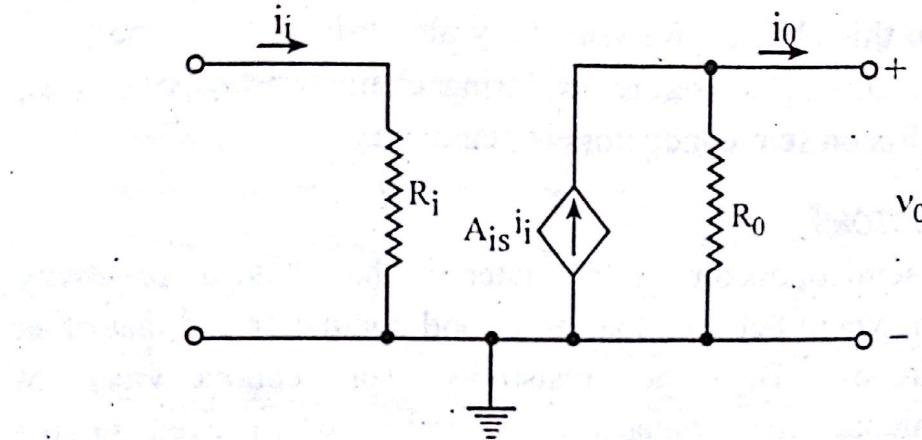


Fig.: Model of current amplifier to show current gain

For the case of CE configuration of transistor,

$$A_{is} = \frac{i_C}{i_B} = \beta$$

2. Determine the colour code of the resistor having resistance of $75 \text{ K}\Omega \pm 10\%$.

violet-green-orange-silver

Chapter - 2

DIODES

INTRODUCTION

The diode is one of the oldest, simplest, and most important semiconductor devices used in all sorts of electrical and electronic systems. In this chapter, we will study about diodes, its types, and application areas. But before exploring characteristics of diodes, deep insights on semiconductors is mandatory.

SEMICONDUCTORS

A semiconductor is a material that has a resistivity somewhere between that of a good conductor and that of an insulator. But the resistivity (or conductivity) of semiconductor changes considerably when even minute amounts of certain other substances, called the impurities, are added to them. Most semiconductor materials used in electronics industry have negative temperature coefficients. Examples of semiconductor materials include silicon (Si), germanium (Ge), gallium arsenide (GaAs), and indium arsenide (InAs).

Pure semiconductor material is known as intrinsic material. Before intrinsic material can be used in the manufacture of a device, impurity atoms must be added to improve its conductivity. The process of adding the atoms is termed doping. Two different types of doping are possible: donor doping and acceptor doping. Donor doping generates free electrons in the conduction band. Acceptor doping produces valence-band holes, or a shortage of valence electrons in the material. After doping, the semiconductor material is known as extrinsic material.

Donor-doped semiconductor is known as n-type semiconductor and acceptor-doped semiconductor is known as p-type semiconductor. Typical donor atoms (also known as pentavalent atoms) are antimony, phosphorus, and

arsenic. Typical acceptor atoms (also known as trivalent atoms) are boron, aluminum, and gallium.

In n-type semiconductor, electrons are the majority charge carriers and holes are the minority charge carriers. Whereas in p-type semiconductor, holes are the majority charge carriers and electrons are the minority charge carriers.

A Silicon Atom

If we look at an isolated silicon atom, it contains four electrons in its valence shell. When atoms combine to form a solid crystal, each atom positions itself between four other silicon atoms in such a way that the valence shells overlap from one atom to another. This causes each individual valence electron to be shared by two atoms as shown in **Figure 2.1**. By sharing the electrons between four adjacent atoms, each individual silicon atom appears to have eight electrons in its valence shell. This sharing of valence electrons is called covalent bonding.

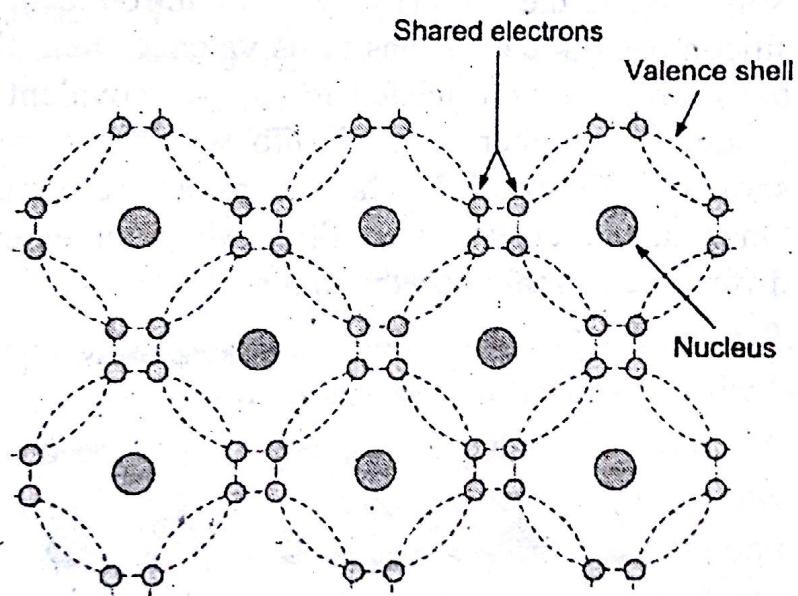


Figure 2.1 Lattice showing covalent bonding

In its pure state, silicon is an insulator because the covalent bonding rigidly holds all of the electrons leaving no free (easily loosened) electrons to conduct current. If, however, an atom of a different element (i.e., an impurity) is introduced that has five electrons in its valence shell, a

surplus electron will be present, as shown in **Figure 2.2**. These free electrons become available for use as charge carriers and they can be made to move through the lattice by applying an external potential difference to the materials.

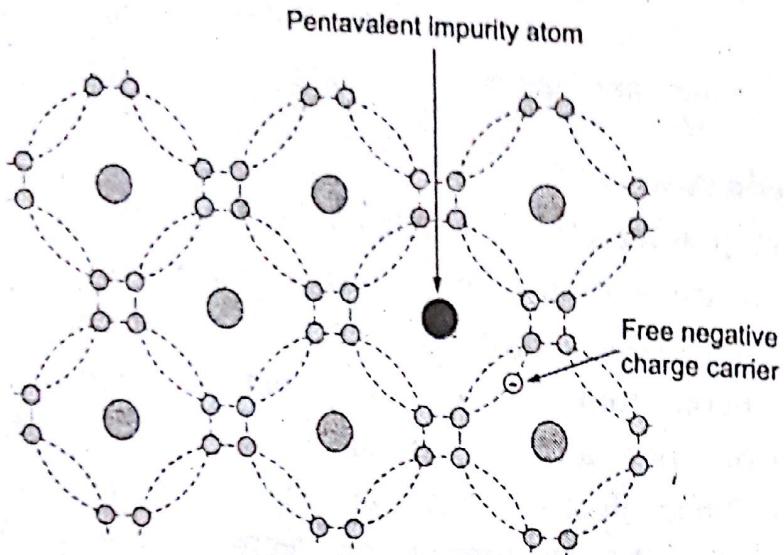


Figure 2.2 Free negative charge carriers (electrons) produced by introducing a pentavalent impurity

Similarly, if the impurity element introduced into the pure silicon has three electrons in its valence shell, the absence of the fourth electron needed for proper covalent bonding will produce a number of gaps into which electrons can fit as shown in **Figure 2.3**. These gaps are referred to as holes. Once again, current will flow when an external potential difference is applied to the material.

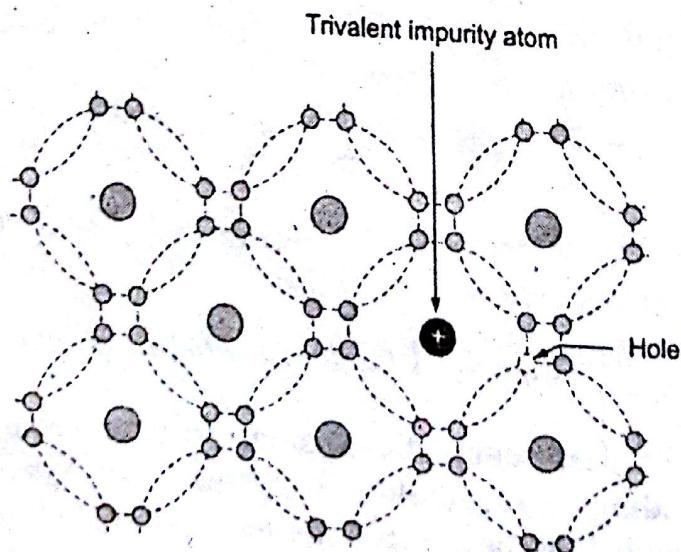


Figure 2.3 Holes produced by introducing a trivalent impurity

Why Semiconductors?

The devices (such as diodes, transistors, etc.) manufactured from semiconductors have many advantages such as compact size, low cost, light weight, rugged construction, more resistive to shocks and vibrations, instantaneous operation (no heating required), low operating voltage, high operating efficiency (no heat loss), and long life with essentially no ageing effect if operated with permissible limits of temperature and frequency. Detailed description of these devices are given in the subsequent topics.

DIODES

The term "diode" refers to a two-electrode, or two-terminal device. Put simply, a diode is a one-way device, offering a low resistance when forward-biased, and behaving almost as an open switch when reverse biased.

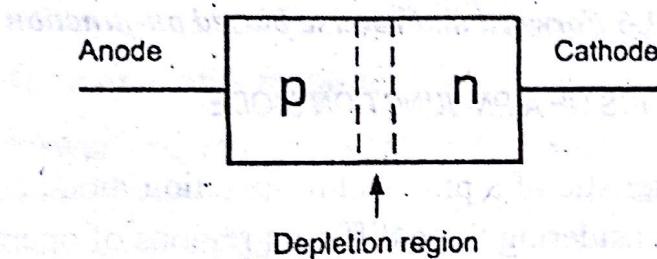


Figure 2.4 A pn-junction diode

A semiconductor junction diode is shown in Figure 2.4. The connection to the p-type material is referred to as the "anode" while that to the n-type material is called the "cathode". With no externally applied potential, electrons from the n-type material will cross into the p-type region and fill some of the vacant holes. This action will result in the production of a region either side of the junction in which there are no free charge carriers. This zone is known as the "depletion region".



Figure 2.5 Diode circuit symbol

Figure 2.6 shows a junction diode in which the anode is made positive with respect to the cathode. This is forward-biased condition in which the diode freely passes current. It also shows a diode with the cathode made positive with respect to the anode. This is reverse-biased condition in which the diode passes a negligible amount of current.

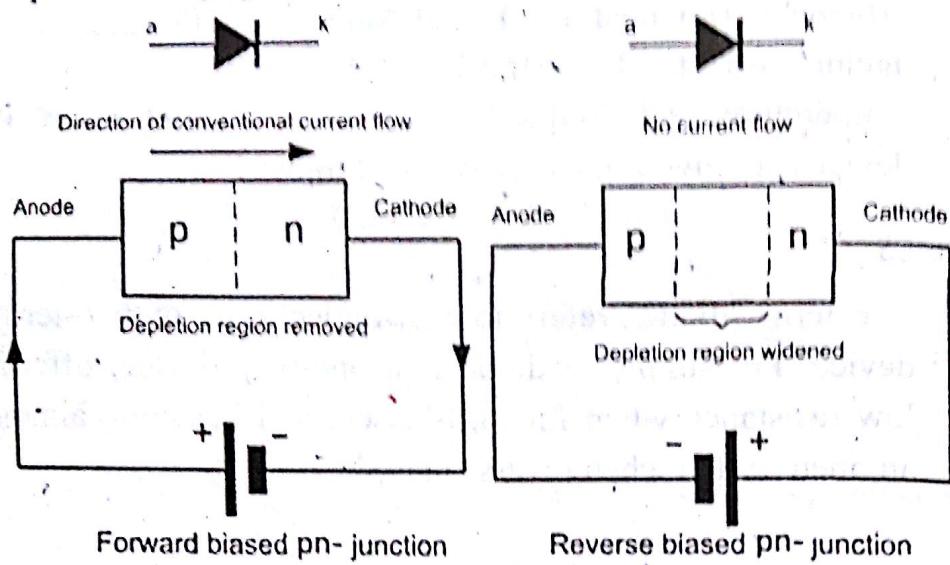


Figure 2.6 Forward and reverse biased pn-junction

I-V CHARACTERISTICS OF A PN-JUNCTION DIODE

The i-v characteristic of a practical pn-junction diode can be best explained by considering three different regions of operation.

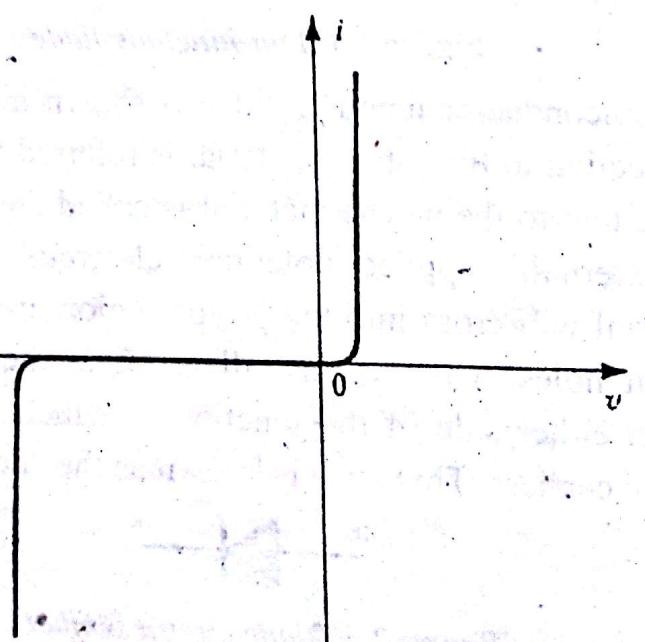


Figure 2.7 The i-v characteristics of a practical silicon junction diode

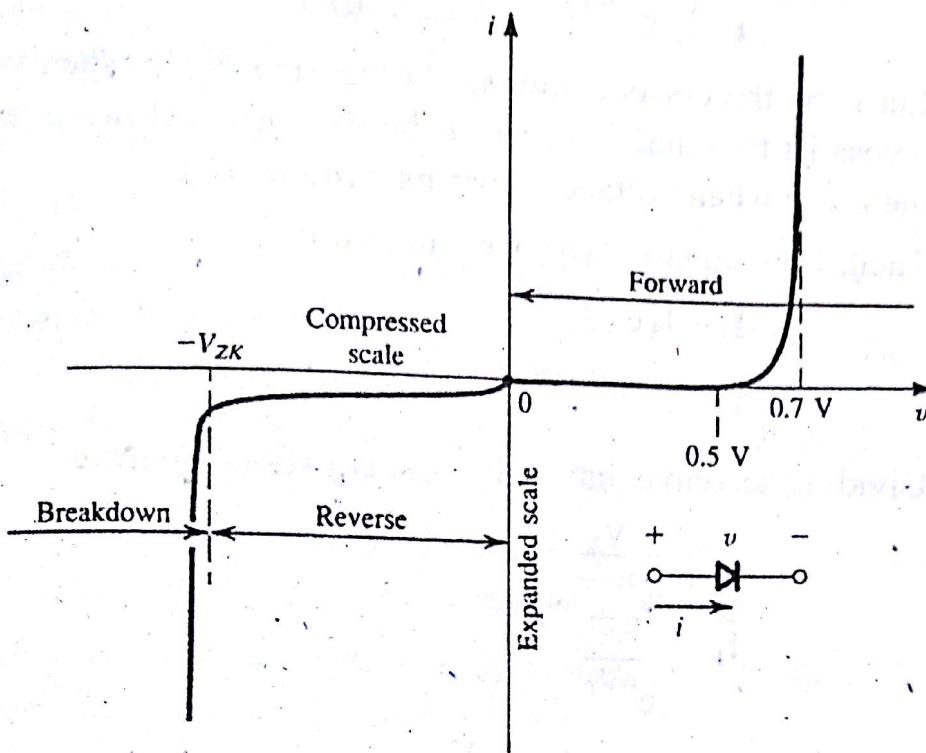


Figure 2.8 The $i-v$ relationship of a practical silicon junction diode with some scale expanded and others compressed in order to reveal details

i. The forward-bias region:

The forward region of operation is entered when the terminal voltage v is positive. In the forward region, the $i-v$ relationship is closely approximated by

$$i = I_S (e^{v/nV_T} - 1) \quad (i)$$

where I_S = A constant for a given diode at a given temperature known as saturation current or scale current.

$$V_T = \frac{KT}{q} = \text{thermal voltage}$$

where K = Boltzmann's constant

T = the absolute temperature in kelvins

q = the magnitude of electronic charge

n = a constant depends on the material and the physical structure of the diode.

For appreciable current i in the forward direction, specially for $i \gg I_S$, equation (i) can be approximated as

$$i = I_S e^{v/nV_T} \dots \dots \dots \text{(ii)}$$

Let I_1 be the current flowing through the diode when voltage across its terminal is V_1 and I_2 be the current flowing through the diode when voltage across its terminal is V_2 .

Then, from equation (ii), we can write

$$I_1 = I_S e^{V_1/nV_T}$$

$$I_2 = I_S e^{V_2/nV_T}$$

Dividing second equation by first equation, we have

$$\frac{I_2}{I_1} = \frac{e^{\frac{V_2}{nV_T}}}{e^{\frac{V_1}{nV_T}}}$$

$$\text{or, } \frac{I_2}{I_1} = e^{\frac{V_2}{nV_T} - \frac{V_1}{nV_T}}$$

$$\text{or, } \frac{I_2}{I_1} = e^{\frac{V_2 - V_1}{nV_T}}$$

Taking natural logarithm on both sides,

$$\ln \frac{I_2}{I_1} = \frac{V_2 - V_1}{nV_T}$$

$$\text{or, } V_2 = V_1 + nV_T \ln \frac{I_2}{I_1}$$

$$\therefore V_2 = V_1 + 2.3 nV_T \log \frac{I_2}{I_1}$$

A glance at the i-v characteristics in the forward region reveals that the current is negligibly small for v smaller than about 0.5 V. This value is usually referred to as the cut-in voltage. But for a "fully-conducting" diode, the voltage drop lies in a narrow range, approximately 0.6 V to 0.8 V.

ii. The reverse-bias region:

The reverse-bias region of operation is entered when the diode voltage v is made negative. Equation (i) predicts that if v is negative and a few times larger than V_T (25 mV) in

magnitude, the exponential term becomes negligibly small compared to unity, and the diode current becomes

$$i \approx -I_S$$

iii. The breakdown region:

The third distinct region of diode operation is the breakdown region, which can be easily identified on the diode $i-v$ characteristic (see Figure 2.8). The breakdown region is entered when the magnitude of the reverse voltage exceeds a threshold value that is specific to the particular diode, called the "breakdown voltage". This is the voltage at the "knee" of the $i-v$ curve in and is denoted V_{ZK} , where the subscript Z stands for Zener and K denotes knee.

An ideal diode on the other hand would exhibit the nature as demonstrated by the graph that follows.

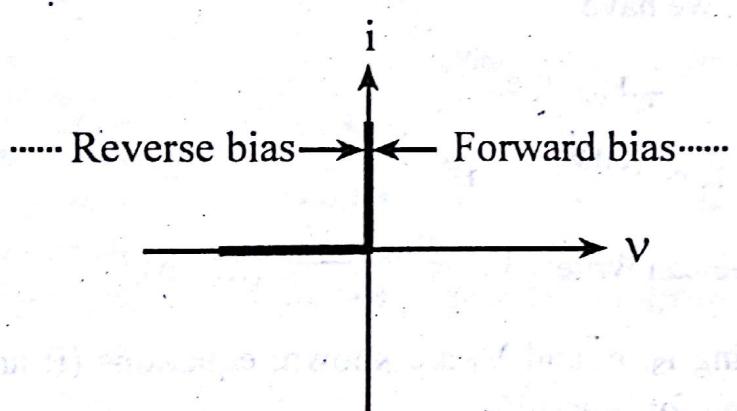


Figure 2.9 $i-v$ characteristics of an ideal diode

MODELING THE SEMICONDUCTOR DIODE FORWARD CHARACTERISTIC

The representation of any device with equivalent electric elements such as resistors, capacitors, inductors, voltage/current sources, etc. is called modeling and the circuit representation of any device with equivalent electric elements without the loss of its exact functional behavior is called "model of the device".

i. The Exponential Model

The most accurate description of the diode operation in the forward region is provided by the exponential model.

However, its severely nonlinear nature makes this model the most difficult to use.

Graphical analysis of diode circuit using the exponential model:

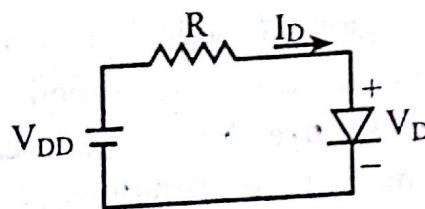


Figure 2.10 A simple circuit used to illustrate the analysis of circuits in which the diode is forward conducting

The circuit consists of a DC source V_{DD} , a resistor R , the diode voltage V_D , and current I_D .

Representing the diode $i-v$ characteristic by the exponential relation, we have

$$i = I_S (e^{v/nV_T} - 1) \approx I_S e^{v/nV_T}$$

$$\text{or, } I_D = I_S e^{V_D/nV_T} \dots \text{(i)}$$

$$\text{Also, we can write: } I_D = \frac{V_{DD} - V_D}{R} \dots \text{(ii)}$$

Assuming I_S , n , and V_T are known, equations (i) and (ii) can be solved for I_D and V_D .

Graphical method is one of the methods to determine I_D and V_D .

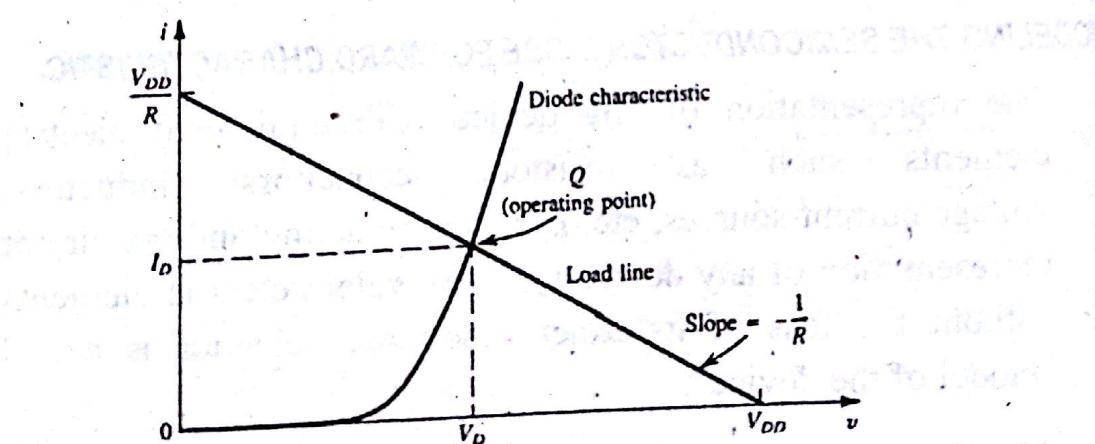


Figure 2.11 Graphical analysis of the circuit using the exponential diode model

Graphical analysis is performed by plotting the relationships of equations (i) and (ii). The solution is the coordinates of the point of intersection of the two graphs. The curve represents equation (i), and the straight line represents equation (ii). Such a straight line is known as the "load line". The load line intersects the diode curve at point Q, which represents the "operating point" of the circuit. Its coordinates give the values of I_D and V_D . Graphical analysis aids in the visualization of circuit operation.

Iterative analysis using the exponential model:

The two equations, namely

$$I_D = I_S e^{V_D/nV_T}, \quad I_D = \frac{V_{DD} - V_D}{R}$$

can be solved using a simple iterative procedure, as illustrated below.

Problem 2.1

Determine the current I_D and the diode voltage V_D for the circuit with $V_{DD} = 5V$ and $R = 1k\Omega$. Assume that the diode has a current of $1mA$ at a voltage of $0.7V$ and that its voltage drop changes by $0.1V$ for every decade change in current.

Solution:

$$I_D = \frac{V_{DD} - V_D}{R} = \frac{5 - 0.7}{1 \times 10^3} = 4.3 \text{ mA}$$

For better estimation of V_D , we use

$$V_2 - V_1 = 2.3 nV_T \log \frac{I_2}{I_1} \dots\dots (i)$$

$$\text{Given, } V_2 - V_1 = 0.1 \text{ V for } \frac{I_2}{I_1} = 10$$

$$\therefore 2.3 nV_T = 0.1$$

Using equation (i),

$$V_2 = V_1 + 2.3 nV_T \log \frac{I_2}{I_1}$$

Taking $V_1 = 0.7 \text{ V}$, $I_1 = 1 \text{ mA}$, and $I_2 = 4.3 \text{ mA}$, we get

$$V_2 = 0.7 + 0.1 \log \frac{4.3}{1} = 0.763 \text{ V}$$

Thus, the results of the first iteration are

$$I_D = 4.3 \text{ mA and } V_D = 0.763 \text{ V.}$$

The second iteration yields

$$I_D = \frac{V_{DD} - V_D}{R} = \frac{5 - 0.763}{1 \times 10^3} = 4.237 \text{ mA.}$$

$$V_2 = V_1 + 2.3 \text{ n } V_T \log \frac{I_2}{I_1} = 0.763 + 0.1 \log \frac{4.237}{4.3} = 0.762 \text{ V}$$

Thus, the second iteration yields $I_D = 4.23 \text{ mA}$ and $V_D = 0.762 \text{ V}$. Since these values are not much different from the values obtained after the first iteration, no further iterations are necessary, and the solution is $I_D = 4.237 \text{ mA}$ and $V_D = 0.762 \text{ V}$.

ii. The Piecewise -Linear Model

The straight-lines (or piecewise-linear) model can be described by

$$i_D = 0, v_D \leq V_{DO} \dots \dots \text{(i)}$$

$$i_D = (v_D - V_{DO})/r_D, v_D \geq V_{DO} \dots \dots \text{(ii)}$$

where V_{DO} is the intercept of line B on the voltage axis and r_D is the inverse of the slope of line B. The piecewise-linear model is depicted in the graph shown below.

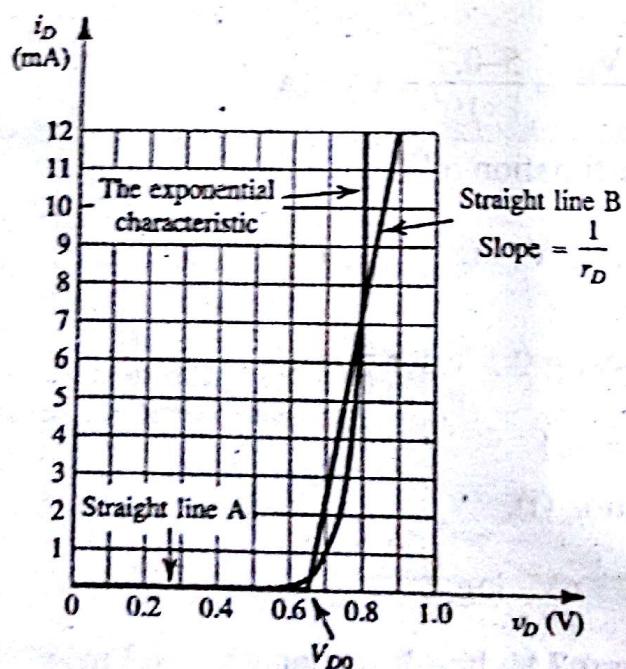


Figure 2.12 Approximating the diode forward characteristic with two straight lines: the piecewise-linear model

The piecewise-linear model described by equations (i) and (ii) can be represented by the equivalent circuit shown in Figure 2.13 below. Note that an ideal diode is included in this model to constrain i_D to flow in the forward direction only. This model is also known as the battery-plus-resistance model.

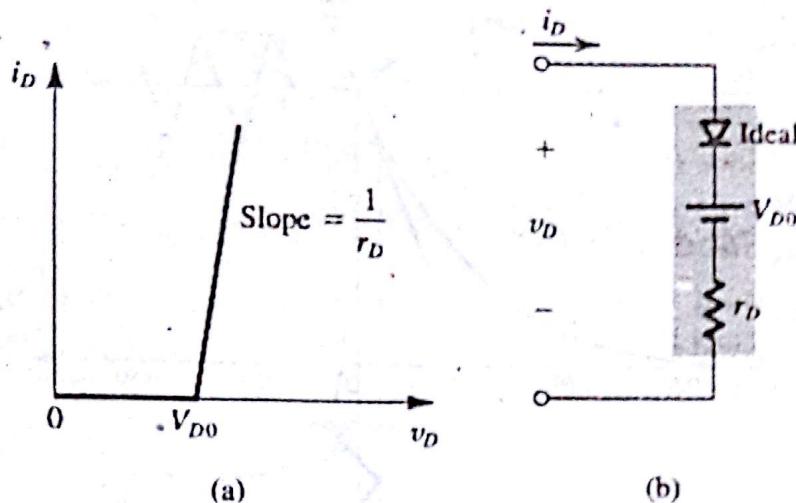


Figure 2.13 Piecewise-linear model of the diode forward characteristic and its equivalent circuit representation

iii. The Small-Signal Model

There are applications in which a diode is biased to operate at a point on the forward i - v characteristic and a small AC signal is superimposed on the DC quantities. For this situation, we first have to determine the DC operating point (V_D and I_D) of the diode. Then, for small-signal operation around the DC bias point, the diode is best modeled by a resistance equal to the inverse of the slope of the tangent to the exponential i - v characteristic at the bias point.

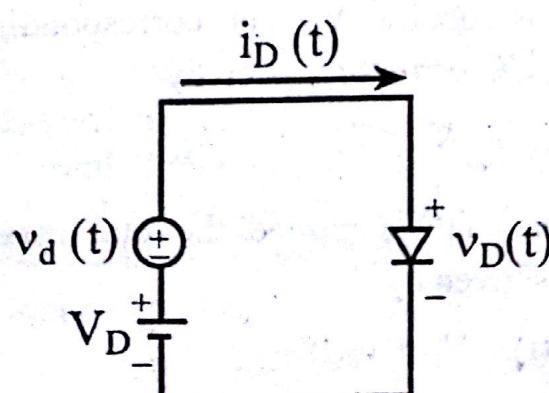


Figure 2.14 Circuit for developing the small-signal model of a diode

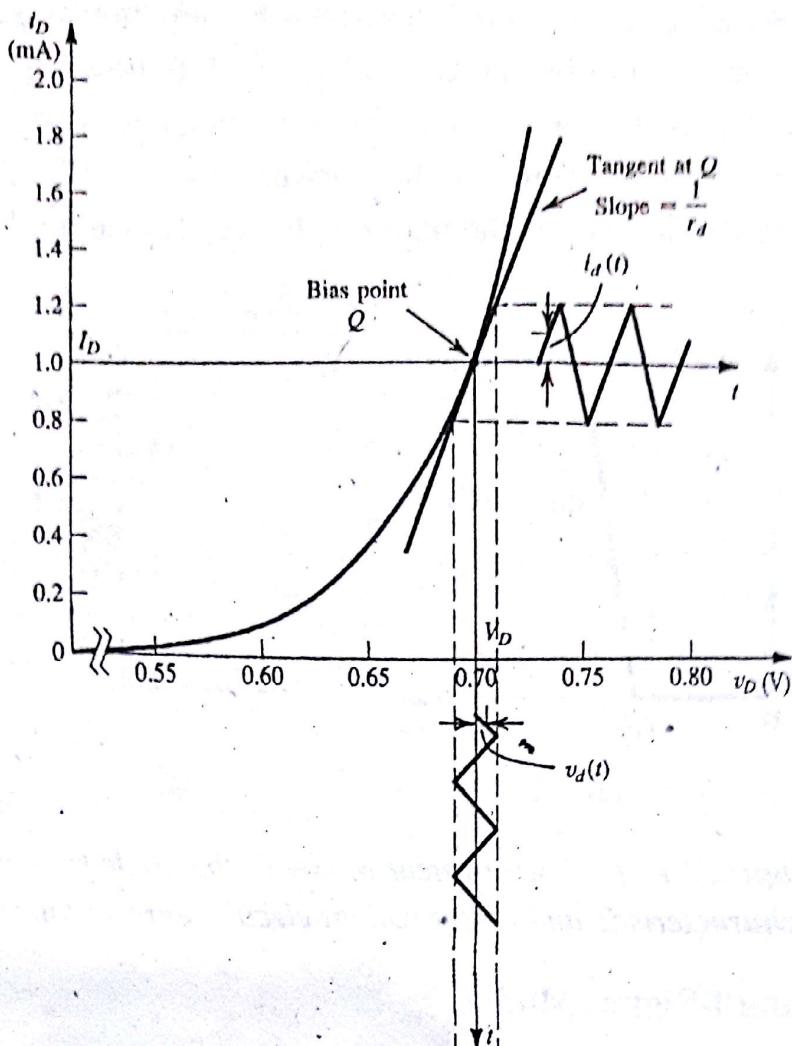


Figure 2.15 i_D - v_D characteristics curve

Consider the conceptual circuit as shown in Figure 2.14 and the corresponding graphical representation as shown in Figure 2.15. A DC voltage V_D , represented by a battery, is applied to the diode, and a time-varying signal $v_d(t)$, assumed (arbitrarily) to have a triangular waveform, is superimposed on the DC voltage V_D . In the absence of the signal $v_d(t)$, the diode voltage is equal to V_D , and correspondingly, the diode will conduct a DC current I_D given by

$$I_D = I_S e^{V_D/nV_T} \dots\dots (i)$$

When the signal $v_d(t)$ is applied, the total instantaneous diode voltage $v_D(t)$ is given by

$$v_D(t) = V_D + v_d(t)$$

Correspondingly, the total instantaneous diode current $i_D(t)$ will be

$$i_D(t) = I_S e^{V_D/nV_T}$$

$$\text{or, } i_D(t) = I_S e^{\frac{V_D + v_d}{nV_T}}$$

$$\text{or, } i_D(t) = I_S e^{V_D/nV_T} e^{v_d/nV_T}$$

Using equation (i), we get

$$i_D(t) = I_D e^{v_d/nV_T} \dots \text{(ii)}$$

Now, if the amplitude of the signal $v_d(t)$ is kept sufficiently small such that

$$\frac{v_d}{nV_T} \ll 1$$

then, we may expand equation (ii) in a series and truncate the series after the first two terms to get

$$i_D(t) \approx I_D \left(1 + \frac{v_d}{nV_T} \right).$$

This is the "small-signal approximation." It is valid for signals whose amplitudes are smaller than about 10 mV for $n=2$ and 5 mV for $n=1$.

$$\text{or, } I_D + i_d = I_D + \frac{I_D}{nV_T} v_d$$

Comparing like terms, we get

$$i_d = \frac{I_D}{nV_T} v_d$$

The quantity relating the signal current i_d to the signal voltage v_d has the dimensions of conductance, mhos (Ω), and is called the "diode small-signal conductance". The inverse of this parameter is the "diode small-signal resistance," or "incremental resistance", or "AC resistance", or "dynamic resistance" denoted by r_d .

$$r_d = \frac{nV_T}{I_D}$$

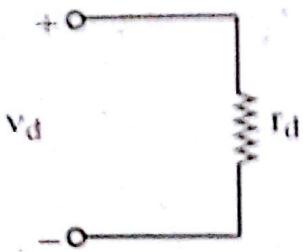


Figure 2.16 Small signal model of a diode

DIODE CIRCUITS

Clampers

Clampers are diode networks that will "clamp" a signal to a different dc level. The network must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen such that the time constant $\tau = RC$ is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is non conducting. There are two basic types of clampers:

i. Positive clamer

A positive clamer shifts its input waveform in a positive direction, so that it lies above a dc reference voltage.

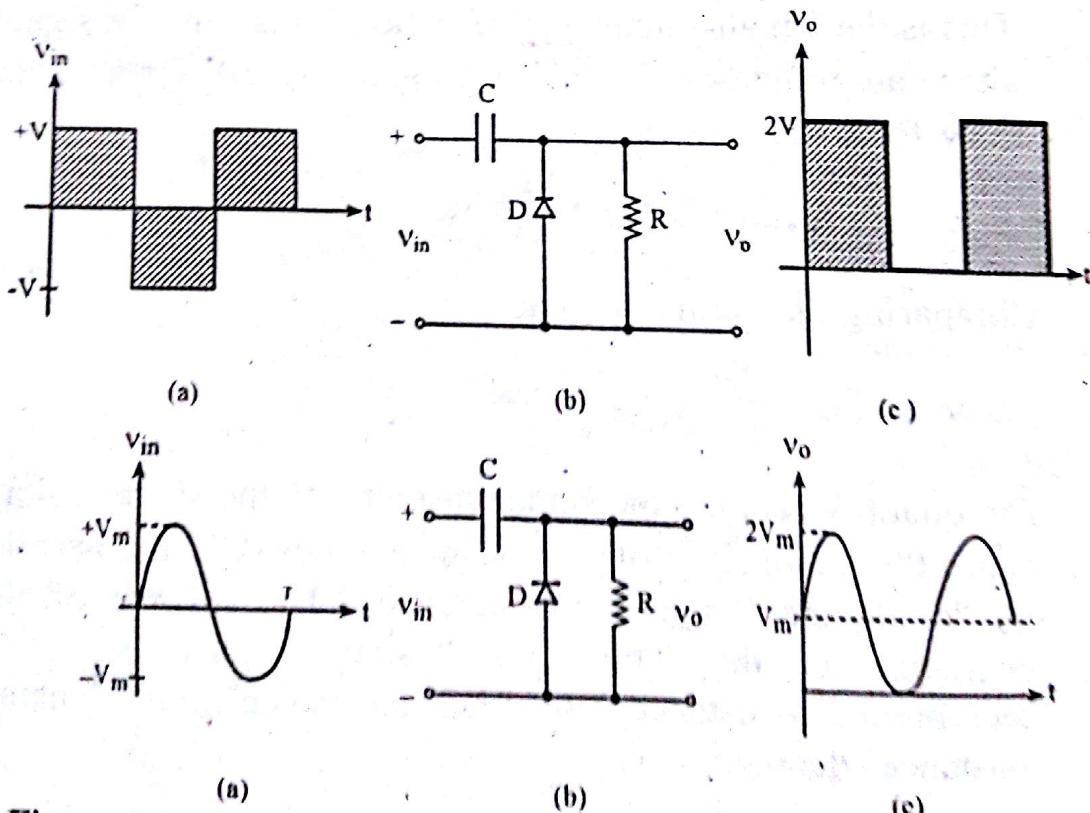


Figure 2.17 (a) Input waveform (b) A positive clamer (c) Output waveform

ii. Negative clammer

A negative clammer shifts its input waveform in a negative direction, so that it lies below a dc reference voltage.

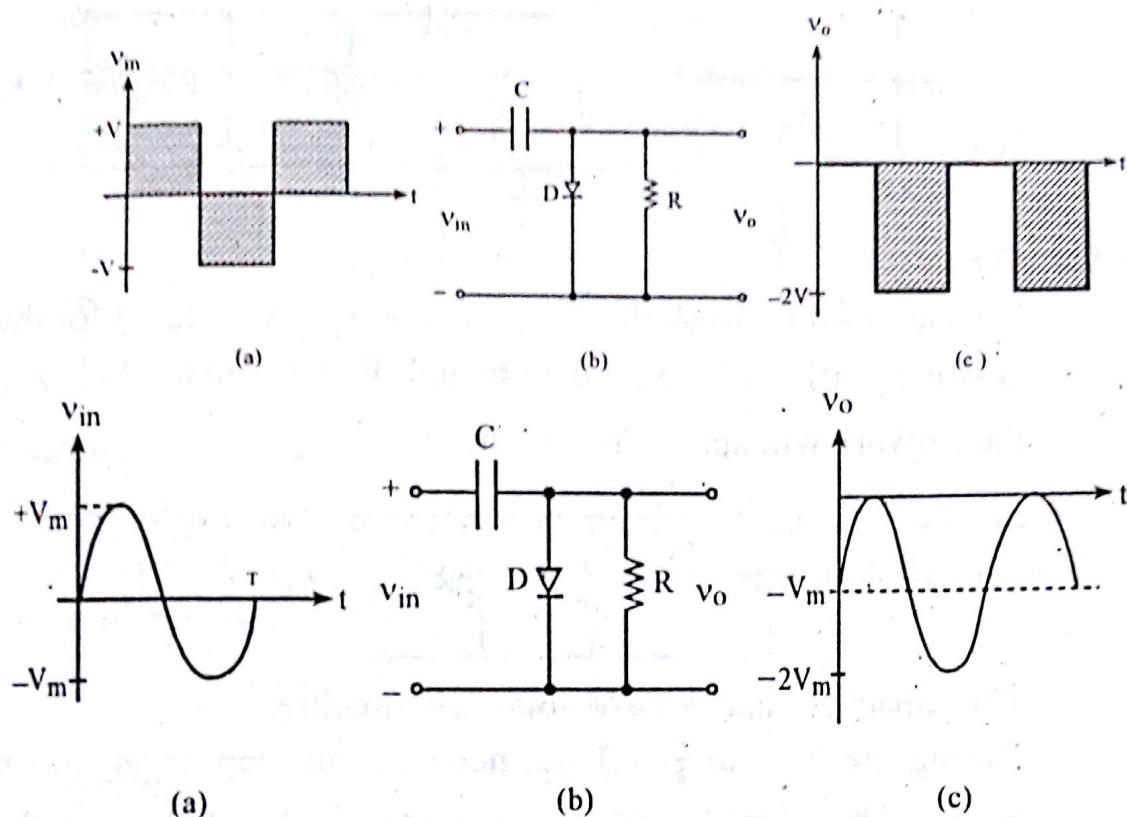


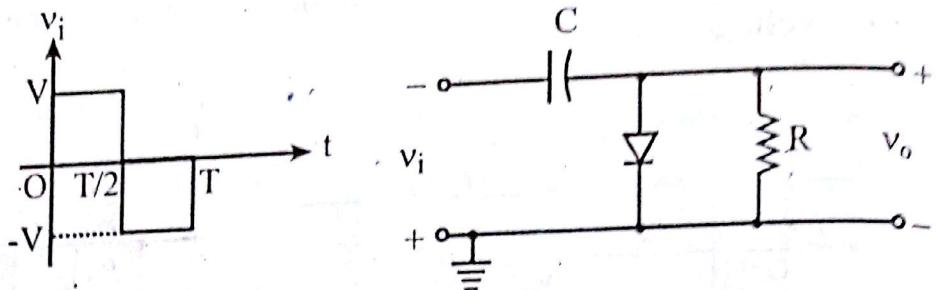
Figure 2.18 (a) Input waveform (b) A negative clammer (c) Output waveform

In general, the following steps may be helpful when analyzing clamping networks:

- i. Start the analysis by examining the response of the portion of the input signal that will forward bias the diode.
- ii. During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the surrounding network.
- iii. Assume that during the period when the diode is in the "off" state the capacitor holds on to its established voltage level.
- iv. Throughout the analysis, maintain a continual awareness of the location and defined polarity for v_o to ensure that the proper levels are obtained.
- v. Check that the total swing of the output matches that of the input.

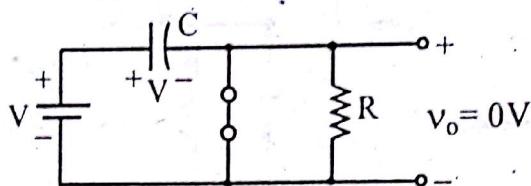
Problem 2.2

Find v_o for the network given below for the input indicated.



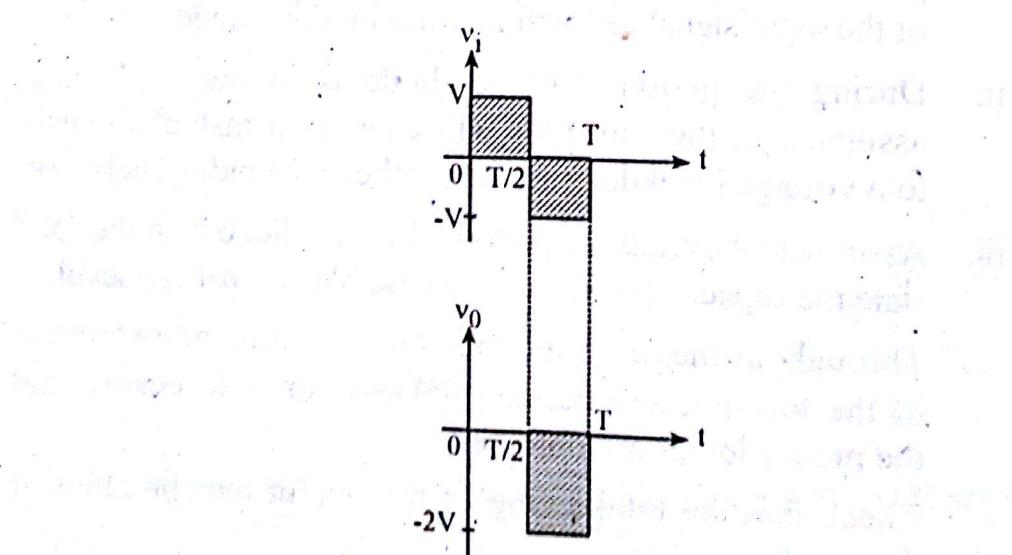
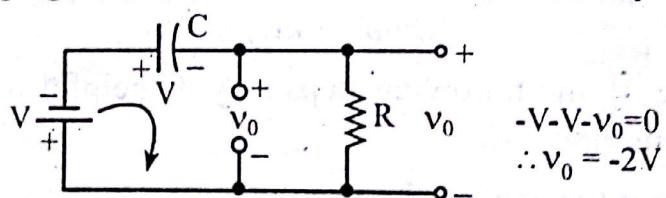
Solution:

For the given network the diode will be forward biased for the positive portion of the applied signal. For the interval $0 \rightarrow \frac{T}{2}$ the network will appear as shown.



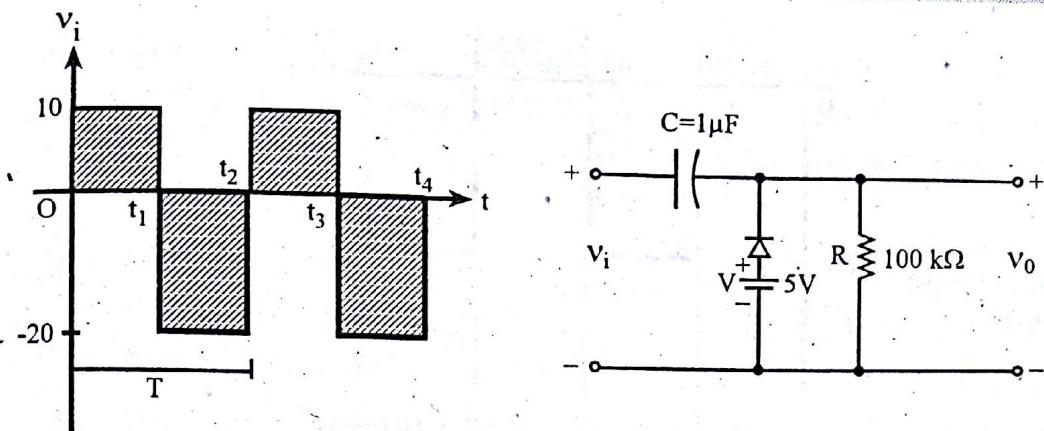
The capacitor charges to V volts very quickly.

During the interval $\frac{T}{2} \rightarrow T$ the network will appear as shown below. The capacitor retains its voltage (V volts) since the discharging time constant $\tau = RC$ chosen is very large.



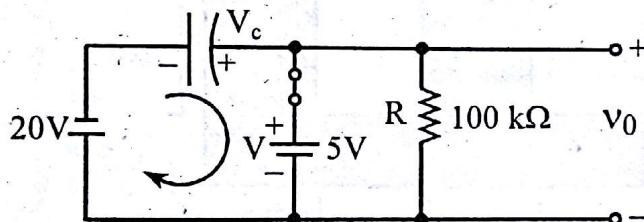
Problem 2.3

Determine v_o for the network given below for the input indicated.



Solution:

We begin the analysis considering the interval t_1 to t_2 because in this interval, the diode will be forward biased. The network will appear as shown.



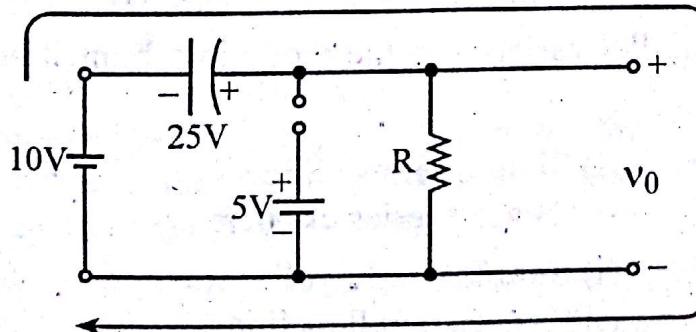
$$-20 + V_C - 5 = 0$$

$$\therefore V_C = 25 \text{ V}$$

The capacitor will therefore charge up to 25 V.

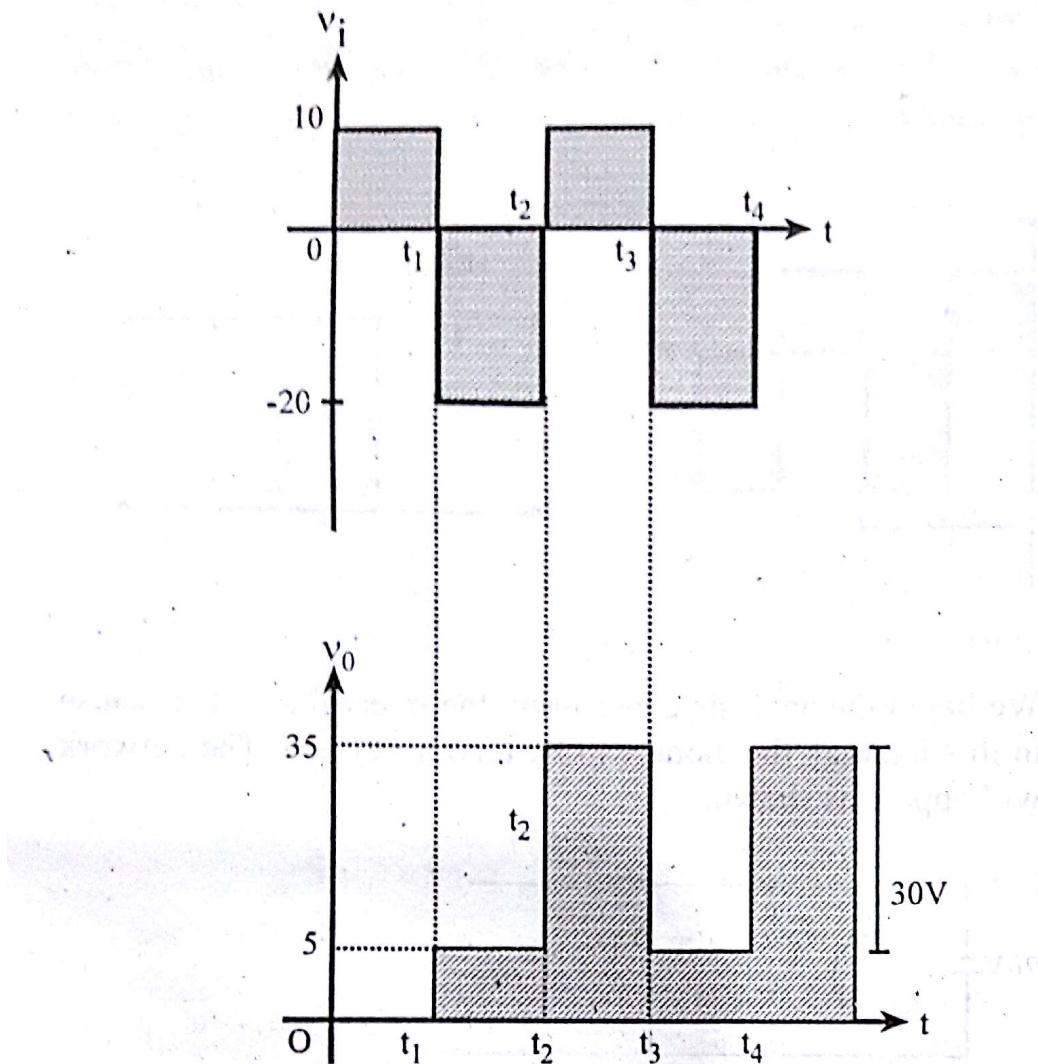
$$v_o = 5 \text{ V}$$

For the period $t_2 \rightarrow t_3$ the network will appear as shown.



$$+ 10 + 25 - v_o = 0$$

$$\therefore v_o = 35 \text{ V}$$



Clippers (sometimes called limiters)

Clippers are networks that employ diodes to "clip" away a portion of an input signal without distorting the remaining part of the applied waveform. There are two general categories of clippers: series and parallel. The series configuration is defined as one where the diode is in series with the load, whereas the parallel variety has the diode in a branch parallel to the load.

Series clippers - (i) Simple series clippers
(ii) Biased series clippers

Parallel clippers - (i) Simple parallel clippers
(ii) Biased parallel clippers

Clippers are useful in signal shaping, circuit protection, and communication.

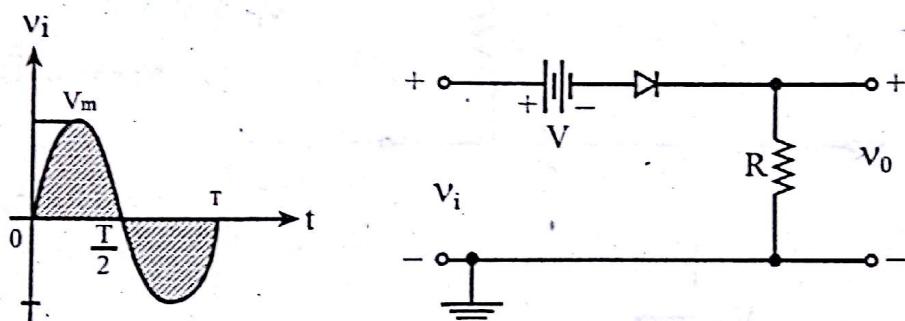
Analysis of series clippers

Important steps:

- i. Take careful note of where the output voltage is defined.
- ii. Try to develop an overall sense of the response by simply noting the "pressure" established by each supply and the effect it will have on the conventional current direction through the diode.
- iii. Determine the applied voltage (transition voltage) that will result in a change of state for the diode from the "off" to the "on" state.
- iv. It is often helpful to draw the output waveform directly below the applied voltage using the same scales for the horizontal axis and the vertical axis.

Problem 2.4

Determine the output waveform for the input shown below.



Solution:

For the network in the above example, the direction of the diode suggests that the signal v_i must be positive to turn it on. The dc supply further requires that the voltage v_i be greater than V volts to turn the diode on. The negative region of the input signal is "pressurizing" the diode into the "off" state, supported further by the dc supply. In general, therefore, we can be quite sure that the diode is an open circuit ("off" state) for the negative region of the input signal.

Now, we determine the applied voltage (transition voltage) that will cause a change in state for the diode. For the ideal diode the transition between states will occur at the point on the characteristics where $v_d = 0$ and $i_d = 0$.

The level of v_i that will cause a transition in state is $v_i = V$.

For $v_i = V$, $v_o = 0V$.

For an input voltage greater than V volts the diode is in the short-circuit state, while for input voltages less than V volts it is in the open-circuit or "off" state.

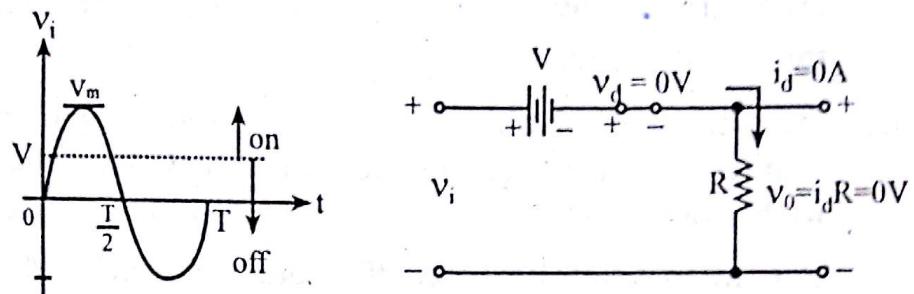
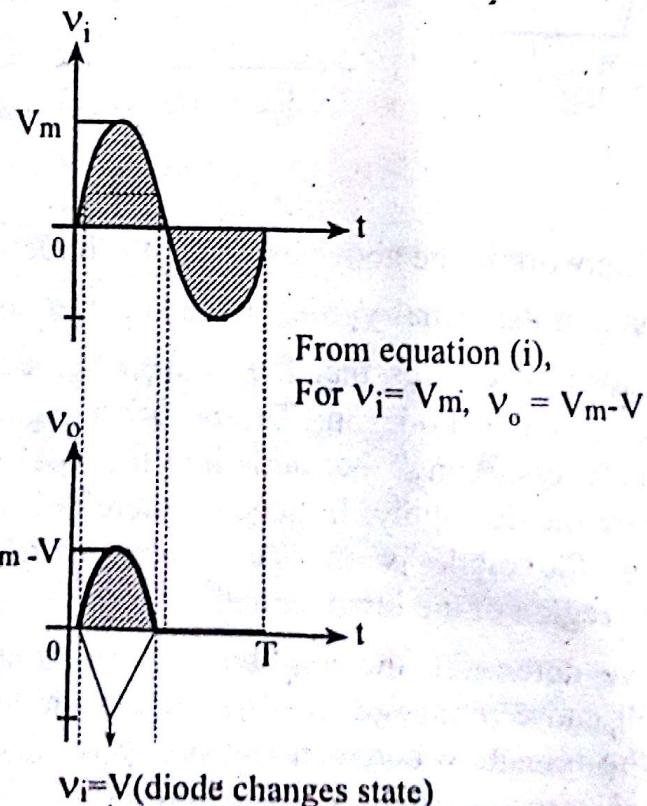
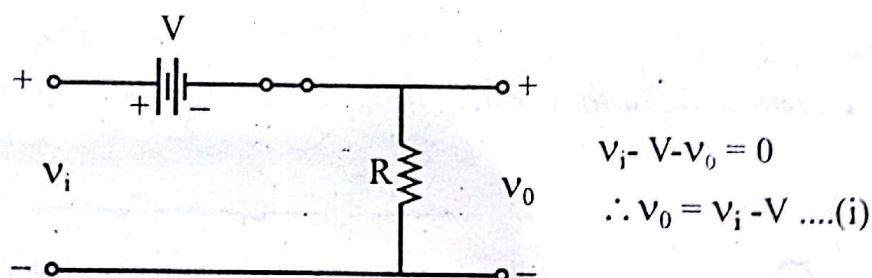
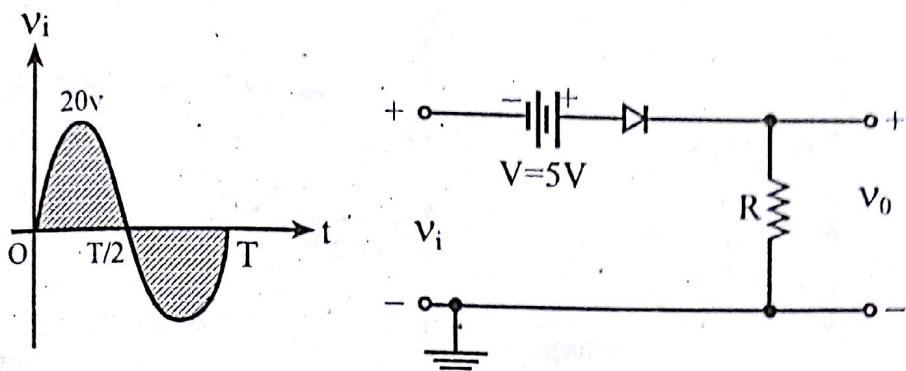


Fig.: Determining the transition level for the circuit



Problem 2.5

Determine the output waveform for the sinusoidal input of Fig. shown below.



Solution:

- Step 1: The output is again directly across the resistor R
- Step 2: The positive region of v_i and the dc supply are both applying "pressure" to turn the diode on. The result is that we can safely assume the diode is in the "on" state for the entire range of positive voltages for v_i . Once the supply goes negative, it would have to exceed the dc supply voltage of 5V before it could turn the diode off.
- Step 3: The transition from one state to the other will occur when

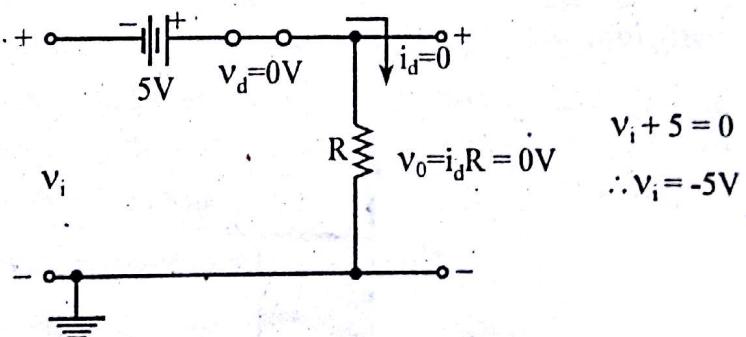
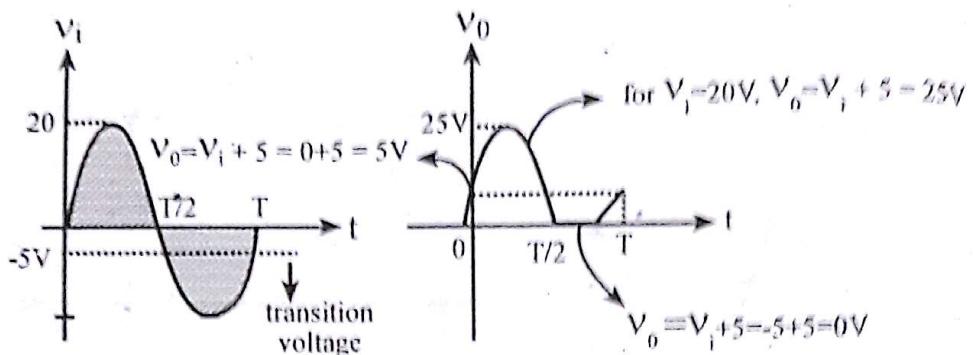


Fig.: Determining the transition level for the circuit

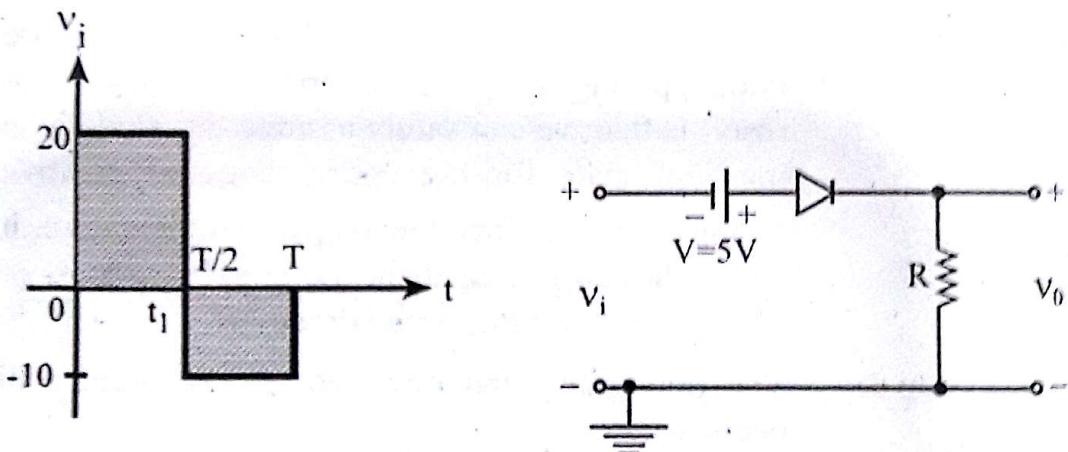
- Step 4: In Fig. shown below, a horizontal line is drawn through the applied voltage at the transition level. For voltages less than -5V the diode is in the open-circuit state and the output is 0V, as shown in the sketch of v_o . Using Fig. below, we find

that for conditions when the diode is on and the diode current is established the output voltage will be the following, as determined using KVL:

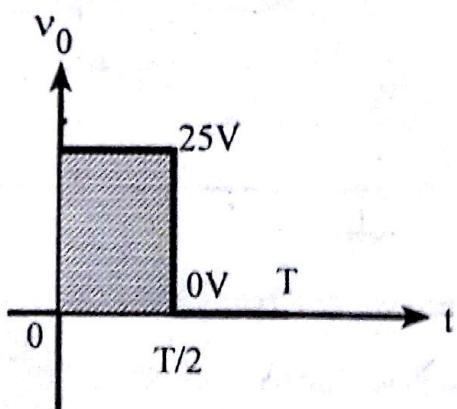


Problem 2.6

Find the output voltage for the network shown.



Solution:

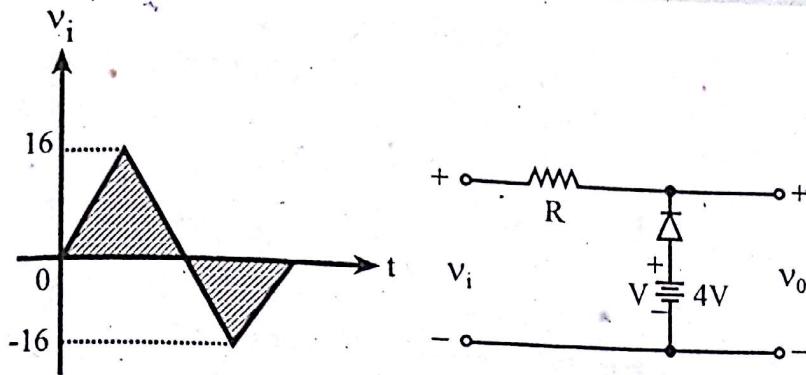


Analysis of parallel clippers

The analysis of parallel clippers is very similar to that applied to series configurations, as demonstrated in the coming examples:

Problem 2.7

Determine v_o for the network of Fig. shown below.



Solution:

- Step 1: The output is defined across the series combination of the 4V supply and the diode, not across the resistor R.
- Step 2: The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "on" state for a good portion of the negative region of the input signal. In fact, it is interesting to note that since the output is directly across the series combination, when the diode is in its short-circuit state the output voltage will be directly across the 4V dc supply, requiring that the output be fixed at 4V. In other words, when the diode is on the output will be 4V. Other than that, when the diode is an open circuit, the current through the series network will be 0 mA and the voltage drop across the resistor will be 0 V. That will result in $v_o = v_i$ whenever the diode is off.

- Step 3: The transition level of the input voltage is

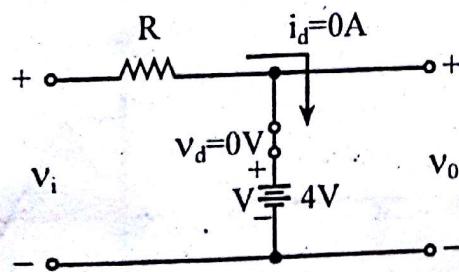
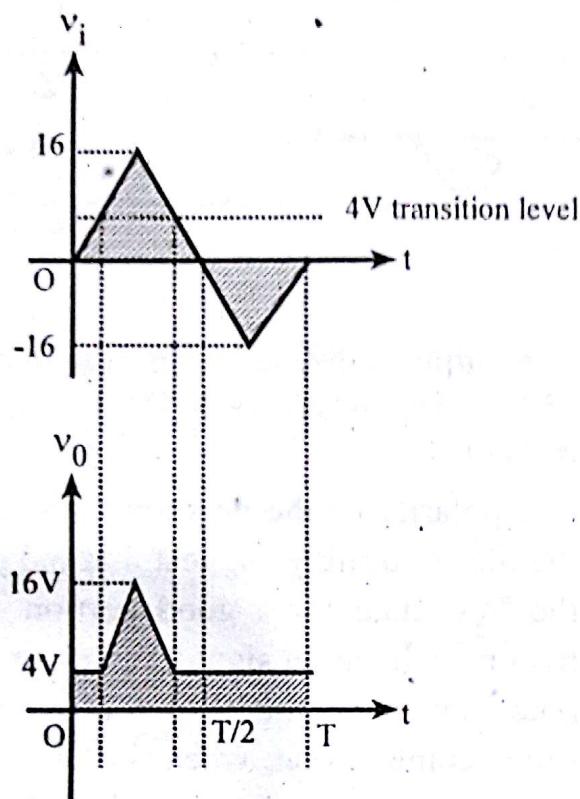


Fig.: Determining the transition level of the circuit.

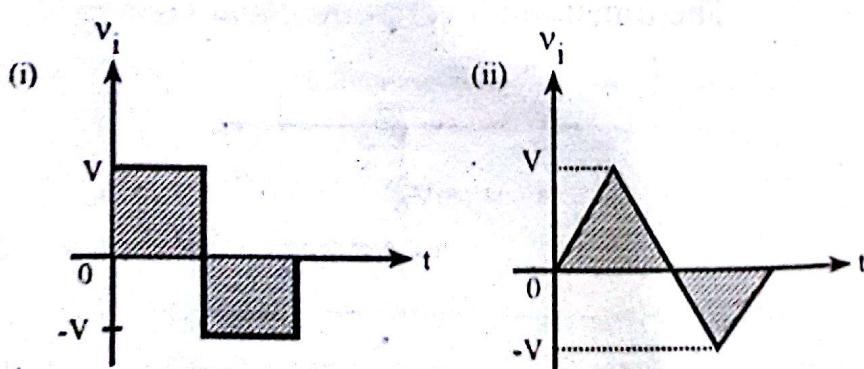
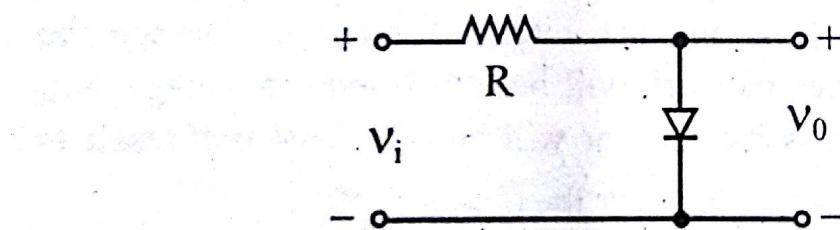
Change in state is at $v_i = 4V$

Step 4: The transition level is drawn along with $v_o = 4V$ when the diode is on. For $v_i \geq 4V$, $v_o = 4V$, and the waveform is simply repeated on the output plot.



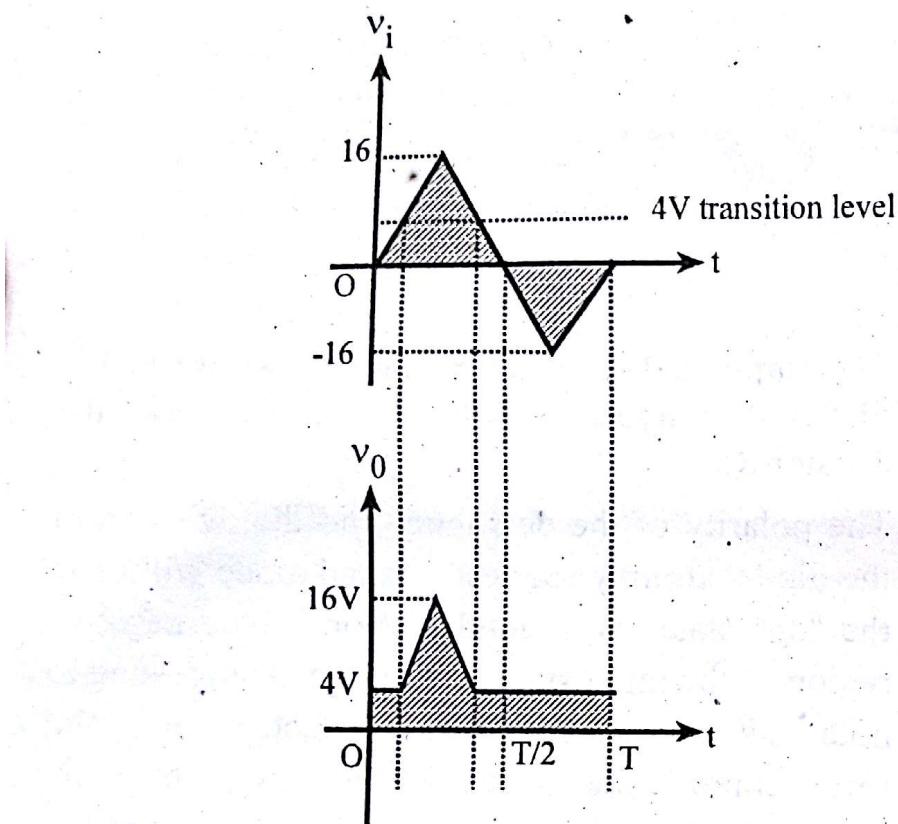
Problem 2.8

For the network given below, find the output waveform if the input waveform is



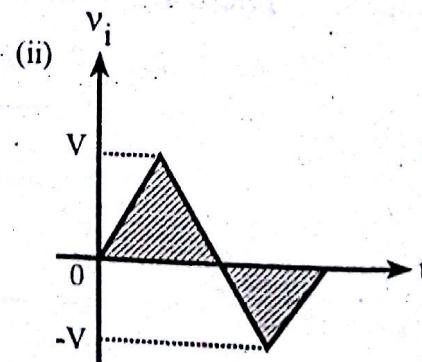
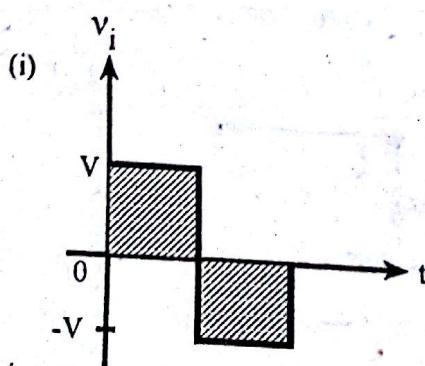
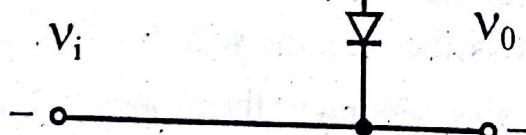
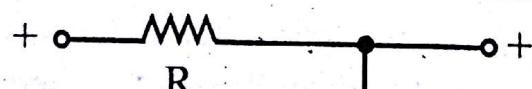
Change in state is at $v_i = 4V$

Step 4: The transition level is drawn along with $v_o = 4V$ when the diode is on. For $v_i \geq 4V$, $v_o = 4V$, and the waveform is simply repeated on the output plot.

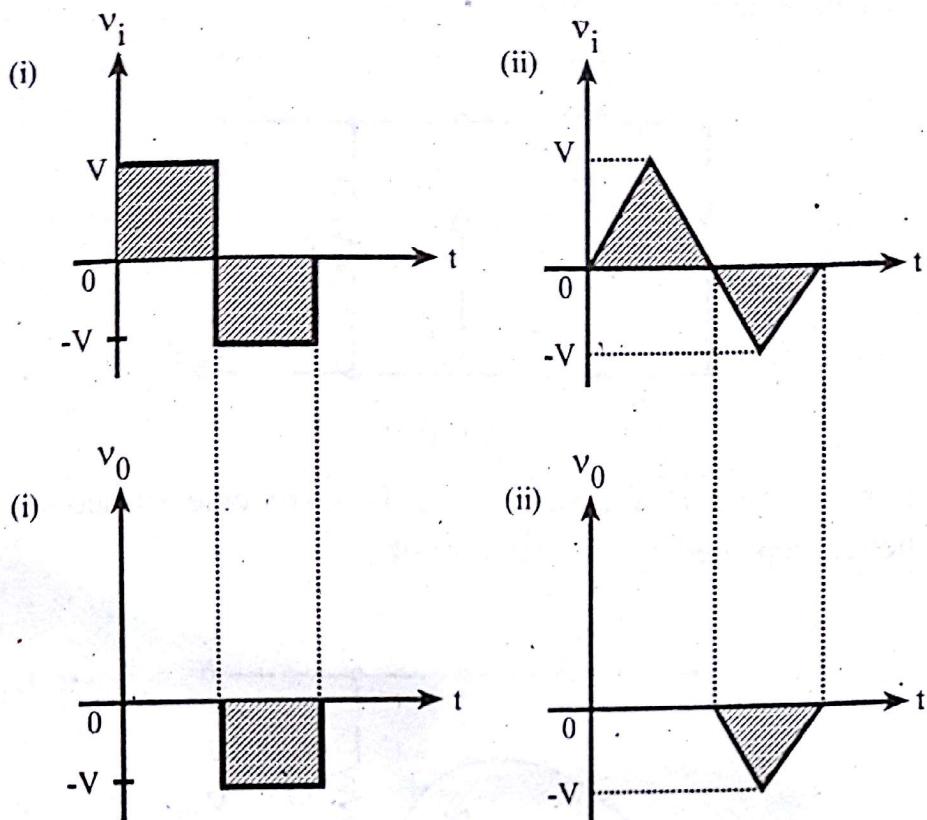


Problem 2.8

For the network given below, find the output waveform if the input waveform is

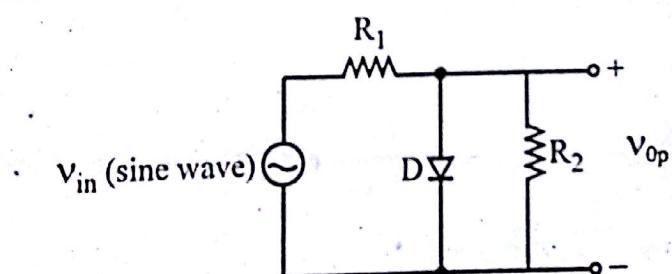


Solution:



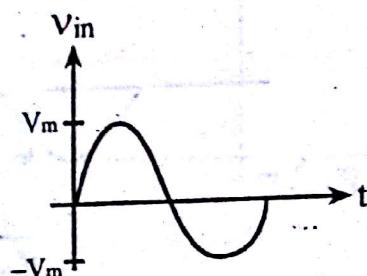
Problem 2.9

Draw the output waveform of the circuit and indicate the peak output voltage. Assume diode is ideal. [2067 Chaitra]

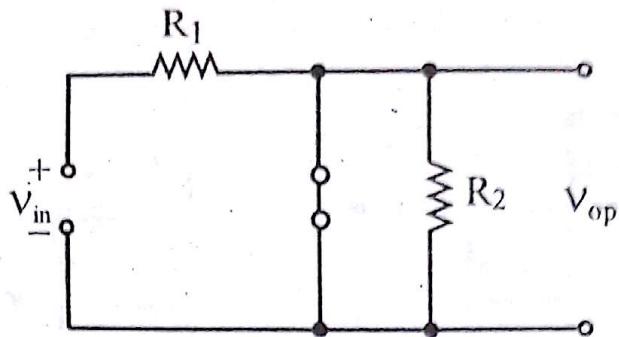


Solution:

Input waveform for $v_{in} = V_m \sin \omega t$ is

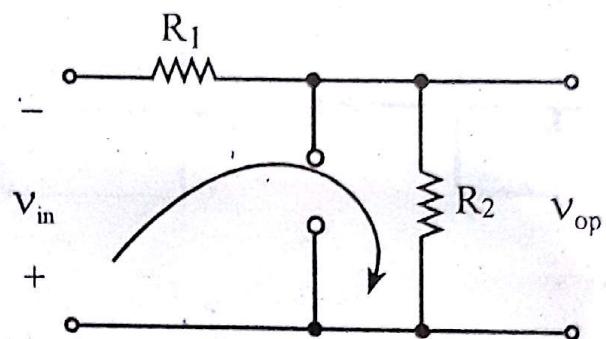


For positive half cycle, diode D is forward biased and hence, replaced by a short circuit.



$$\therefore v_{op} = 0 \text{ V.}$$

For negative half cycle, diode D is reverse biased and hence, replaced by an open circuit.

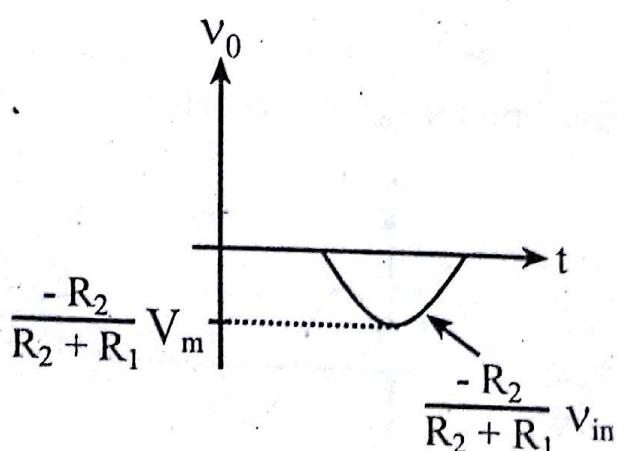


$$v_{op} = \frac{R_2}{R_1 + R_2} (-v_{in})$$

For $v_{in} = V_m$,

$$v_{op} = \frac{R_2}{R_1 + R_2} (-V_m) = \frac{-R_2}{R_1 + R_2} (V_m)$$

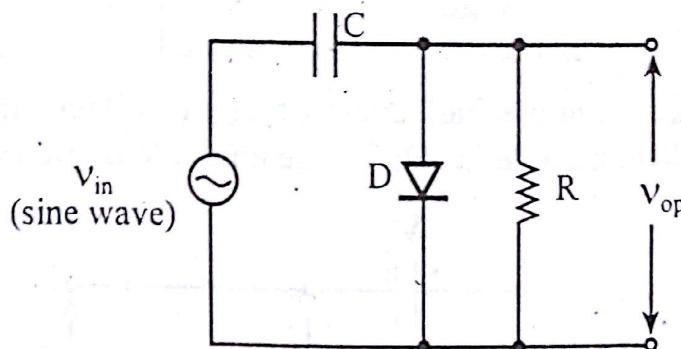
The output waveform is



Problem 2.10

Draw output waveforms of the following circuits and indicate the peak output voltage. Assume diode is ideal.

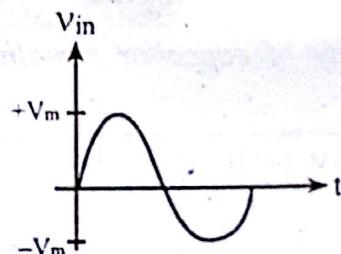
[2067 Chaitra]



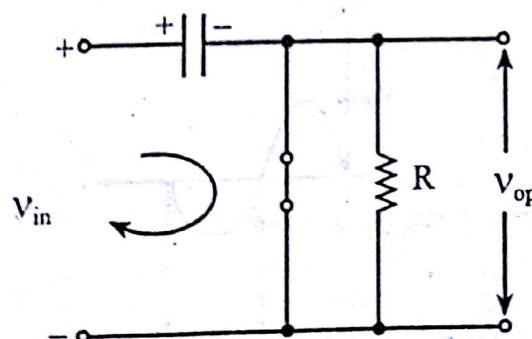
Solution:

$$\text{Let } v_{in} = V_m \sin \omega t$$

Input waveform for $v_{in} = V_m \sin \omega t$ is



Positive half cycle is considered first because it will forward bias the diode. When the diode starts to conduct, capacitor starts being charged. At the positive peak, the capacitor is charged to maximum value.



Applying KVL,

$$+v_{in} - V_c = 0$$

$$\text{For } v_{in} = V_m,$$

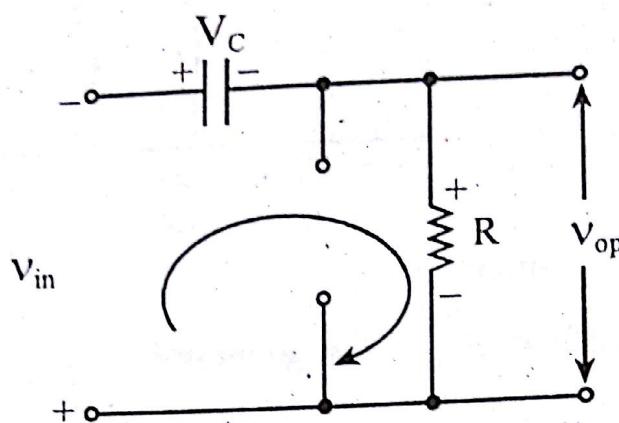
$$+V_m - V_c = 0$$

or, $V_c = V_m$ (The capacitor charges to $+V_m$ volts)

$$\text{and } v_{op} = 0V$$

Slightly beyond the positive peak, the diode is shunt off and the capacitor charged to V_m behaves as a battery.

For entire negative half cycle of input voltage, the diode is "OFF". When diode is "OFF", the equivalent circuit is



Note: The polarity of capacitor remains same as it was during charging process.

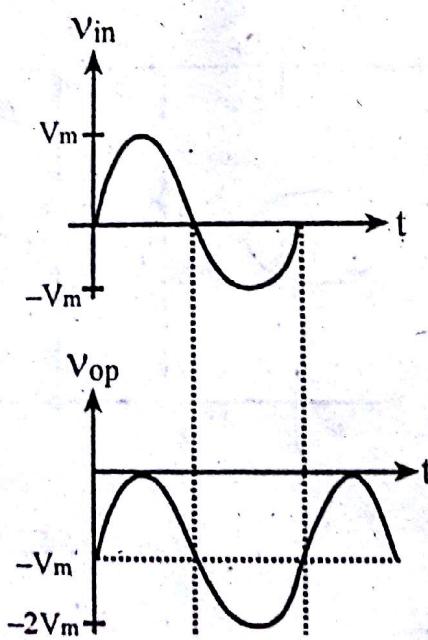
$$- \quad v_{in} - V_c - v_{op} = 0$$

For $v_{in} = V_m$,

$$- \quad V_m - V_m - v_{op} = 0$$

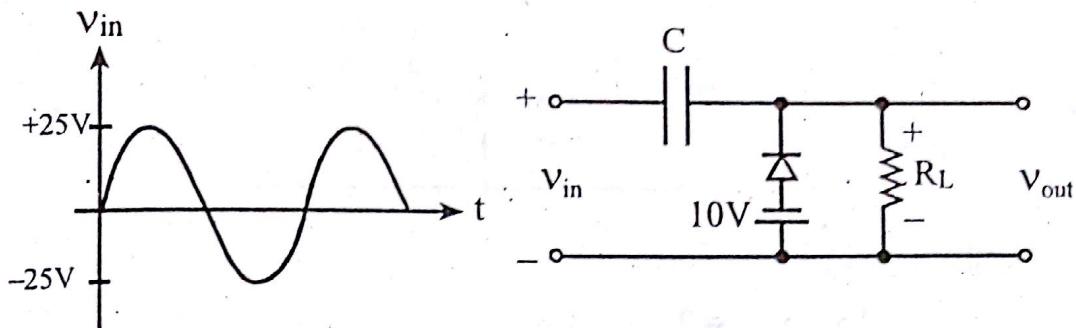
$$\therefore v_{op} = -2 V_m$$

The output waveform is drawn below.



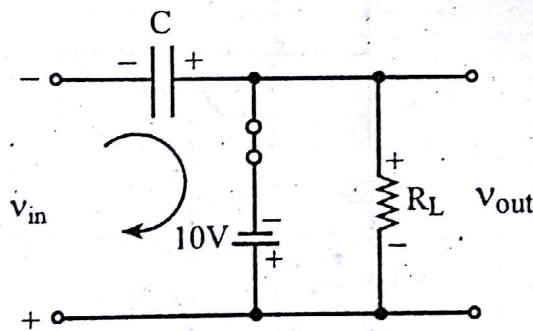
Problem 2.11

Find the output waveform of the given circuit. [2069 Bhadra]



Solution:

Negative half cycle is considered first because it will forward bias the diode. But, we should note that the diode will be "ON" only after negative half cycle of input voltage reaches 10V (considering ideal diode). For negative half cycle (after diode is ON), the diode is replaced by a short circuit (considering ideal case of diode).



Applying KVL,

$$-v_{in} + V_C + 10 = 0$$

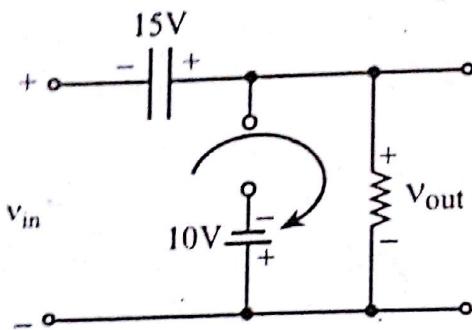
For $v_{in} = 25V$,

$$-25 + V_C + 10 = 0$$

or, $V_C = 15 V$ (The capacitor charges to 15 V)

Also, $v_{out} = -10 V$

For positive half cycle, the diode is replaced by an open circuit (considering ideal case of diode).



Applying KVL, we have

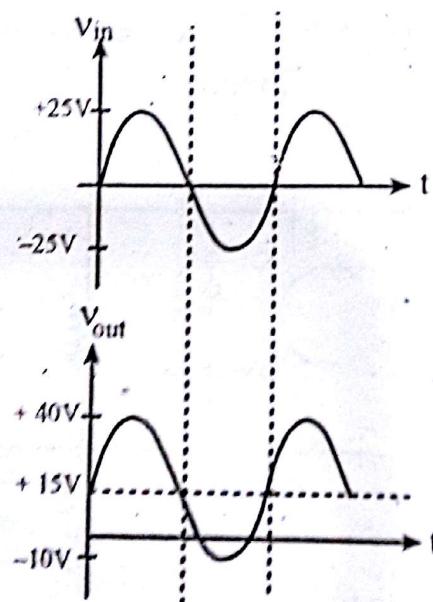
$$v_{in} + 15 - v_{out} = 0$$

For $v_{in} = 25V$,

$$25 + 15 - v_{out} = 0$$

$$\text{or, } v_{out} = 40 \text{ V.}$$

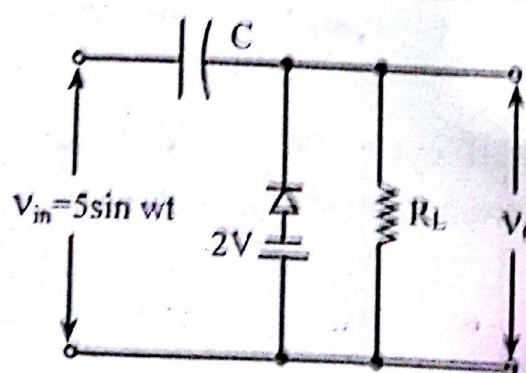
The output waveform is drawn below.



Problem 2.12

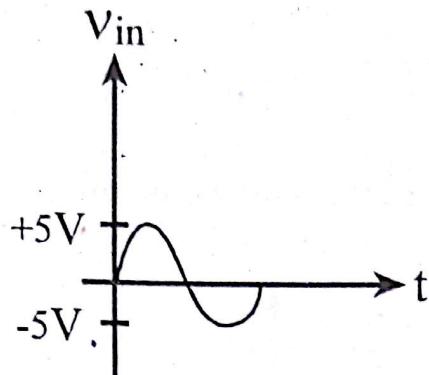
Find the output waveform for the following circuit.

[2008 Bhadra]

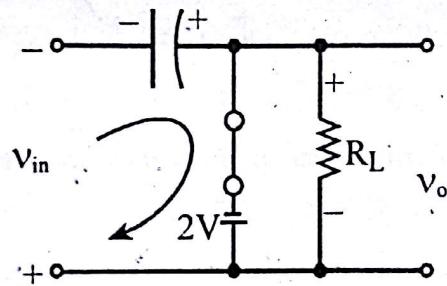


Solution:

$$v_{in} = 5 \sin \omega t = V_m \sin \omega t$$



Negative half cycle is considered first because it will forward bias the diode. But, we should note that the diode will be "ON" only after negative half cycle of input voltage reaches 2V (considering ideal diode). For negative half cycle (after diode is ON), the diode is replaced by a short circuit.



Applying KVL,

$$-v_{in} + V_C + 2 = 0$$

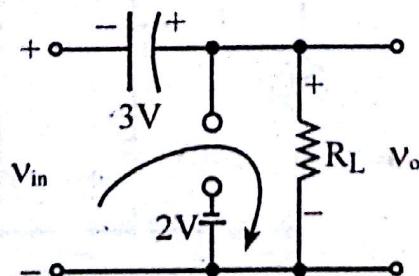
For $v_{in} = 5V$,

$$-5 + V_C + 2 = 0$$

or, $V_C = 3V$ (The capacitor charges to 3V)

Also, $v_o = -2V$

For positive half cycle, the diode is replaced by an open circuit.



Applying KVL,

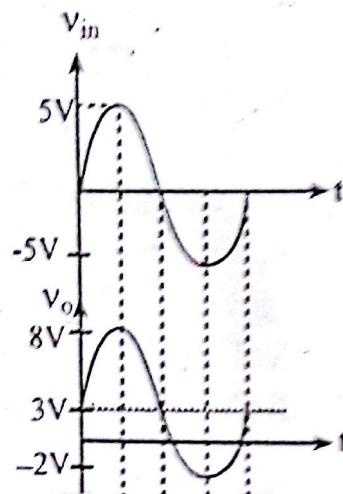
$$+v_{in} + 3 - v_o = 0$$

For $v_{in} = 5V$,

$$+5 + 3 - v_o = 0$$

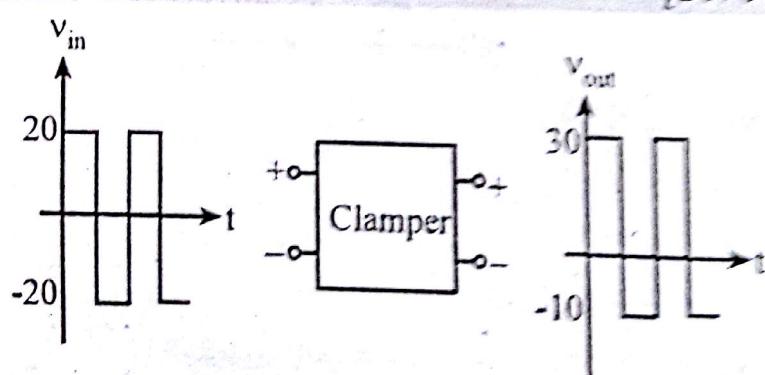
$$\therefore v_o = 8V$$

The output waveform is drawn below.

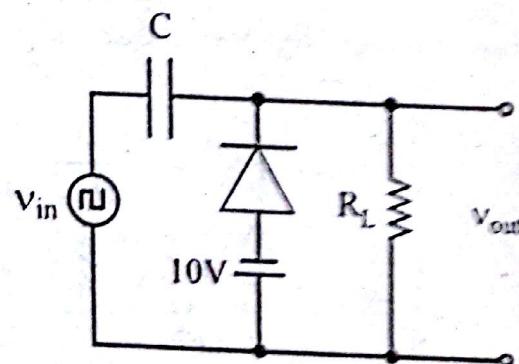


Problem 2.13

Design a clamper circuit to perform the function indicated in the figure below. [2070 Marks]



Solution:



Check:

When diode is forward biased, the diode is replaced by a short circuit.

$$-20 + v_c + 10 = 0$$

$$\therefore v_c = +10V$$

and

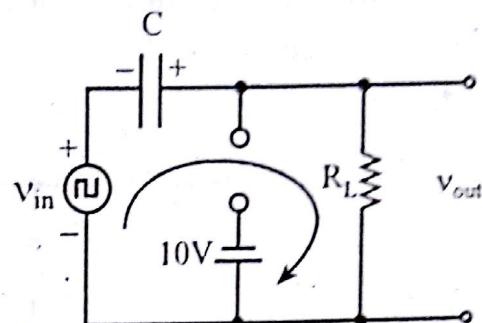
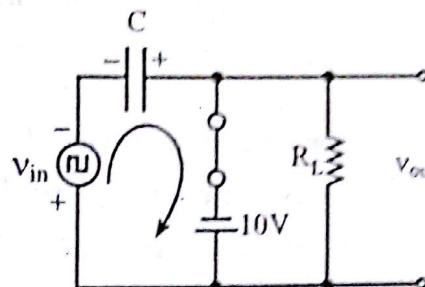
$$v_{out} = -10V$$

When diode is reverse biased,
the diode is replaced by an
open circuit.

$$20 + v_c - v_{out} = 0$$

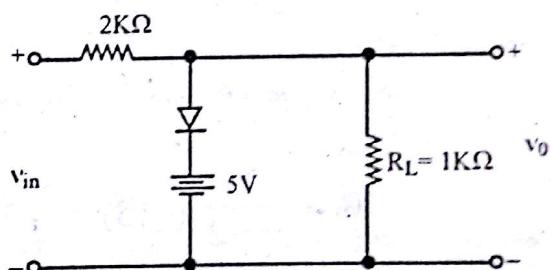
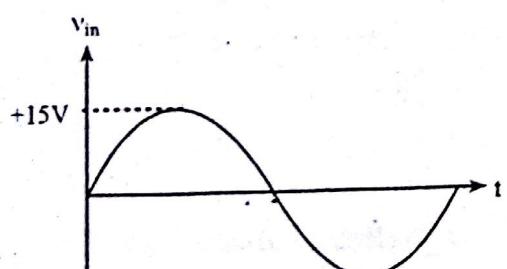
$$\text{or, } 20 + 10 - v_{out} = 0$$

$$\therefore v_{out} = 30V$$



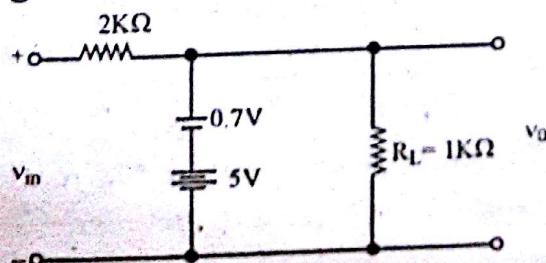
Problem 2.14

Draw the output waveform of circuit shown below. Assume real silicon diode.
[2071 Bhadra]



Solution:

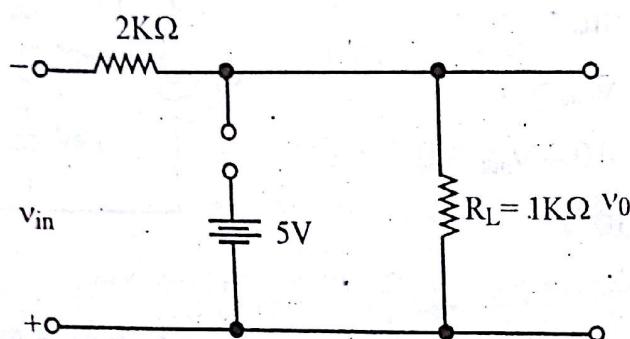
Positive half cycle of input voltage is considered first because it will forward bias the diode. And, when we consider practical silicon diode, voltage drop of 0.7 V should be taken into account. Hence, diode will be "ON" only after input voltage reaches 5.7 V. In this case, equivalent circuit is



$$v_o = 0.7 + 5 = 5.7 \text{ V}$$

For remaining portion of positive half cycle, diode will be "OFF", and thus, $v_o = v_{in}$.

For entire negative half cycle of input voltage, the diode is reverse biased. Actually in this condition, negligible amount of reverse saturation current flows. For simplifying analysis, we may consider diode as an "open circuit". The equivalent circuit is

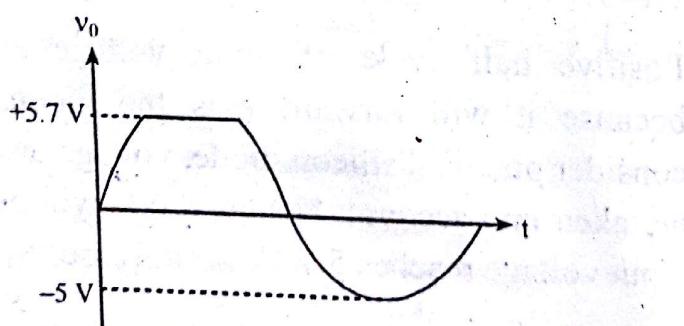


$$v_o = \frac{1}{1+2} (-v_{in})$$

For $v_{in} = 15 \text{ V}$,

$$v_o = \frac{1}{1+2} (-15) = -5 \text{ V}$$

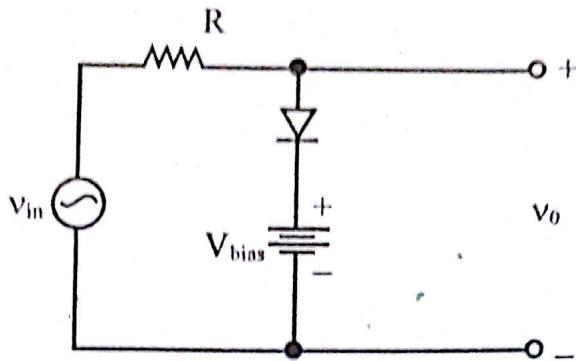
The output waveform is therefore



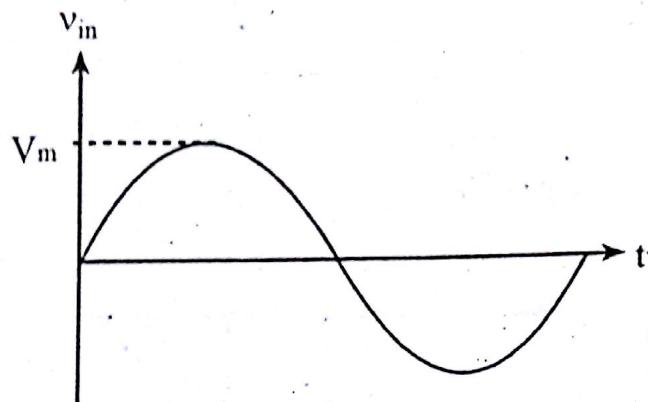
Problem 2.15

Draw the sinusoidal waveform of the following circuit and indicate the output voltage. Assume diode is ideal.

[2071 Magh]



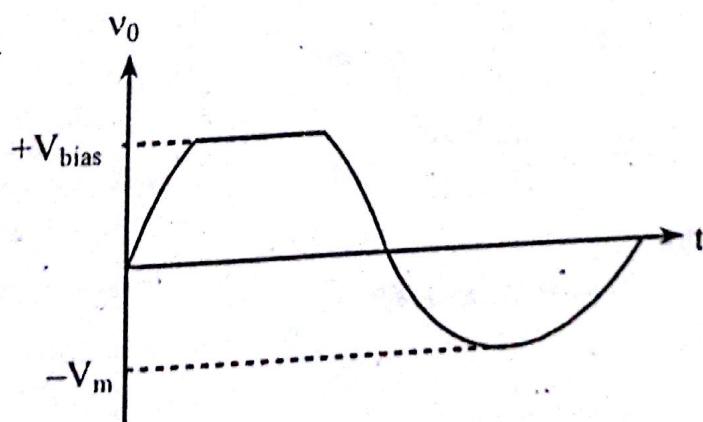
Solution: Let $v_{in} = V_m \sin \omega t$.



The diode is not "on" until the positive half cycle of input voltage reaches V_{bias} . The output voltage is $v_o = v_{in}$ for the portion of positive half cycle from zero to V_{bias} and V_{bias} to zero. For the remaining portion of positive half cycle, $v_o = V_{bias}$.

For entire negative half cycle of input voltage, the diode is "off", and hence, $v_o = v_{in}$.

The output waveform is shown below.

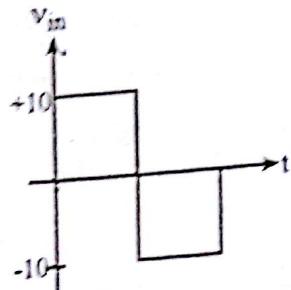


Problem 2.16

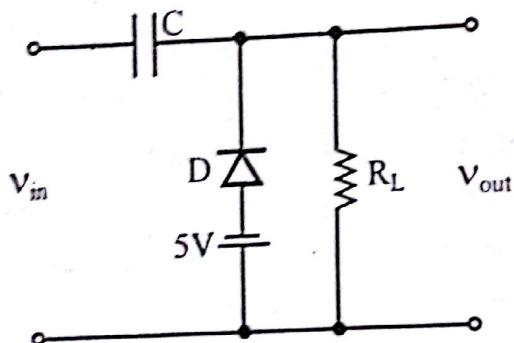
Draw the clamper circuit that adds +5 volts DC level on AC voltage.
[2072 Magh]

Solution:

Consider input AC voltage as

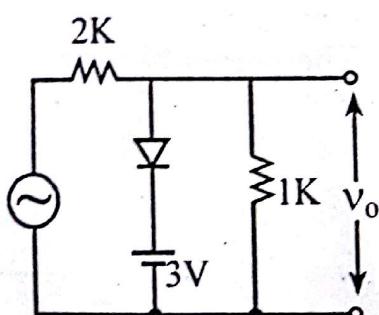
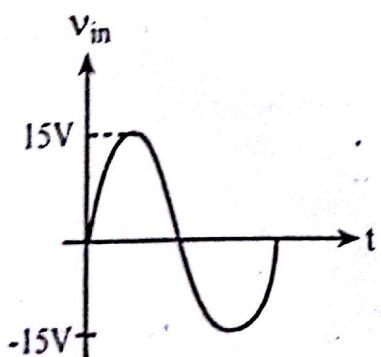


The required clamper circuit that adds +5 volts DC level on input AC voltage is



Problem 2.17

Find the output waveform of the given circuit. [2073 Magh]



Solution:

[Do it yourself]

ZENER DIODE

A Zener diode is a special type of diode that is designed to operate in the reverse breakdown region. An ordinary diode operated in this region will usually be destroyed due to excessive current. This is not the case for the Zener diode.

The circuit symbol for Zener diode and its conduction direction is shown below.

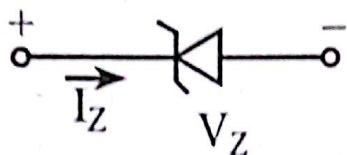


Figure 2.18 Zener diode

The i-v characteristics of a Zener diode is shown below.

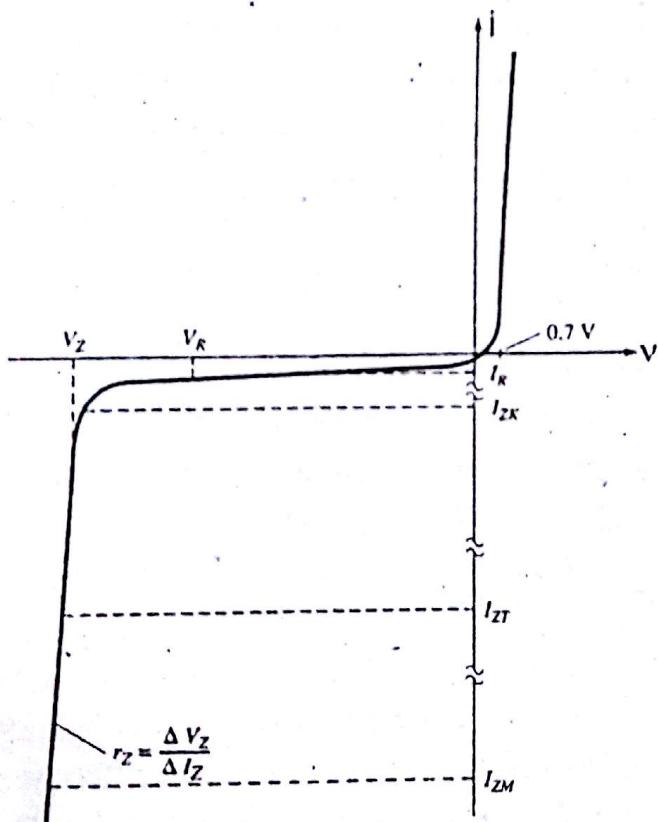


Figure 2.19 Zener diode characteristics with the equivalent model for each region

V_Z : Zener breakdown voltage

I_{ZT} : Test current for measuring V_Z

I_{ZK} : Reverse current near the knee of the characteristic, the minimum reverse current to sustain breakdown

I_{ZM} : Maximum Zener current, limited by the maximum power dissipation

ZENER EFFECT

In a heavily doped pn-junction diode with a very narrow depletion region, the electric field strength (volts/width) produced by a reverse bias voltage can be very high. The high intensity electric field causes electrons to break away from their atoms, thus converting the depletion region from an insulating material into a conductor. This effect is called Zener effect. This is ionization by electric field and it usually occurs with reverse bias voltage less than 5V i.e., $V_Z < 5V$.

AVALANCHE EFFECT

In a highly doped pn-junction diode with depletion region too wide for Zener effect, increase in voltage across the diode increases the velocity of the minority carriers responsible for reverse saturation current I_S . Eventually, their velocity and associated kinetic energy will be sufficient to release additional carriers through collisions with other stable atomic structure. This is ionization by collision. These additional carriers can then aid the ionization process to the point where a high avalanche current (I_Z) is established. This effect is called Avalanche effect. It usually occurs with reverse bias voltage levels above 5V i.e., $V_Z > 5V$.

LIGHT EMITTING DIODES (LEDS)

LEDs are optoelectronic devices which emit a fairly narrow bandwidth of visible (usually red, orange, yellow or green) or invisible (infrared) light when its internal diode junction is stimulated by a forward electric current/voltage (power).

The operation of LED is based on the phenomenon of electroluminescence. Electroluminescence is the emission of light from a semiconductor under the influence of an electric field.

LEDs are broadly divided into two categories:

- (i) Surface - emitting LEDs
- (ii) Edge - emitting LEDs

Light emitting diodes are available in various formats with the round types being most popular. The symbol for a LED is shown in the figure below.



Figure 2.20 Symbol of a LED

Application of LEDs

- i. LEDs are used in burglar-alarm systems.
- ii. They are used in solid-state video displays.
- iii. They are used in the field of optical fibre communication system.
- iv. They are used for numeric displays in hand-held or pocket calculators.

PHOTODIODE

Photodiode is a two terminal semiconductor pn-junction device having a small transparent window to allow light to strike the pn-junction and is designed to operate with reverse bias.

If a reverse-biased pn-junction is illuminated- that is, exposed to incident light- the photons impacting the junction cause covalent bonds to break, and thus, electron-hole pairs are generated in the depletion layer. The electric field in the depletion region then sweeps the liberated electrons to the n-side and the holes to the p-side, giving rise to a reverse current across the junction. This current, known as photocurrent, is proportional to the intensity of the incident light. Such diodes are called photodiodes which can be used to convert light signals into electrical signals. The definition of photodiode is now clear.

The basic biasing arrangement, construction, and symbol for the device appears below.

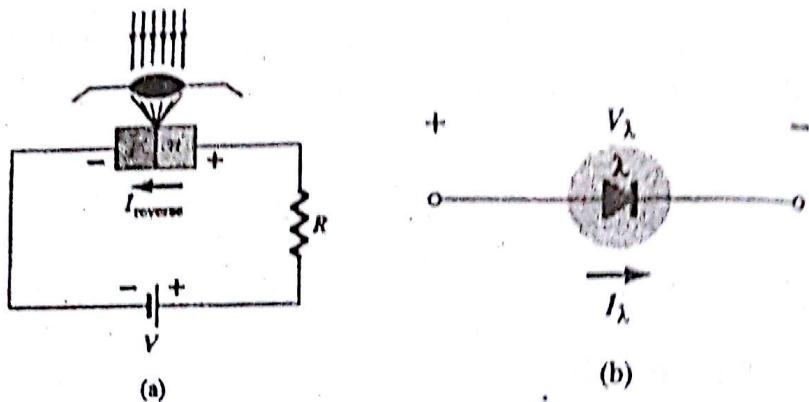


Figure 2.21 Photodiode: (a) Basic biasing arrangement and construction (b) symbol

Relation between reverse current (I_λ) and luminous flux (f_c)

The almost equal spacing between the curves for the same increment in luminous flux reveals that the reverse current and the luminous flux are almost linearly related. In other words, an increase in the light intensity will result in a similar increase in reverse current. A plot of the two to show this linear relationship appears below for a fixed voltage V_A of 20 V.

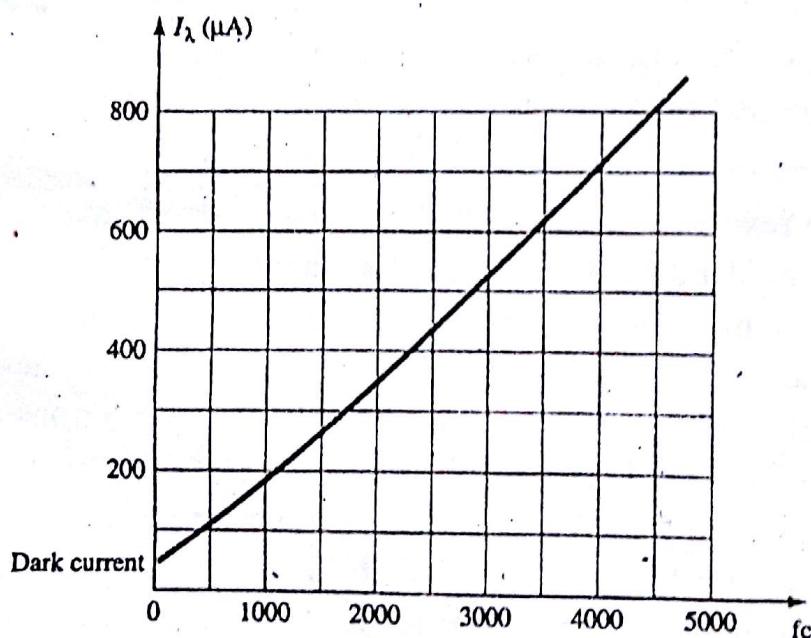


Figure 2.22 I_λ (μA) versus f_c (at $V_A = 20\text{V}$) for the photodiode

Application of photodiode

- Photodiode is used to count items on a conveyor belt.
- Photodiode is used in an alarm system.
- Photodiodes are also used in logic circuits that require stability and high speed.

VARACTOR DIODE

Special diodes that are fabricated to be used as voltage-variable capacitors are known as varactor diodes or simply, varactors. Varactor diode is a reverse-biased diode and its mode of operation depends on the capacitance that exist at the pn-junction. It is also called varicap or VVC (voltage variable capacitor) or tuning diode.

The pn-junction capacitance (transition capacitance) is given by

$$C_T = \epsilon \frac{A}{w_d}$$

where ϵ = permittivity of the semiconductor

A = the pn-junction area

w_d = depletion width

The symbol for a varactor diode is shown below.



Figure 2.23 Symbol of a varicap diode

Working principle

As the reverse-bias potential increases the width of the depletion region increases, which in turn reduces the transition capacitance. The characteristics of a typical commercially available varicap are shown below.

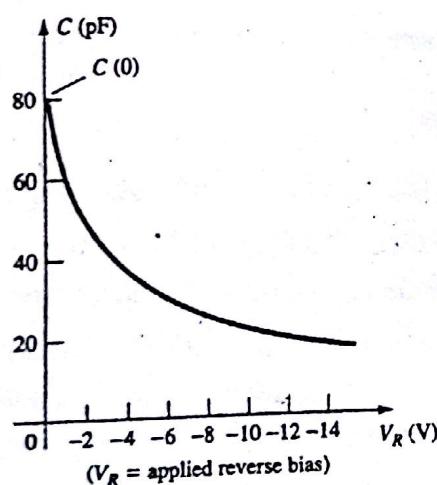


Figure 2.24 Varicap characteristics: $C(pF)$ versus V_R

Particularly, the junction capacitance varies inversely with the square root of the reverse bias voltage (V_R).

$$\text{i.e., } C_T \propto \frac{1}{\sqrt{V_R}}$$

Applications of varactor diode

- i. FM modulators
- ii. Automatic frequency control (AFC)
- iii. Automatic frequency tuning (AFT)
- iv. Band pass filter.

TUNNEL DIODE

A tunnel diode is a high conductivity two terminal pn-junction diode doped heavily-about 1000 times higher than a conventional junction diode. Due to heavy doping, the width of depletion layer is extremely reduced to a small value of the order of 10^{-5} mm. This reduced depletion layer can result in carriers punching through the junction even when they do not possess enough energy to overcome the potential barrier. The result is that large forward current is produced at relatively low forward voltage. Such a mechanism of conduction in which charge carriers (possessing very little energy) punch through a barrier directly instead of climbing over it is called tunneling. That is why, such diodes are called tunnel diodes.



Figure 2.25 Symbol of a tunnel diode

Working principle

The depletion region is an insulator because it locks charge carriers and usually charge carriers can cross it only when the external bias is large enough to overcome the barrier potential. However, because the depletion region in a tunnel diode is so narrow, it does not constitute a large barrier to electron flow. Consequently, a small forward or reverse bias can give charge carriers sufficient energy to cross the depletion region. When

this occurs, the charge carriers are said to be tunneling through the barrier.

Characteristics of tunnel diode

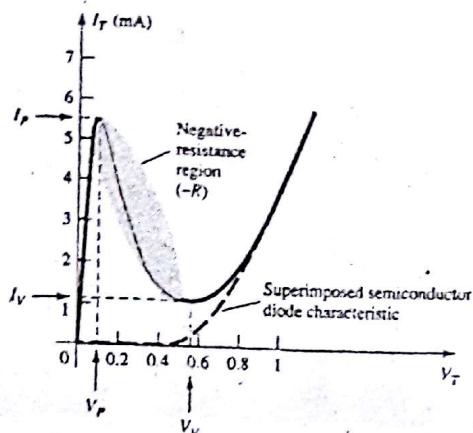


Figure 2.26 Tunnel diode characteristics

A forward biased tunnel diode initially increases forward current with the increase of forward voltage (V_T). Eventually, a peak level of tunneling is reached, and then further increase in forward voltage causes forward current to decrease. The decrease in forward current continues until the normal process of current flows across a forward-biased junction.

Application

Used in high-speed applications such as in computers where switching times in the order of nanoseconds or picoseconds are desirable.

RECTIFIER CIRCUITS

Rectifier is a device used for converting alternating current (AC) to direct current (DC).

1. Half-Wave Rectifier

The process of removing one-half the input signal to establish a dc level is called half-wave rectification. The half-wave rectifier utilizes alternate half-cycles of the input sinusoid. For analysis, the circuit of a half-wave rectifier, assuming an ideal diode is shown in the Fig. below.

this occurs, the charge carriers are said to be tunneling through the barrier.

Characteristics of tunnel diode

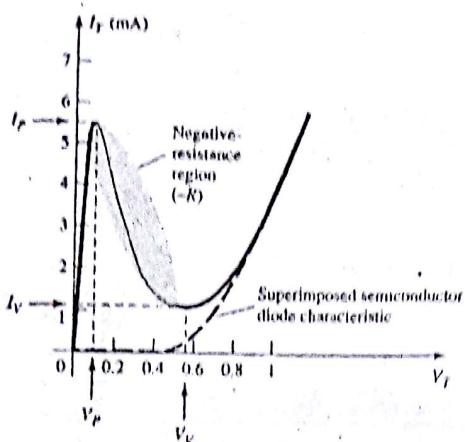


Figure 2.26 Tunnel diode characteristics

A forward biased tunnel diode initially increases forward current with the increase of forward voltage (V_T). Eventually, a peak level of tunneling is reached, and then further increase in forward voltage causes forward current to decrease. The decrease in forward current continues until the normal process of current flows across a forward-biased junction.

Application

Used in high-speed applications such as in computers where switching times in the order of nanoseconds or picoseconds are desirable.

RECTIFIER CIRCUITS

Rectifier is a device used for converting alternating current (AC) to direct current (DC).

1. Half-Wave Rectifier

The process of removing one-half the input signal to establish a dc level is called half-wave rectification. The half-wave rectifier utilizes alternate half-cycles of the input sinusoid. For analysis, the circuit of a half-wave rectifier, assuming an ideal diode is shown in the Fig. below.

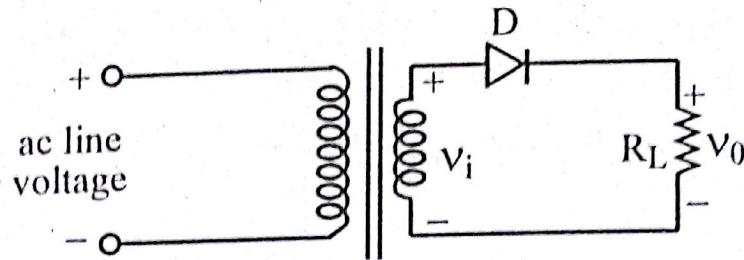


Figure 2.27 Half-wave rectifier

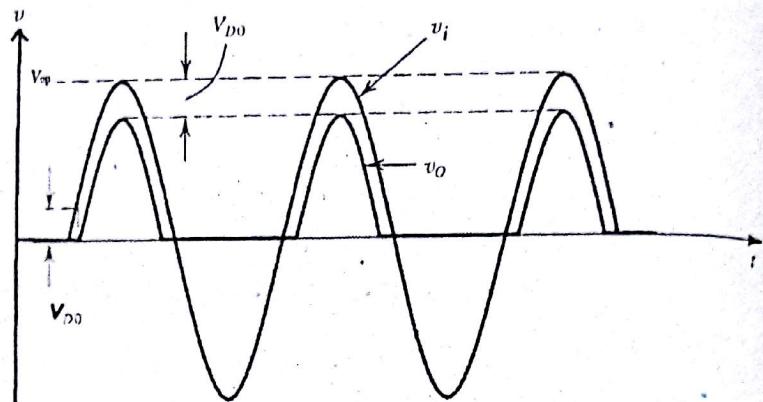


Figure 2.28 Input and output waveforms

During the positive half-cycles of the input voltage, v_i is positive and thus, current is conducted through diode D, and R_L . During the negative half-cycles of the input voltage, v_i will be negative, which makes diode D in reverse-biased condition.

The characteristics of half-wave rectifier can be summarized as follows:

- i. DC output current: $I_{dc} = \frac{I_{op}}{\pi}$
- ii. DC output voltage: $V_{dc} = \frac{V_{op}}{\pi}$
- iii. RMS value of current: $I_{rms} = \frac{I_{op}}{2}$
- iv. RMS value of output voltage: $V_{rms} = \frac{V_{op}}{2}$
- v. Form factor: $K_f = \frac{\text{RMS value}}{\text{Average value}} = 1.57$
- vi. Peak factor: $K_p = \frac{\text{Peak value}}{\text{RMS value}} = 2$

vii. Ripple factor: $\gamma = 1.21$

viii. Rectification efficiency:

$$\eta = \frac{\text{DC power delivered to the load}}{\text{AC input power from the transformer}} = \frac{P_{dc}}{P_{ac}} = 40.6\%$$

The advantages and disadvantages of a half-wave rectifier are given below:

Advantages

- i. Simple circuit and low cost.

Disadvantages

- i. Ripple factor is high, and an elaborate filtering is, therefore, required to give steady dc output.
- ii. The power output, and therefore, rectification efficiency is quite low.
- iii. DC saturation of transformer core resulting in magnetizing current, hysteresis losses and generation of harmonics.

2. Full-Wave Rectifier

The full-wave rectifier utilizes both halves of the input sinusoid. To provide a unipolar output, it inverts the negative halves of the sine wave.

i. Center-tapped transformer full-wave rectifier

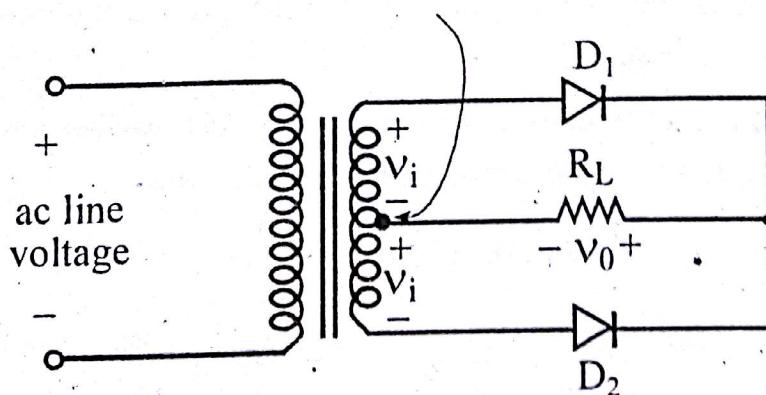


Figure 2.29 Center-tapped transformer full-wave rectifier

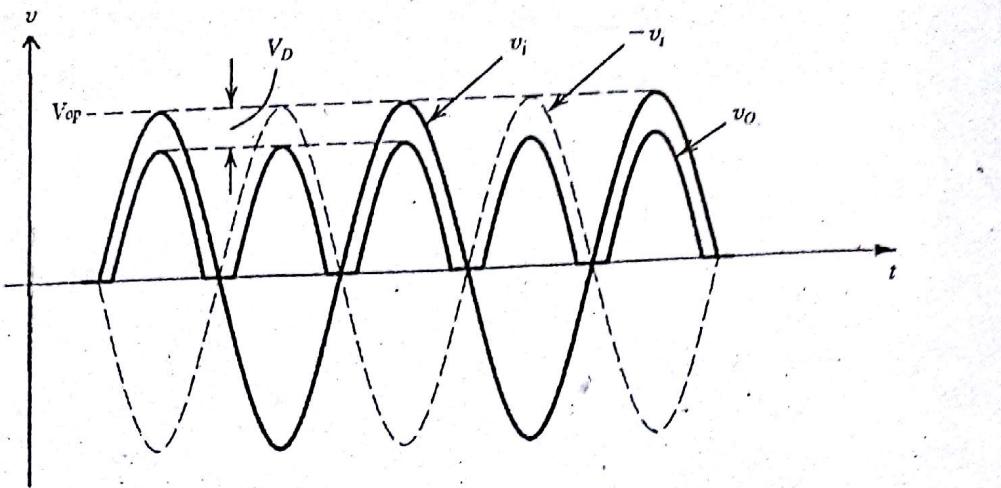


Figure 2.30 Input and output waveforms

As shown in the circuit, the transformer winding is center-tapped to provide two equal voltages v_i across the two halves of the secondary winding with the polarities indicated. During the positive half-cycle of the ac line voltage (primary side), both of the signals labeled v_i will be positive. In this case, D_1 will conduct and D_2 will be reverse biased. The current through D_1 will flow through R_L and back to the center tap of the secondary. During the negative half-cycle of the ac line voltage (primary side), both of the voltages labeled v_i will be negative. Thus, D_1 will be cut off while D_2 will conduct. The current conducted by D_2 will flow through R_L and back to the center tap.

The characteristics of center-tapped transformer full-wave rectifier can be summarized as follows:

- i. DC output current: $I_{dc} = \frac{2I_{op}}{\pi}$
- ii. DC output voltage: $V_{dc} = \frac{2V_{op}}{\pi} = \frac{2I_{op}}{\pi} R_L$
- iii. RMS value of current: $I_{rms} = \frac{I_{op}}{\sqrt{2}}$
- iv. RMS value of output voltage: $V_{rms} = \frac{V_{op}}{\sqrt{2}} = \frac{I_{op}}{\sqrt{2}} R_L$
- v. Form factor: $k_f = 1.11$

- vi. Peak factor: $k_p = \sqrt{2}$
- vii. Ripple factor: $\gamma = 0.482$
- viii. Rectification efficiency: $\eta = 81.2\%$

ii. Full-wave bridge rectifier

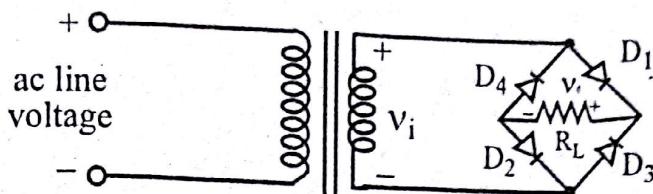


Figure 2.31 Full-wave bridge rectifier

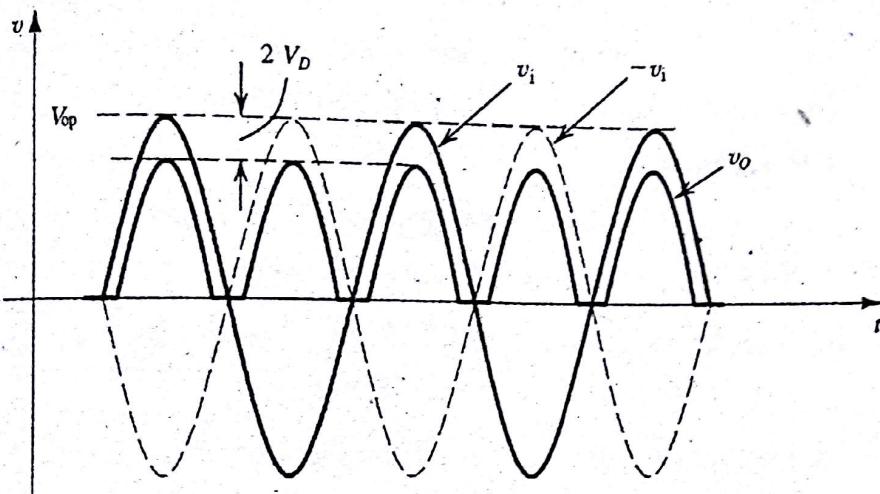


Figure 2.32 Input and output waveform

The bridge rectifier circuit operates as follows: During the positive half-cycles of the input voltage, v_i is positive, and thus, current is conducted through diode D_1 , resistor R , and diode D_2 . Meanwhile, diodes D_3 and D_4 will be reverse biased. During the negative half-cycles of the input voltage, v_i will be negative, and thus $-v_i$ will be positive, forcing current through D_3 , R_L , and D_4 . Meanwhile, diodes D_1 and D_2 will be reverse biased. It should be noted that, during both half-cycles of the input voltage, current flows through R_L in the direction (from right to left).

The characteristics of full-wave bridge rectifiers can be summarized as follows:

- i. DC output current: $I_{dc} = \frac{2I_{op}}{\pi}$

- ii. DC output voltage: $V_{dc} = \frac{2V_{op}}{\pi} = \frac{2I_{op}}{\pi} R_L$
- iii. RMS value of current: $I_{rms} = \frac{I_{op}}{\sqrt{2}}$
- iv. RMS value of output voltage: $V_{rms} = \frac{V_{op}}{\sqrt{2}} = \frac{I_{op}}{\sqrt{2}} R_L$
- v. Form factor: $k_f = 1.11$
- vi. Peak factor: $k_p = \sqrt{2}$
- vii. Ripple factor: $\gamma = 0.482$
- viii. Rectification efficiency: $\eta = 81.2\%$

Now, we will see the advantages and disadvantages of full-wave rectifiers over half-wave rectifiers.

Advantages

- i. The rectification efficiency of a full-wave rectifier is double of that of a half-wave rectifier.
- ii. Ripple factor is low, and so simple filtering circuit is required in a full-wave rectifier.
- iii. Higher output voltage and higher output power in case of a full-wave rectifier.

Disadvantages

- i. Full-wave rectifier needs more circuit elements and is costlier.

RIPPLE VOLTAGE OF CAPACITOR FILTER WHEN CONNECTED ACROSS A RECTIFIER

i. For half-wave rectifier

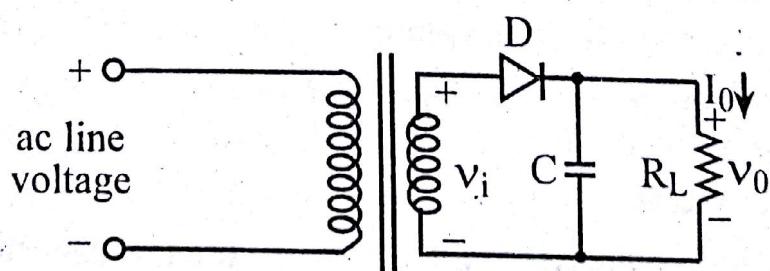


Figure 2.33 Half-wave rectifier with a capacitor filter

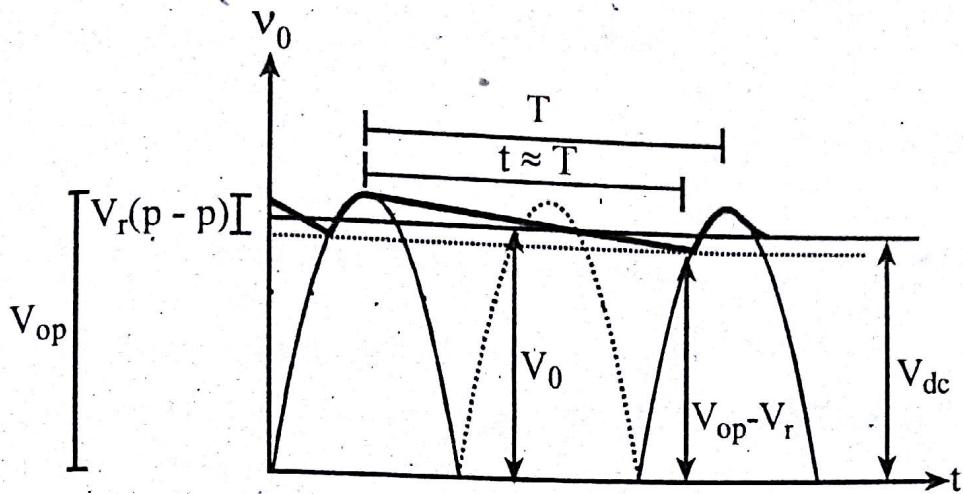


Figure 2.34 Approximate triangular ripple voltage for capacitor filter (in case of half-wave rectifier)

$$V_o = \{V_{op} + (V_{op} - V_r)\} / 2 = V_{op} - \frac{V_r}{2}$$

If $V_r \ll V_{op}$, then $V_0 \approx V_{op}$

The amount of voltage discharge (V_r) in a period of time $t = T$ is given by

$$Q = CV_r = I_0 T; I_0 = \frac{V_0}{R_L}$$

$$\text{or, } CV_r = \frac{V_0}{R_L} \frac{1}{f}$$

$$\therefore V_r = \frac{V_0}{fCR_L} \approx \frac{V_{op}}{fCR_L}$$

where V_r = ripple voltage in peak to peak value.

ii. For full-wave rectifier

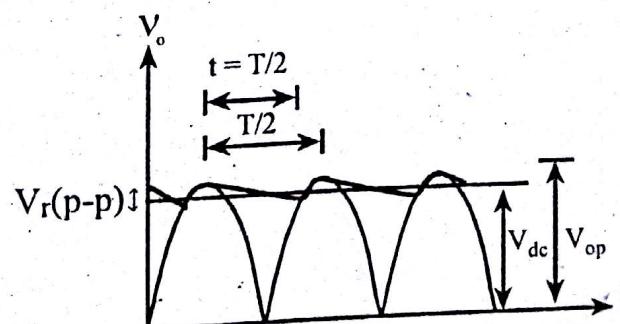


Figure 2.35 Approximate triangular ripple voltage for capacitor filter (in case of full wave rectifier)

$$V_o = \{V_{op} + (V_{op} - V_r)\} / 2$$

$$= V_{op} - \frac{V_r}{2}$$

If $V_r \ll V_{op}$, then $V_o \approx V_{op}$

The amount of voltage discharge (V_r) in a period of time

$t = T$ is given by

$$Q = CV_r = I_0 \frac{T}{2}; I_0 = \frac{V_0}{R_L}$$

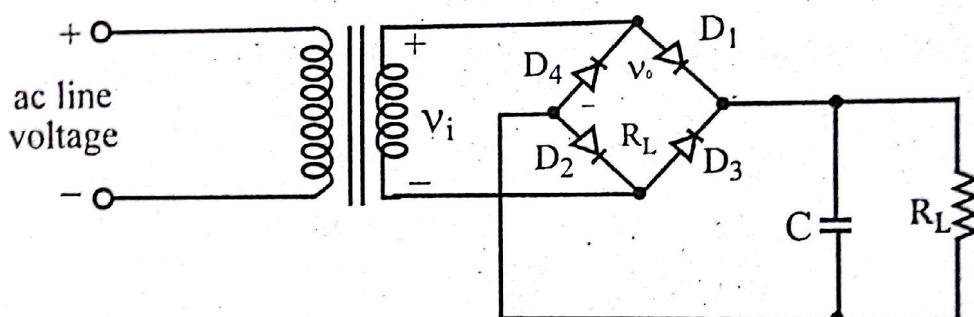
$$\text{or, } CV_r = \frac{V_0}{R_L} \frac{1}{2f}$$

$$\therefore V_r = \frac{V_0}{2fCR_L} \approx \frac{V_{op}}{2fCR_L}$$

Problem 2.18

Express the ripple factor if smoothing capacitor, C is connected to the bridge rectifier circuit. [2007 Chaitra]

Solution:



The ripple factor of a voltage is defined by

$$r = \frac{\text{rms value of ac component of signal}}{\text{average value of signal}}$$

$$= \frac{V_r(\text{rms})}{V_{dc}}$$

$$= \frac{V_r(\text{p-p})}{2\sqrt{3}} \\ = \frac{2\sqrt{3}}{V_{dc}}$$

$$= \frac{V_{op}}{2\sqrt{3}V_{dc}} = \frac{1}{4\sqrt{3}fCR_L} \cdot \frac{V_{op}}{V_{dc}}$$

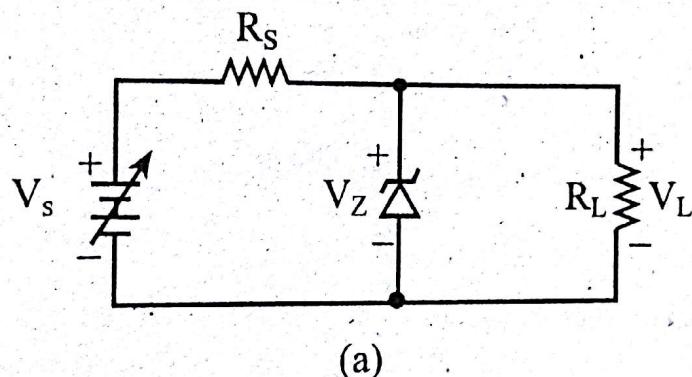
If ripple content is very small, $V_{op} \approx V_{dc}$

$$\therefore r = \frac{1}{4\sqrt{3}fCR_L}$$

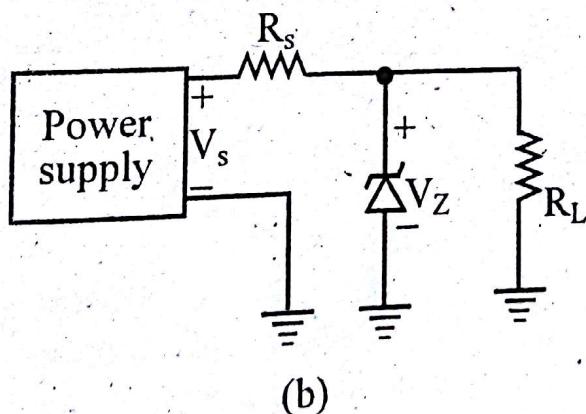
Note: For half-wave rectifier, $r = \frac{1}{2\sqrt{3}fCR_L}$

ZENER VOLTAGE REGULATOR

Figure 2.36 (a) shows a loaded Zener regulator and Figure 2.36 (b) shows the same circuit with grounds. The Zener diode operates in the breakdown region and holds the load voltage constant. Even if the source voltage changes or the load resistance varies, the load voltage will remain fixed and equal to the Zener voltage.



(a)



(b)

Figure 2.36 Loaded Zener regulator: (a) Basic circuit (b) practical circuit

Explanation:

Series current - Assuming that the Zener diode is operating in the breakdown region, the current through the series resistor is given by:

$$I_S = \frac{V_S - V_Z}{R_S}$$

This is Ohm's law applied to the current-limiting resistor. It is the same whether or not there is a load resistor. In other words, if you disconnect the load resistor, the current through the series resistor still equals the voltage across the resistor divided by the resistance.

Load current - Ideally, the load voltage equals the Zener voltage because the load resistor is in parallel with the Zener diode.

As an equation:

$$V_L = V_Z$$

This allows us to use Ohm's law to calculate the load current:

$$I_L = \frac{V_L}{R_L}$$

Zener current - With Kirchhoff's current law:

$$I_S = I_Z + I_L$$

The Zener diode and the load resistor are in parallel. The sum of their currents has to equal the total current, which is the same as the current through the series resistor.

We can rearrange the foregoing equation to get this important formula:

$$I_Z = I_S - I_L$$

This tells you that the Zener current no longer equals the series current, as it does in an unloaded Zener regulator. Because of the load resistor, the Zener current now equals the series current minus the load current.

Working principle

Case I: Regulation when the input source voltage varies

To analyze the working principle, the load resistance (R_L) is kept fixed and the input source voltage (V_S) is varied.

For instance, let's suppose that the V_S increases. This increases I_S , as a result, the current through Zener diode (I_Z) will

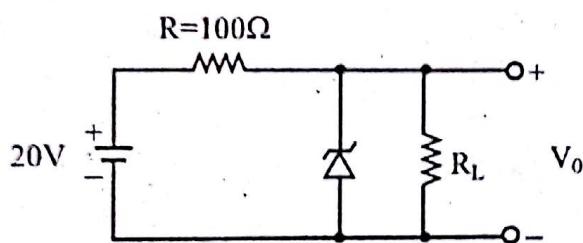
increase without affecting load current (I_L). As I_S has increased, voltage drop across R_S is increased keeping load voltage (V_L) unchanged. Same principle applies when the source voltage decreases.

Case II: Regulation when the load resistance varies

The input source voltage (V_s) is kept fixed and the load resistance (R_L) is varied for analysis. For instance, suppose that R_L decreases. This will increase I_L but decrease I_Z which makes $I_S = I_Z + I_L$ constant. So, voltage drop across R_S is unchanged and hence, the load voltage (V_L) is held constant. Same principle applies when R_L increases.

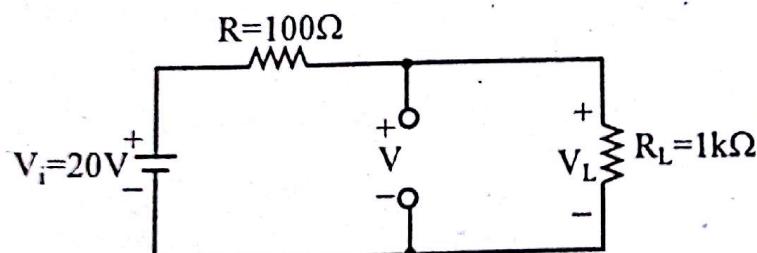
Problem 2.19

Find the Zener current in the following circuit when $R_L = 1\text{ k}\Omega$ and $R_L = 200\text{ }\Omega$. Assume $V_Z = 12\text{ V}$.



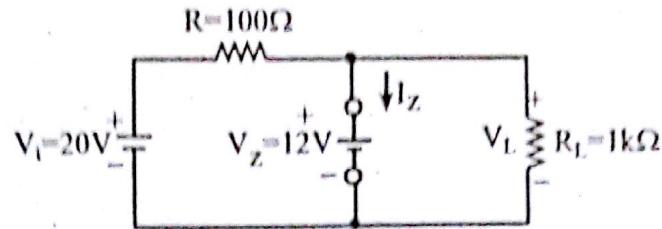
Solution:

- R_L has a fixed value of $1\text{k}\Omega$. Also $V_i = 20\text{ V}$ is fixed. We proceed by determining the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.



$$V = V_L = \left(\frac{R_L}{R + R_L} \right) V_i = \left(\frac{1000}{100 + 1000} \right) \times 20 = 18.18\text{ V}$$

Since $V = 18.18\text{ V}$ is greater than $V_Z = 12\text{ V}$, the diode is in the "on" state and the following network will result.



But $V_L = V_Z = 12 \text{ V}$

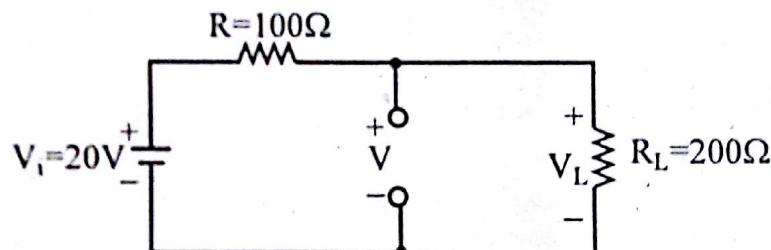
$$V_R = V_i - V_L = 20 - 12 = 8 \text{ V}$$

$$I_L = \frac{V_L}{R_L} = \frac{12}{1000} = 0.012 \text{ A}$$

$$I_R = \frac{V_R}{R} = \frac{8}{100} = 0.08 \text{ A}$$

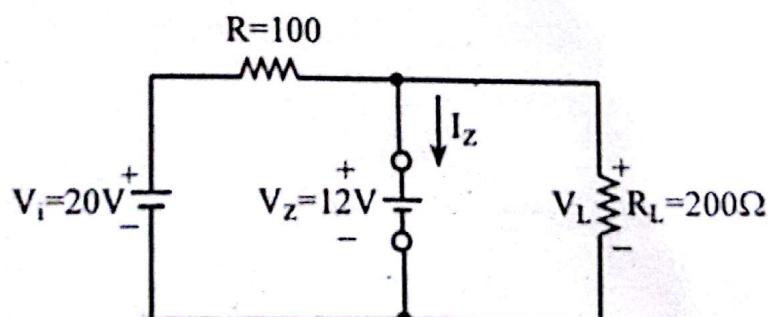
$\therefore I_Z = I_R - I_L = 0.068 \text{ A}$ which is the required Zener current.

- b. R_L has a fixed value of 200Ω . Also $V_i = 20 \text{ V}$ is fixed. We proceed by determining the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.



$$V = V_L \left(\frac{R_L}{R + R_L} \right) V_i = \left(\frac{200}{100+200} \right) \times 20 = 13.333 \text{ V}$$

Since $V = 13.333 \text{ V}$ is greater than $V_Z = 12 \text{ V}$, the diode is in the "on" state and the following network will result.



But $V_L = V_Z = 12 \text{ V}$

$$V_R = V_i - V_L = 20 - 12 = 8 \text{ V}$$

$$I_L = \frac{V_L}{R_L} = \frac{12}{200} = 0.06 \text{ A}$$

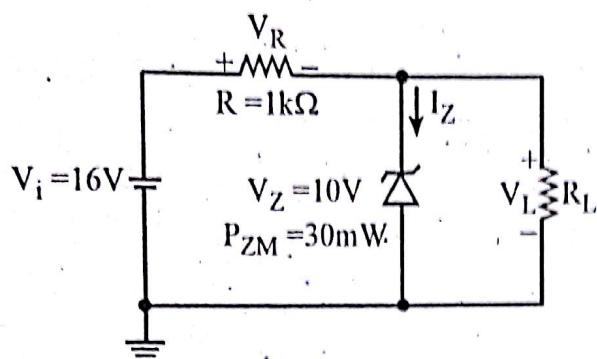
$$I_R = \frac{V_R}{R} = \frac{8}{100} = 0.08 \text{ A}$$

$$\therefore I_Z = I_R - I_L = 0.08 - 0.06$$

= 0.02 A which is the required Zener current.

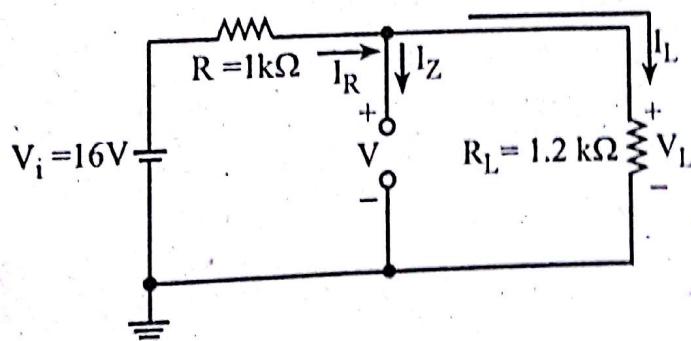
Problem 2.20

For the Zener diode network shown below, determine V_L , V_R , I_Z and P_z for $R_L = 1.2 \text{ k}\Omega$ and $R_L = 3 \text{ k}\Omega$.



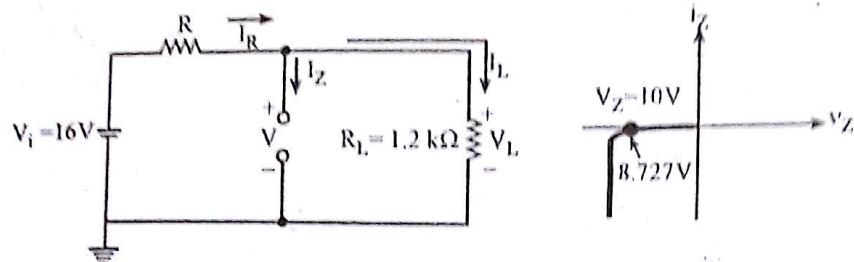
Solution:

- a. R_L has a fixed value of $1.2 \text{ k}\Omega$. Also $V_i = 16\text{V}$ is fixed. We proceed by determining the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.



$$V = V_L = \left(\frac{R_L}{R + R_L} \right) V_i = \left(\frac{1.2}{1 + 1.2} \right) \times 16 = 8.727$$

Since $V = 8.727 \text{ V}$ is less than $V_z = 10\text{V}$, the diode is in the "off" state and the following network will result.



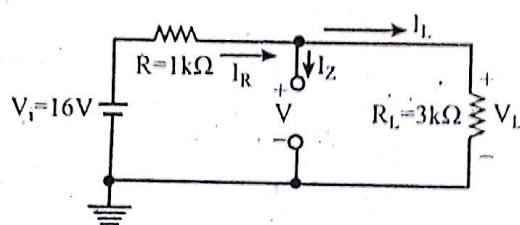
$$V_L = V = 8.727 \text{ V}$$

$$V_R = V_i - V_L = 16 - 8.727 = 7.27 \text{ V}$$

$$I_Z = 0 \text{ A}$$

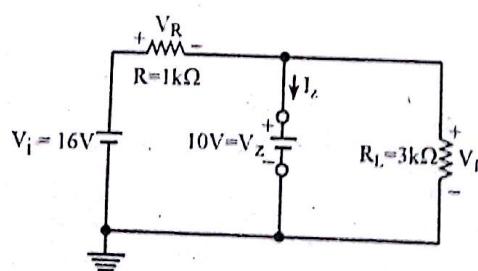
$$P_Z = V_Z I_Z = 0 \text{ W}$$

- b. R_L has a fixed value of $3\text{k}\Omega$. Also $V_i = 16 \text{ V}$ is fixed. We proceed by determining the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.



$$V = V_L = \left(\frac{R_L}{R + R_L} \right) V_i = \left(\frac{3}{1 + 3} \right) \times 16 = 12 \text{ V}$$

Since $V = 12 \text{ V}$ is greater than $V_Z = 10 \text{ V}$, the diode is in the "on" state and the following network will result.



$$V_L = V_Z = 10 \text{ V}, \quad V_R = V_i - V_L = 16 - 10 = 6 \text{ V}$$

$$I_L = \frac{V_L}{R_L} = \frac{10}{3 \times 10^3} = 3.33 \times 10^{-3} \text{ A}$$

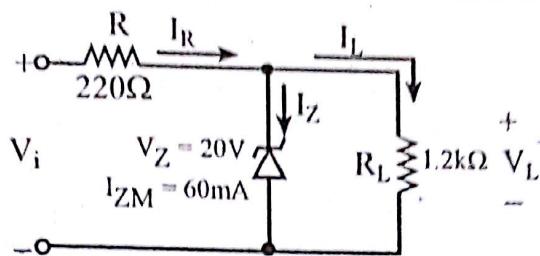
$$I_R = \frac{V_R}{R} = \frac{6}{1 \times 10^3} = 6 \times 10^{-3} \text{ A}$$

$$\therefore I_Z = I_R - I_L = 6 \times 10^{-3} - 3.33 \times 10^{-3} = 2.67 \times 10^{-3} \text{ A}$$

$$P_Z = V_Z I_Z = 10 \times 2.67 \times 10^{-3} = 26.7 \text{ mW} \text{ which is less than the specified } P_{ZM} = 30 \text{ mW.}$$

Problem 2.21

Determine the range of values of V_i that will maintain the Zener diode (see Fig.) in the 'on' state.



Solution:

I_{ZM} = maximum Zener current

V_{imin} = minimum turn-on voltage

V_{imax} = maximum turn-on voltage

$$V_{imin} = \frac{(R_L + R)V_Z}{R_L} = \frac{(1200 + 220)(20)}{1200} = 23.67V$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20}{1.2} = 16.67 \text{ mA}$$

$$I_{Rmax} = I_{ZM} + I_L = 60 + 16.67 = 76.67 \text{ mA}$$

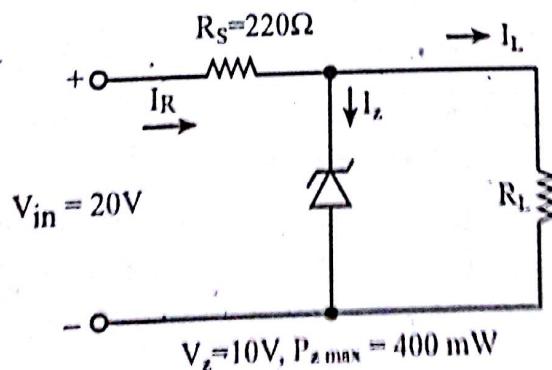
$$V_{imax} = I_{Rmax} R + V_Z = (76.67)(0.22) + 20 = 36.87 \text{ V}$$

Hence, the range of V_i is 23.67 - 36.87 V

Problem 2.22

Determine V_L , I_L , I_Z and I_R for the network shown in figure below for following conditions.

a. If $R_L = 180 \Omega$ b. If $R_L = 470 \Omega$ [2070 Bhadra]



Solution:

[Do it yourself]

TRANSISTORS

INTRODUCTION

The bipolar junction transistor (BJT) is a three-layer semiconductor device which is able to amplify a signal and consists of either two n- and one p- type layers of material or two p- and one n- type layers of material. The former is called an npn transistor, and the latter is called a pnp transistor. It is called "bipolar" because the conduction takes place due to both electrons as well as holes. There are three terminals in the BJT namely the base, the collector, and the emitter.

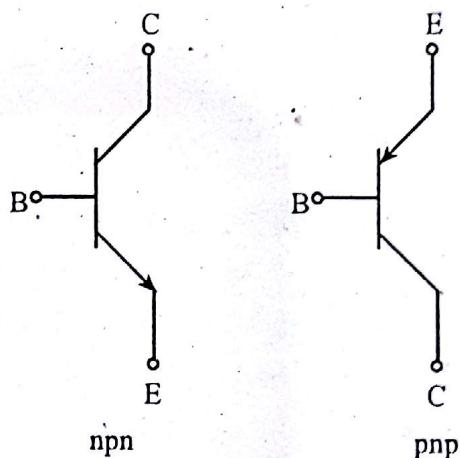
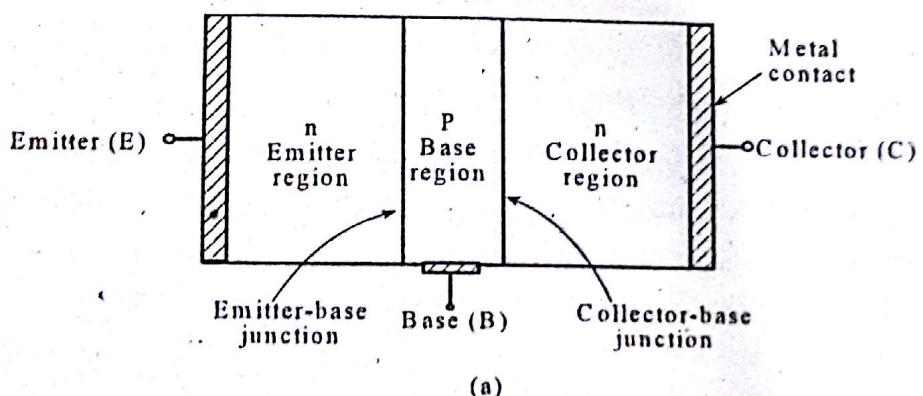


Figure 3.1 Circuit symbols for BJTs

The basic amplifying action of transistor was produced by transferring a current I from a low-to high-resistance circuit. The combination of the two terms in *italics* results in the label *transistor*; that is, transfer + resistor → *transistor*

CONSTRUCTION AND OPERATION OF NPN BJT



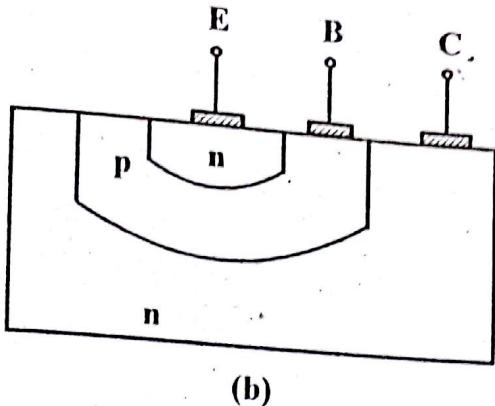


Figure 3.2 (a) Simplified sketch of an npn transistor (b) Cross-section of an npn transistor

As can be seen from **Figure 3.2 (a)**, the BJT is formed from two back-to-back pn junctions: (i) base-emitter junction (ii) base-collector junction. In practice, most of the BJTs are asymmetrically constructed as shown in **Figure 3.2 (b)**. The figure shows that base-collector junction and base-emitter junction have very differently sized surface contact areas. That is, area of base-collector junction is greater than that of base-emitter junction. Emitter region is doped heaviest, collector region is doped moderately, and base region is doped very lightly.

For normal operation (as an amplifier), base-emitter junction is forward biased and base-collector junction is reverse biased. This mode of operation is called active mode of operation.

The forward bias at base-emitter junction reduces its barrier potential (depletion layer is diminished). As a result, electrons from E-region flow into B- region (The electrons are said to be emitted into the base region; hence, the name "emitter"). Holes also flow from p-type B- region into n- type E-region. But because the base is much lightly doped than the emitter, large number of electrons that couldn't recombine with the holes of the base region tend to accumulate in the base region. These electrons behave like minority charge carriers for reverse-biased base-collector junction. Hence, they flow into collector region as minority carrier current. The reverse-biased condition at the base-collector junction causes the base-

collector depletion layer (region) to penetrate deeper into the base region. Thus, the thin base region becomes more thinner. As a result, the electrons emitted from E-region into B-region immediately approach the base-collector junction where large positive collector reverse biased voltage is present, causing almost all these electrons to cross the base-collector junction and flow into collector region as collector current. Due to both of these phenomena, more than 99% of emitter current becomes collector current. Very few electrons only succeed recombining with the holes of the base forming base current. It is only 1% or less of the emitter current.

BETA (β) AND ALPHA (α)

The beta (β) of transistor is defined as the ratio of the dc collector current to the dc base current.

$$\beta = I_C/I_B$$

The beta is also known as the "current gain" because a small base current produces a much larger collector current. For low-power transistor (under 1 W), the current gain is typically 100 to 300. High-power transistors (over 1 W) usually have current gains of 20 to 100.

The alpha (α) of a transistor is defined as the ratio of the dc collector current to the dc emitter current.

$$\alpha = \frac{I_C}{I_E}$$

Since the collector current almost equals the emitter current, the alpha is slightly less than 1. For instance, in a low-power transistor, the alpha is typically greater than 0.99. Even in a high-power transistor, the alpha is typically greater than 0.95.

Relationship between α and β

For any transistor,

$$I_E = I_C + I_B$$

$$\text{or, } \frac{I_E}{I_C} = 1 + \frac{I_B}{I_C}$$

Since $\alpha = \frac{I_C}{I_E}$ and $\beta = \frac{I_C}{I_B}$, we have

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

Simplification will yield

$$\alpha = \frac{\beta}{\beta + 1}, \quad \beta = \frac{\alpha}{1 - \alpha}$$

BJT BIASING

For a transistor to work properly, it should be biased adequately. The purpose of biasing is to establish a proper working point (quiescent or Q-point) of the transistor circuit. Biasing provides a proper voltage across emitter-base junction and base-collector junction so that a constant and required dc collector (emitter) current is established.

i. Emitter-feedback bias

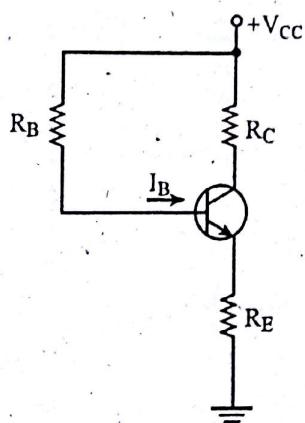


Figure 3.3 Emitter-feedback bias

Historically, the first attempt at stabilizing the Q point was emitter-feedback bias, shown in Figure 3.3.

Notice that an emitter resistor has been added to the circuit. The basic idea is this: If I_c increases, V_E increases, causing V_B to increase. More V_B means less voltage across R_B . This results in less I_B , which opposes the original increase in I_c . It's called feedback because the change in emitter voltage is being fed back to the base circuit. Also, the feedback is called negative because it opposes the original change in collector current.

current. Emitter-feedback bias never became popular. The movement of the Q point is still too large for most applications that have to be mass-produced. Here are the equations for analyzing the emitter-feedback bias:

$$I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta}$$

$$V_E = I_E R_E$$

$$V_B = V_E + 0.7V$$

$$V_C = V_{CC} - I_C R_C$$

ii. Collector-feedback bias

Figure 3.4 shows collector-feedback bias (also called self-bias). Historically, this was another attempt at stabilizing the Q point. Again, the basic idea is to feed back a voltage to the base in an attempt to neutralize any change in collector current.

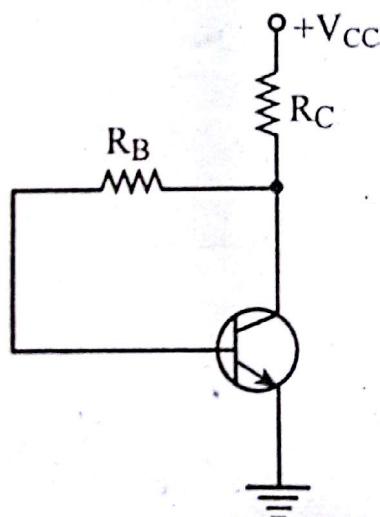


Figure 3.4 Collector-feedback bias

For instance, suppose the collector current increases. This decreases the collector voltage, which decreases the voltage across the base resistor. In turn, this decreases the base current, which opposes the original increase in collector current. Like emitter-feedback bias, collector-feedback uses negative feedback in an attempt to reduce the original change in collector current. Here are the equations for analyzing collector-feedback bias:

$$I_E = \frac{V_{CC} - V_{BE}}{R_e + R_B/\beta}$$

$$V_B = 0.7V$$

$$V_C = V_{CC} - I_C R_C$$

The Q point is usually set near the middle of the load line by using a base resistance of:

$$R_B = \beta R_C$$

iii. Collector- and emitter-feedback bias

Emitter-feedback bias and collector-feedback bias were the first steps toward a more stable bias for transistor circuits. Even though the idea of negative feedback is sound, these circuits fall short because there is not enough negative feedback to do the job. This is why the next step in biasing was the circuit shown in **Figure 3.5**.

The basic idea is to use both emitter and collector feedback to try to improve the operation.

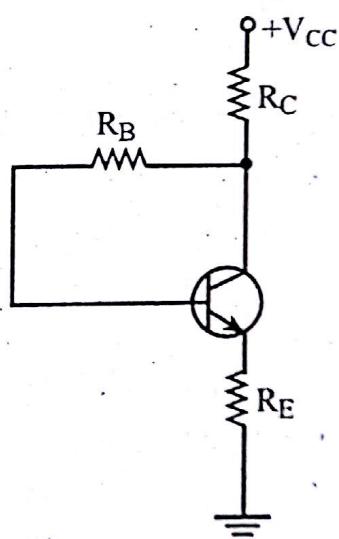


Figure 3.5 Collector-emitter feedback bias

As it turns out, more is not always better. Combining both types of feedback in one circuit helps but still falls short of the performance needed for mass production. Here are the equations for analyzing it.

$$I_E = \frac{V_{CC} - V_{BE}}{R_e + R_E + R_B/\beta}$$

$$V_E = I_E R_E$$

$$V_B = V_E + 0.7V$$

$$V_C = V_{CC} - I_C R_C$$

iv. Voltage-divider bias

Figure 3.6 shows the most widely used biasing circuit. Notice that the base circuit contains a voltage divider (R_1 and R_2). Because of this, this circuit is called voltage-divider bias (VDB).

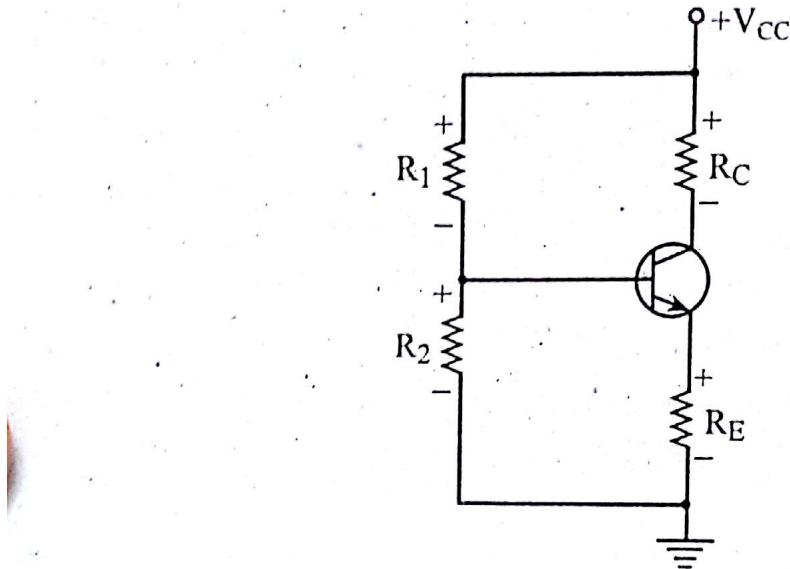
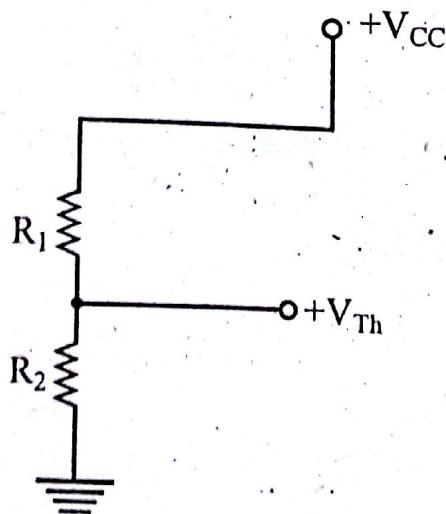


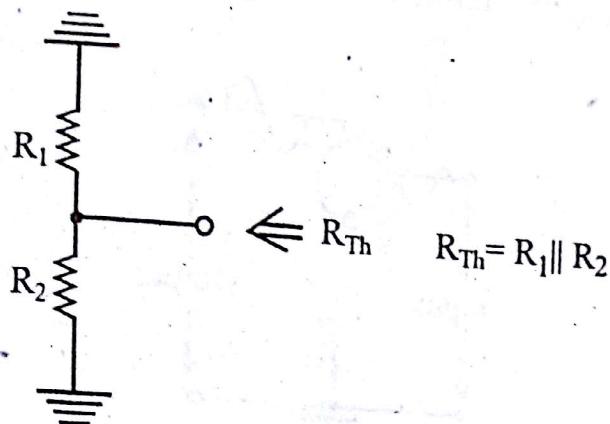
Figure 3.6 Voltage-divider bias

In any well-designed VDB circuit, the base current is much smaller than the current through the voltage divider. Since the base current has a negligible effect on the voltage divider, we can mentally open the connection between the voltage divider and the base to get the equivalent circuit as shown.

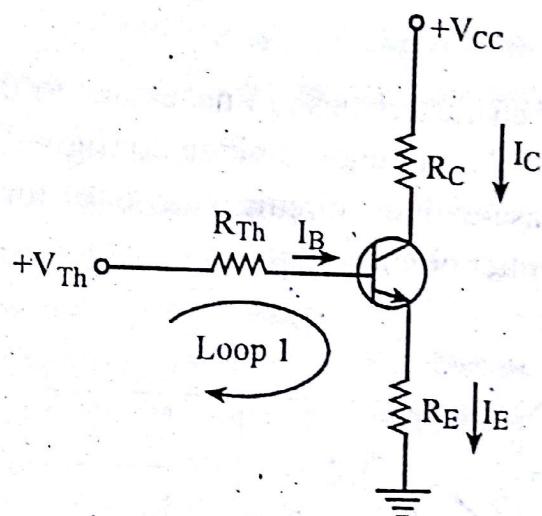


$$V_{Th} = \left(\frac{R_2}{R_1 + R_2} \right) \times V_{CC}$$

Looking back into the voltage divider with V_{CC} grounded, we see R_1 in parallel with R_2 .



Finally, the circuit with its Thevenin's equivalent is



Applying KVL in loop 1,

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$\text{or, } V_{Th} - \frac{I_E}{(\beta + 1)} R_{Th} - V_{BE} - I_E R_E = 0$$

$$\therefore I_E = \frac{V_{Th} - V_{BE}}{R_E + R_{Th}/(\beta + 1)}$$

BJT CONFIGURATION

(1) Common-emitter configuration

It is the most frequently encountered transistor configuration. It is used in about 90 to 95 percent of all transistor applications. Its

application areas include preamplifier and power amplifier circuits. It is called the "common-emitter configuration" because the emitter is common or reference to both the input and output terminals (in this case, common to both the base and collector terminals).

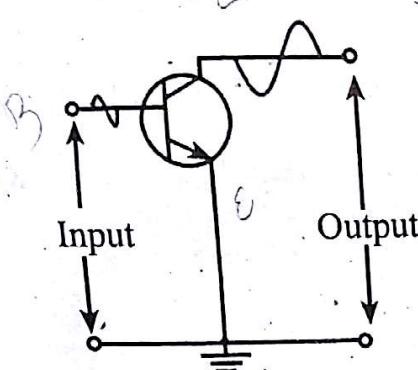
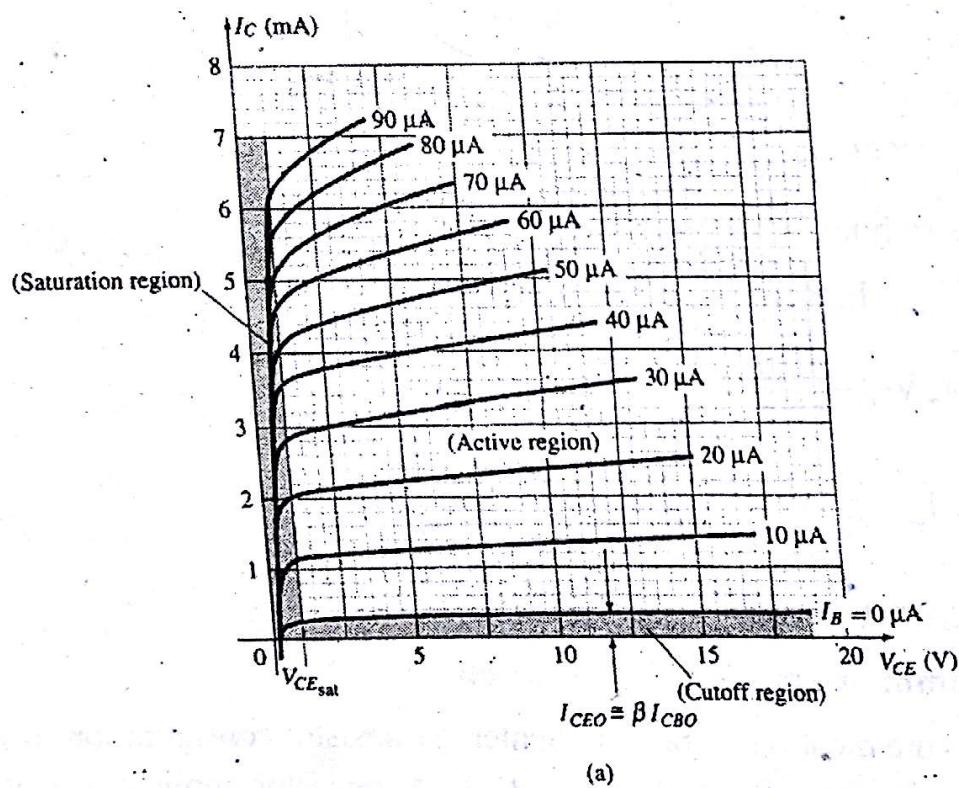
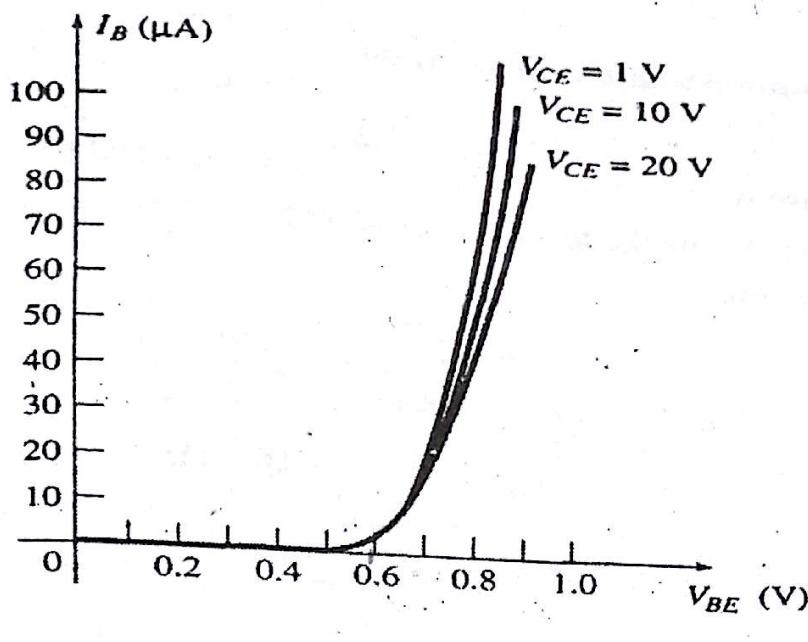


Figure 3.7 Common-emitter configuration (npn transistor)

Two sets of characteristics are necessary to describe fully the behaviour of the common-emitter configuration: one for the input or base-emitter circuit and one for the output or collector-emitter circuit.



(a)



(b)

Figure 3.8 Characteristics of a silicon transistor in the common-emitter configuration: (a) output characteristics (b) input characteristics

For the common-emitter configuration, the output characteristics are a plot of the output current (I_C) versus output voltage (V_{CE}) for a range of values of input current (I_B). The input characteristics are a plot of the input current (I_B) versus the input voltage (V_{BE}) for a range of values of output voltage (V_{CE}).

The active region for the common-emitter configuration is that portion of the upper-right quadrant that has the greatest linearity, that is, that region in which the curves for I_B are nearly straight and equally spaced. In Figure 3.8 (a), this region exists to the right of the vertical dashed line at $V_{CE}(\text{sat})$ and above the curve for I_B equal to zero. The region to the left of $V_{CE}(\text{sat})$ is called the saturation region.

The active region of the common-emitter configuration can be employed for voltage, current, or power amplification. The cutoff region is the region between $I_B = 0 \mu\text{A}$ and the V_{CE} -axis. This region (below $I_B = 0 \mu\text{A}$) is to be avoided if an undistorted output signal is required.

(2) Common-base configuration

In this configuration, input is applied between emitter and base while output is taken across collector and base. Thus, the base forms the terminal common to both the input and output circuits.

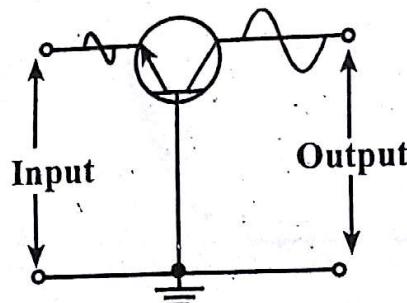
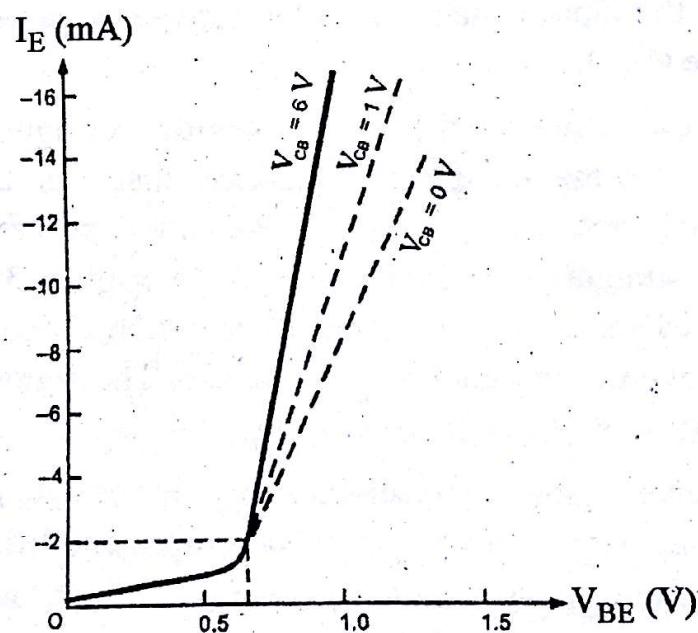
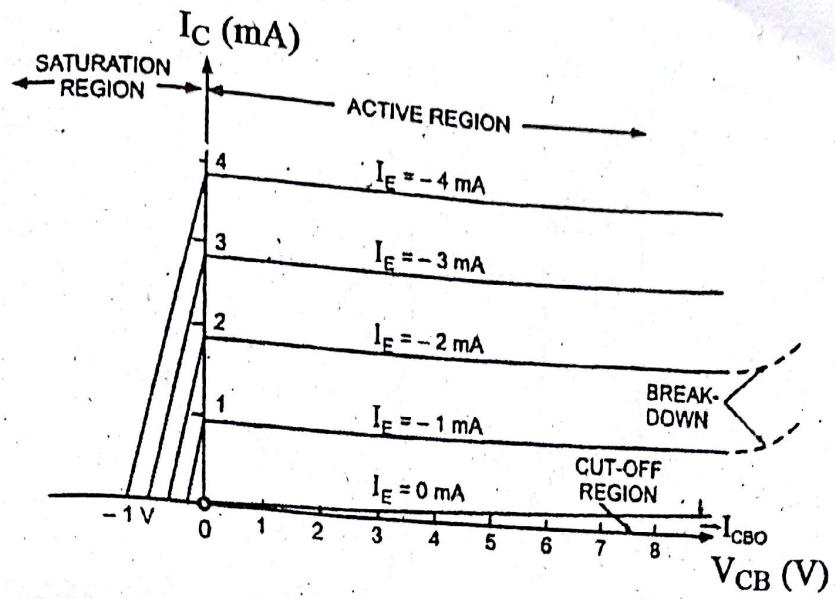


Figure 3.9 Common-base configuration (npn transistor)

Two sets of characteristic are required to explain the nature of common-base configuration: input characteristic curve and output characteristic curve. The curve drawn between emitter current I_E and base-emitter voltage V_{BE} for a given value of collector-base voltage V_{CB} is known as input characteristic. While the curve drawn between collector current I_C and collector-base voltage V_{CB} for a given value of emitter current I_E is known as output characteristic.



(a)



(b)

Figure 3.10 Characteristic curves: (a) Input characteristics (b) Output characteristics

(3) Common-collector configuration

In this circuit arrangement, input is applied between base and collector while the output is taken across emitter and collector. Thus, the collector forms the terminal common to both the input and output circuits.

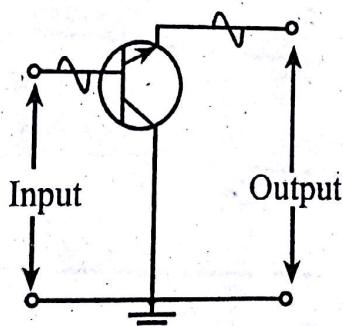
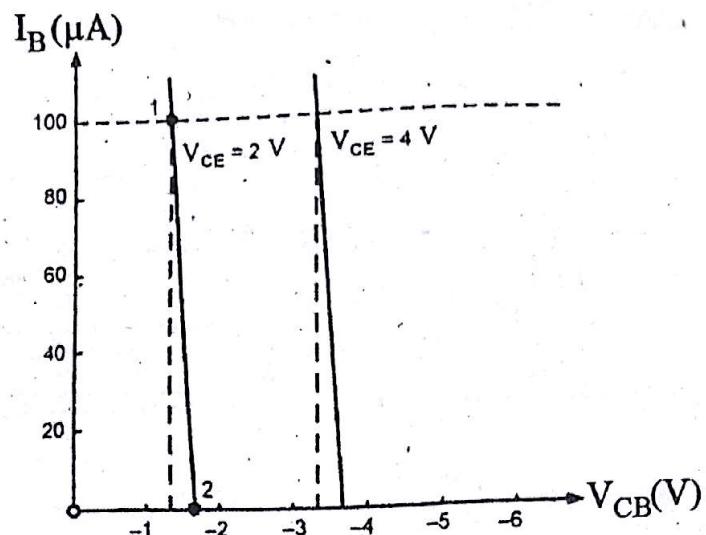


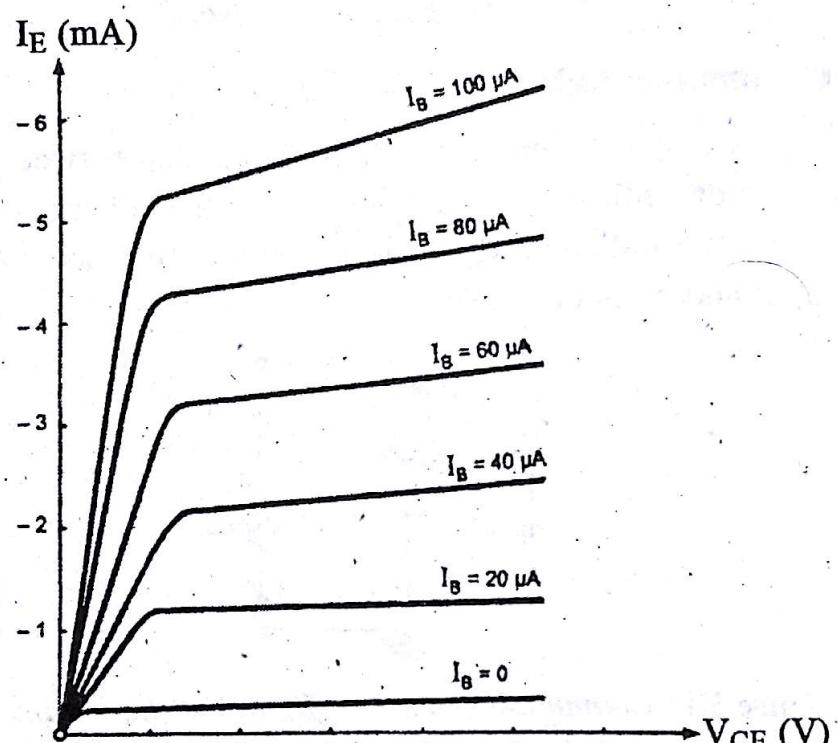
Figure 3.11 Common-collector configuration (npn transistor)

The performance of transistor can be determined from two characteristic curves: input characteristic curve and output characteristic curve. The curve drawn between base current I_B and collector-base voltage V_{CB} for a given value of collector-emitter voltage V_{CE} is known as input characteristic. While the curve drawn between emitter current I_E and collector-emitter

voltage V_{CE} for a given value of base current I_B is known as output characteristic.



(a)



(b)

Figure 3.12 Characteristic curves: (a) Input characteristics (b) Output characteristics

DIFFERENT MODES OF OPERATION OF BJT

The following table illustrates the different BJT modes of operation. EBJ stands for emitter-base junction and CBJ stands for collector-base junction.

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Reverse active	Reverse	Forward
Saturation	Forward	Forward

Table 3.1 BJT modes of operation

BJT SWITCH AND LOGIC CIRCUITS

i. The BJT Inverter (Transistor Switch)

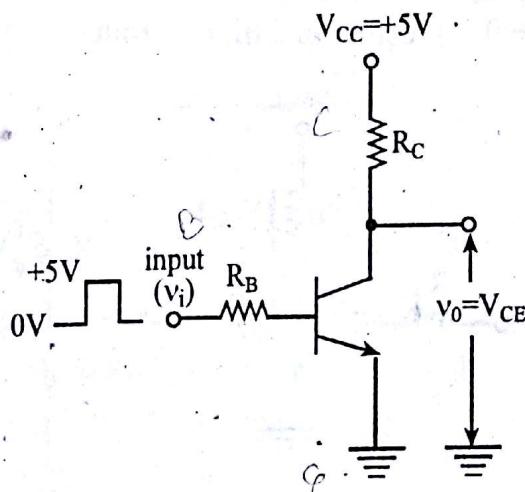


Figure 3.13 An npn transistor inverter or switch

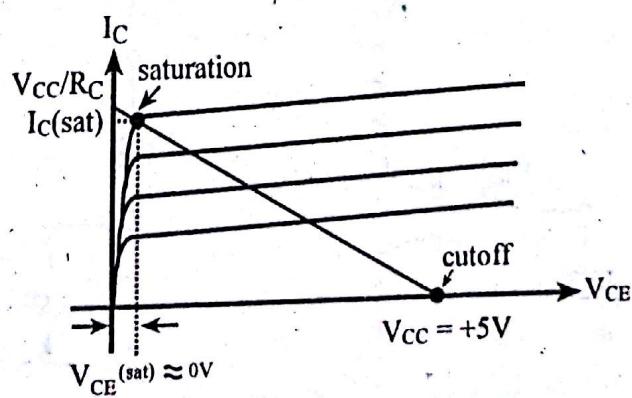


Figure 3.14 A load line plotted on I_C versus V_{CE} characteristics

Consider an npn transistor inverter as shown in the Figure 3.13 above. When the input to the transistor is high (+ 5 V), the base-emitter junction is forward biased and current flows through R_B into the base. The values of R_B and R_C are chosen (designed) so that the amount of base current flowing is enough to saturate the transistor. Note that the value of V_{CE} corresponding to a point in the saturation region, called $V_{CE}(\text{sat})$ is very nearly 0 (typically about 0.1V). When the transistor is saturated, it is said to be ON. The conclusion reached is: A high input to the inverter (+5 V) results in a low output (≈ 0 V).

When the input to the transistor is low (0 V), the base-emitter junction has no forward bias applied to it, so no base current, and hence, no collector current flows. There is therefore, no voltage drop across R_C , and it follows that V_{CE} must be the same as V_{CC} : +5 V. In this situation, the transistor is in the cutoff region. The conclusion reached is: A low input to the inverter (+ 0 V) results in a high output (+ 5 V).

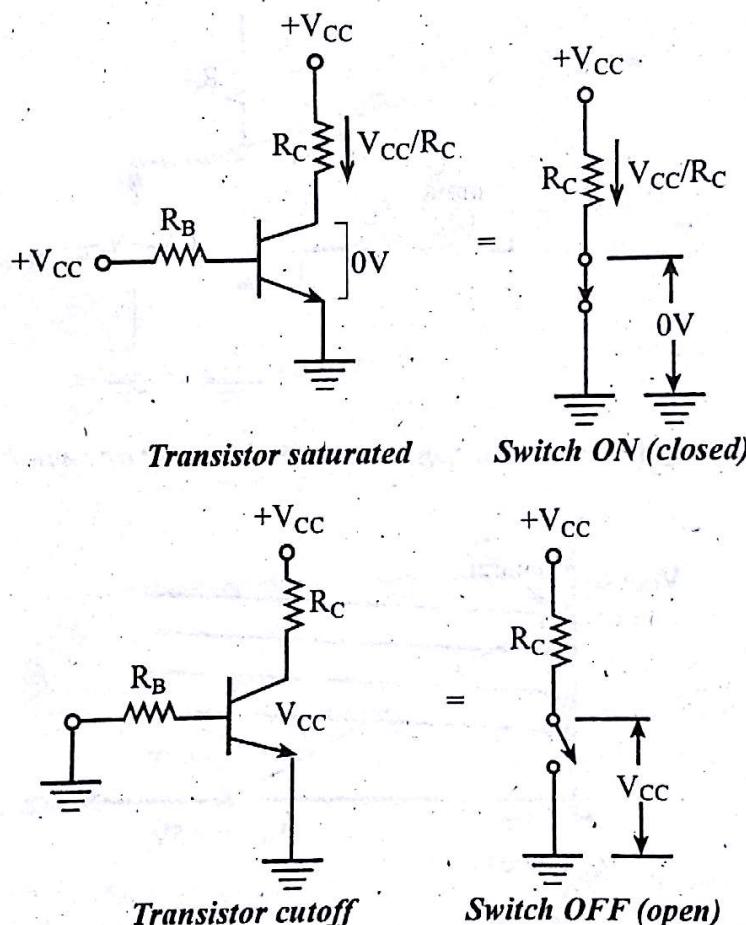


Figure 3.15 The transistor as a voltage-controlled switch. A high input closes the switch and a low input opens it.

ii. OR gate

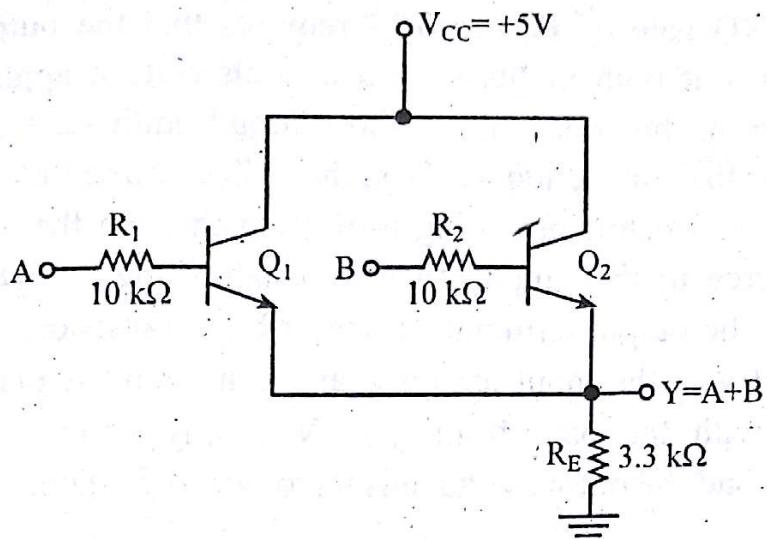


Figure 3.16 OR gate

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Table 3.2 Truth table

If both A and B of the OR gate of Figure 3.16 have a low or 0V input, both transistors are off (cutoff), and the impedance between the collector and the emitter of each transistor can be approximated by an open circuit. Mentally replacing both transistors by open circuits between the collector and the emitter will remove any connection between the applied bias of 5V and the output. The result is zero current through each transistor and through the 3.3 kΩ resistor. The output voltage is therefore 0V or "low". On the other hand, if transistor Q₁ is on and Q₂ is off due to a positive voltage at the base of Q₁ and 0V at the base of Q₂, then the short-circuit equivalent between the collector and emitter for transistor Q₁ can be applied, and the voltage at the output is 5V or "high". Finally, if both transistors are turned on by a positive voltage applied to the base of each, they will both ensure that the output voltage is 5V or "high".

iii. AND gate

The AND gate of Figure 3.17 requires that the output be high only if both inputs have a turn-on voltage applied. If both are in the "on" state, a short-circuit equivalent can be used for the connection between the collector and the emitter of each transistor, providing a direct path from the applied 5V source to the output, thereby establishing a high or 1 state at the output terminal. If one or both transistors are off due to 0V at the input terminal, an open circuit is placed in series with the path from the 5V supply voltage to the output, and the output voltage is 0V or an "off" state.

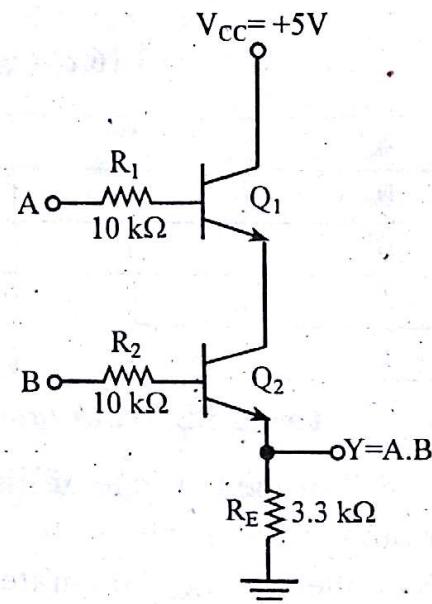


Figure 3.17 AND gate

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Table 3.3 Truth table

iv. NOR gate

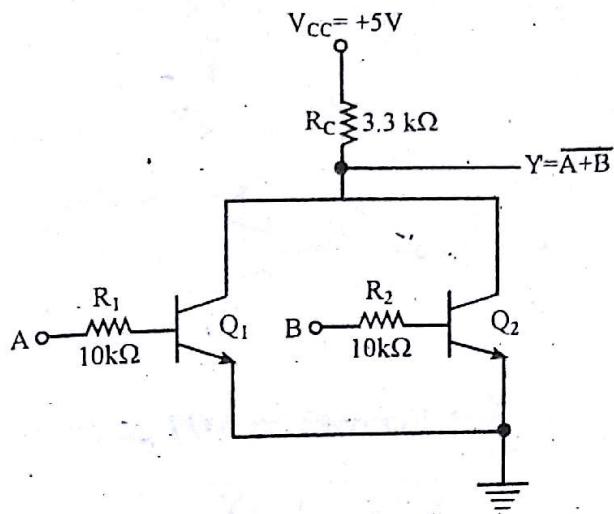


Figure 3.18 NOR gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Table 3.4 Truth table

v. NAND gate

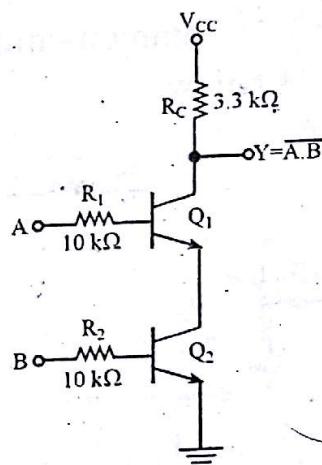


Figure 3.19 NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Table 3.5 Truth table

vi. NOT gate

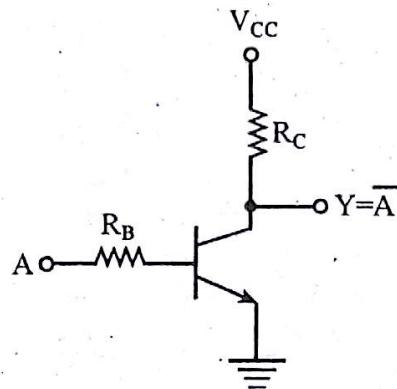


Figure 3.20 NOT gate

A	Y
0	1
1	0.

Table 3.6 Truth table

TRANSISTOR MODELING

A model is a combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.

Consider a circuit in common-emitter configuration as shown in the Figure 3.21 below.

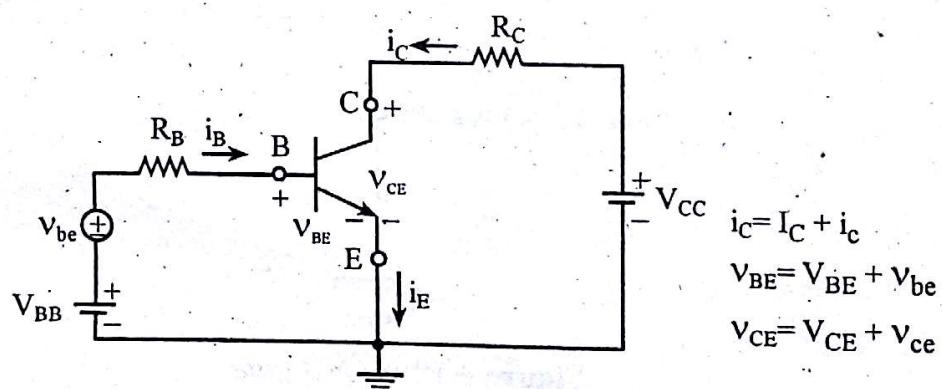


Figure 3.21 Conceptual circuit to illustrate the operation of the transistor as an amplifier

i. DC analysis (Large signal model)

For DC analysis, all the AC components are removed (here, v_{in} is replaced by a short circuit).

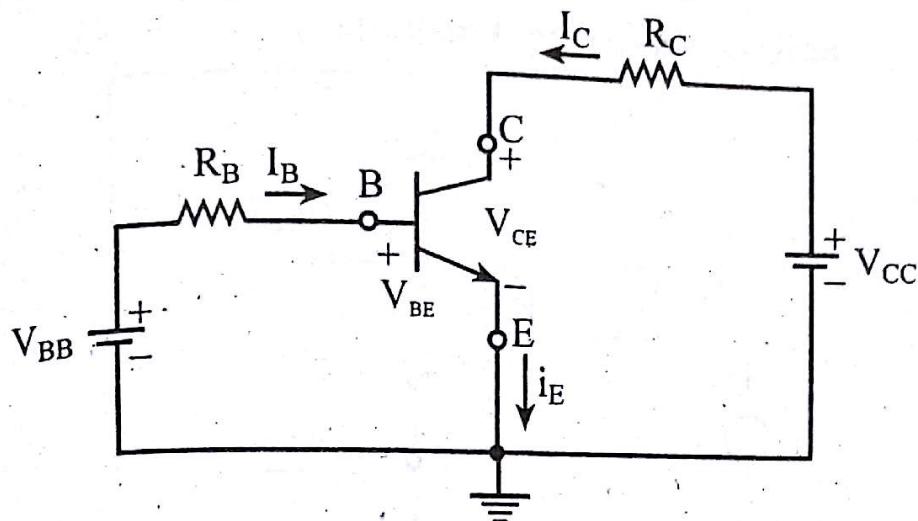


Figure 3.22 Circuit for DC analysis

Looking through the base terminal (B), we notice a forward biased diode between base (B) and emitter (E) and the current I_B flows into the terminal. Looking at the collector terminal, we see that current I_C flows into the terminal.

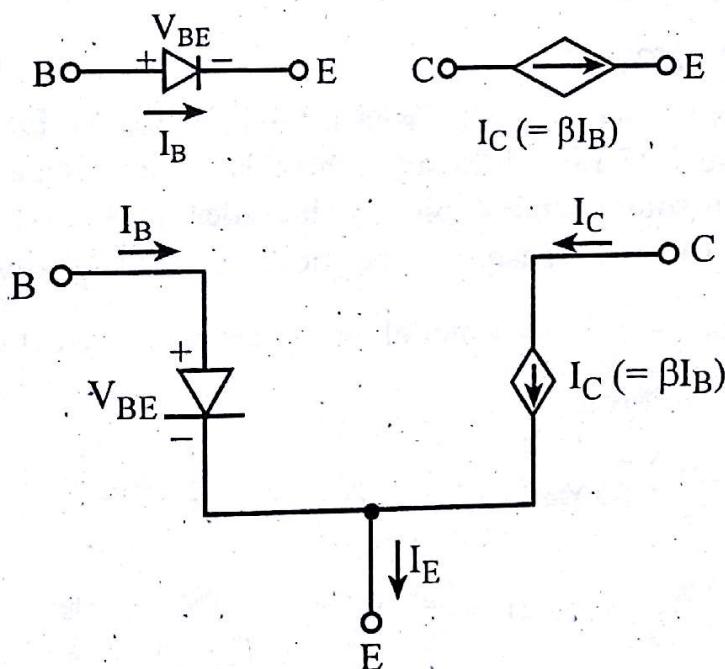


Figure 3.23 Large signal model [DC (bias) equivalent circuit]

ii. AC analysis (small signal model)

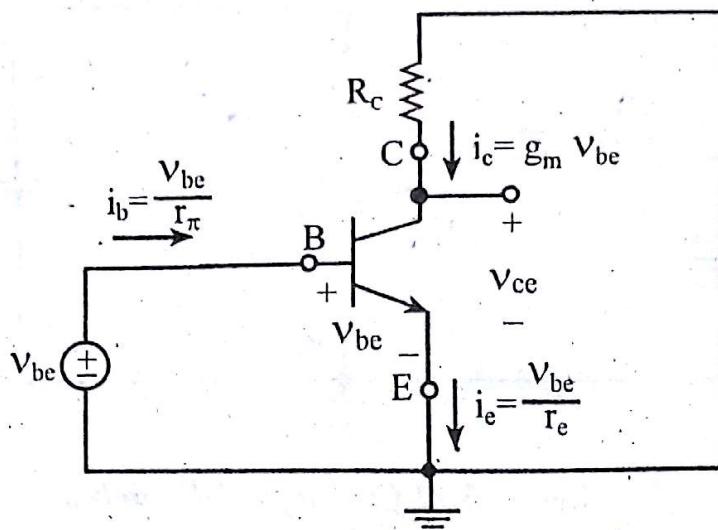


Figure 3.24 Small signal model (AC equivalent circuit)

For AC analysis, we eliminate (short circuit) the DC sources and thus, only the signal components are present. Note that, this is a representation of the signal operation of the BJT and not an actual amplifier circuit.

THE HYBRID- π MODEL

This is the most widely used model for the BJT. The model (**Figure 3.25 (a)**) represents the BJT as a voltage-controlled current source and explicitly includes the input resistance looking into the base, r_π . The model obviously yields $i_c = g_m v_{be}$ and $i_b = \frac{v_{be}}{r_\pi}$. This model also yields the correct expression for i_e as follows:

$$\begin{aligned} i_e &= \frac{v_{be}}{r_\pi} + g_m v_{be} \\ &= \frac{v_{be}}{r_\pi} (1 + g_m r_\pi) = \frac{v_{be}}{r_\pi} (1 + \beta) = \frac{v_{be}}{\left(\frac{r_\pi}{1+\beta}\right)} = \frac{v_{be}}{r_e} \end{aligned}$$

A slightly different equivalent circuit model (**Figure 3.25 (b)**) can be obtained by expressing the current of the controlled source ($g_m v_{be}$) in terms of the base current i_b as follows:

$$g_m v_{be} = g_m (i_b r_\pi) = (g_m r_\pi) i_b = \beta i_b$$

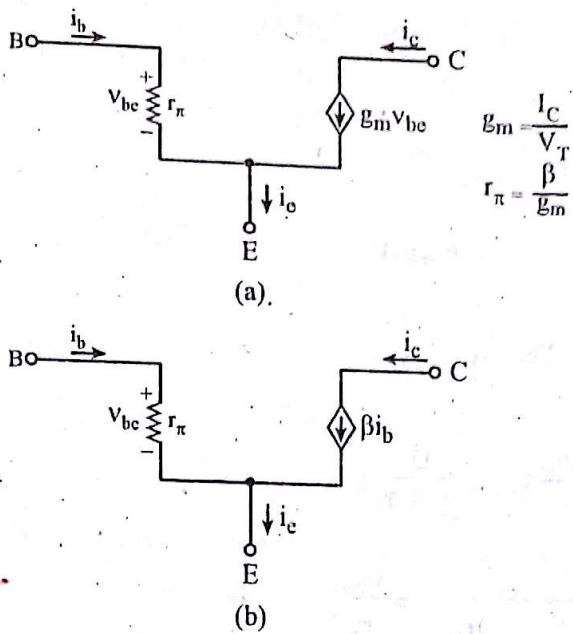


Figure 3.25 Two slightly different versions of the simplified hybrid- π model for the small-signal operation of the BJT. The equivalent circuit in (a) represents the BJT as a voltage-controlled current source (a transconductance amplifier), and in (b) represents the BJT as a current-controlled current source (a current amplifier).

THE T MODEL

Although the hybrid- π model can be used to carry out small-signal analysis of all transistor circuits, there are situations in which an alternative model, called the T model, is much more convenient.

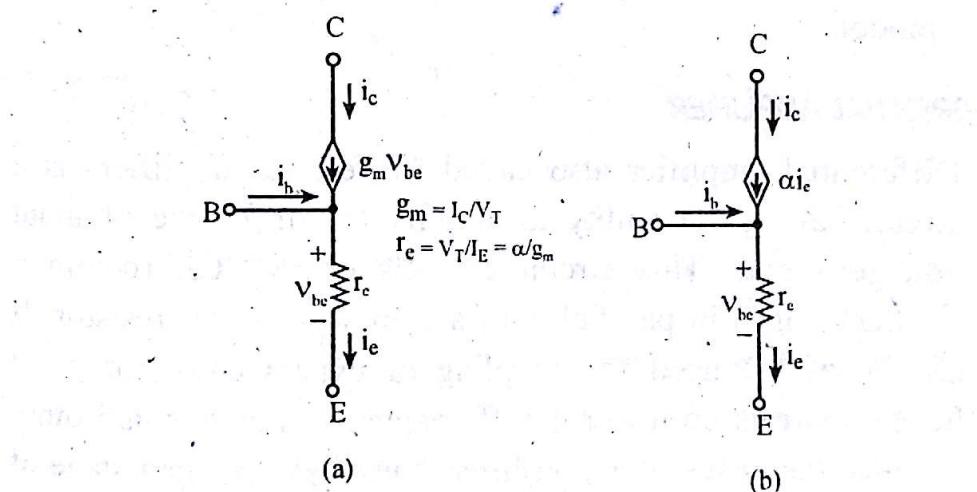


Figure 3.26 Two slightly different versions of the T model of the BJT. The circuit in (a) is a voltage-controlled current source representation, and in (b) is a current-controlled current source representation.

The value of i_b is expressed as

$$\begin{aligned} i_b &= \frac{v_{be}}{r_e} - g_m v_{be} \\ &= \frac{v_{be}}{r_e} (1 - g_m r_e) \\ &= \frac{v_{be}}{r_e} (1 - \alpha) \\ &= \frac{v_{be}}{r_e} \left(1 - \frac{\beta}{\beta + 1}\right) \\ &= \frac{v_{be}}{(\beta + 1)r_e} = \frac{v_{be}}{r_\pi} \end{aligned}$$

If in the model of **Figure 3.26 (a)**, the current of the controlled source is expressed in terms of the emitter current as follows:

$$\begin{aligned} g_m v_{be} &= g_m (i_e r_e) \\ &= (g_m r_e) i_e = \alpha i_e \end{aligned}$$

we obtain the alternative T model (see **Figure 3.26 (b)**).

Both of these models explicitly show the emitter resistance r_e rather than the base resistance r_π featured in the hybrid- π model.

DIFFERENTIAL AMPLIFIER

Differential amplifier also called "difference amplifier" is a circuit having the ability to amplify the difference of input voltage signal. This circuit consists of two CE (common emitter) stages in parallel with a common emitter resistor. It eliminates the need for coupling or bypass capacitors, and hence, there is no lower cutoff frequency. For this and other reasons, the differential amplifier is used as the input stage of almost every IC op-amp.

Ideally, the circuit (see **Figure 3.27**) has identical transistors that remain biased in forward active region, and equal collector resistors. The two base terminals are the two signal

inputs v_{i1} and v_{i2} . The two collector terminals are the two outputs v_{o1} and v_{o2} . The basic relationship between the input and output in differential amplifier is

$$v_{o1} - v_{o2} = -A (v_{i1} - v_{i2})$$

where A is the differential voltage gain of the amplifier.

The ac output voltage is defined as the voltage between the collectors with the polarity shown i.e.,

$$v_{\text{out}} = v_{o2} - v_{o1} = A (v_{i1} - v_{i2})$$

Input v_{i1} is referred to as a "non-inverting input" as a positive voltage v_{i1} acting alone provides a positive output voltage. Similarly, input v_{i2} acting alone provides a negative output voltage, and is therefore, called "inverting input". Consequently, the base terminal to which v_{i1} is impressed is known as "non-inverting terminal" and the base terminal to which v_{i2} is applied is known as "inverting terminal".

Note: Here, ac voltages also includes 0 Hz as a special case.

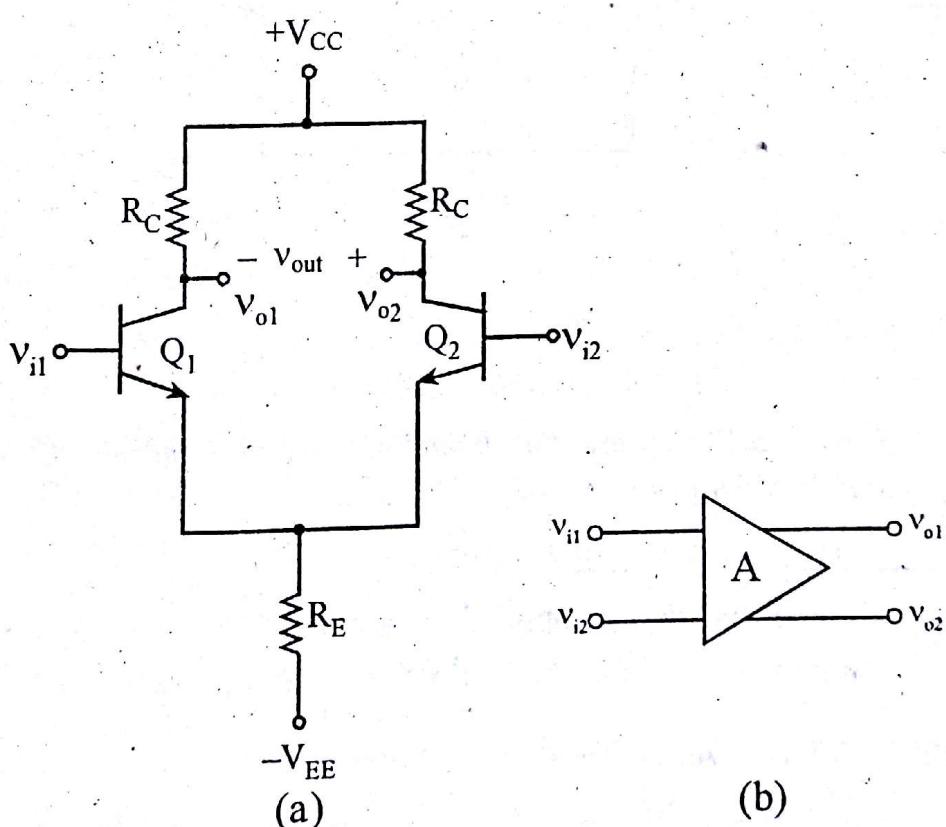


Figure 3.27 (a) Basic differential amplifier circuit (b) schematic symbol

There are three configurations of a differential amplifier.

Case-I: Single-ended input

If a signal is applied to either input with other input connected to ground, the operation is referred to as single-ended input.

Case-II: Double-ended (differential) input

If opposite-polarity signals are applied to inputs, the operation is referred to as double-ended or differential mode input. The waveform at the collector terminals for sinusoidal differential inputs is depicted below.

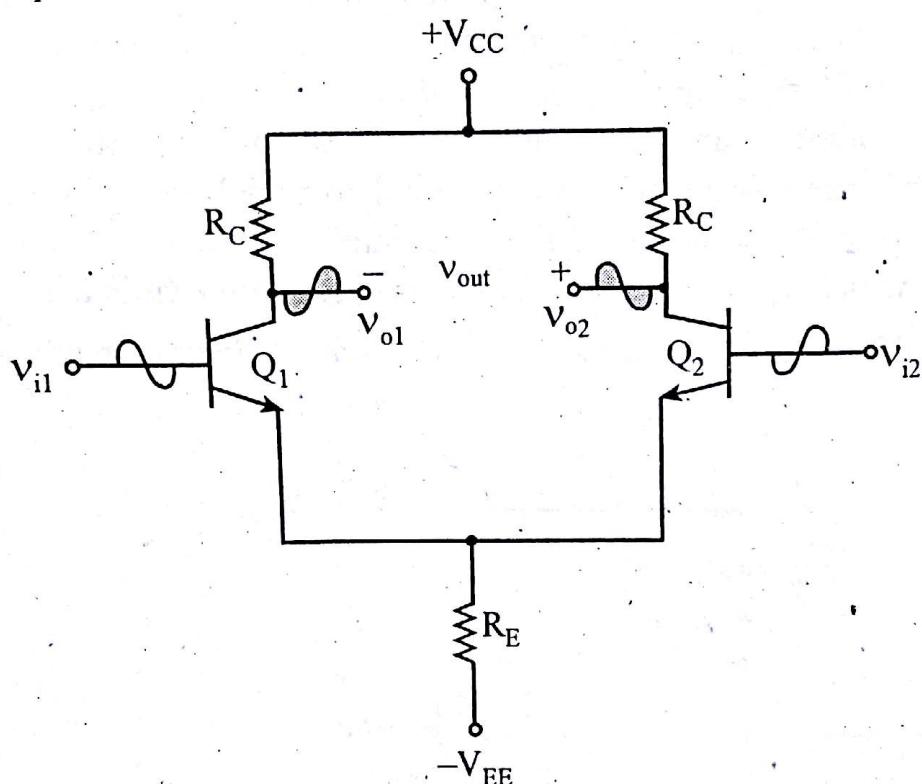


Figure 3.28 Differential mode of operation of a differential amplifier with waveforms.

Case-III: Common-mode input

If same signals are applied to inputs, the operation is called common-mode input. The output voltage v_{out} is zero in this case.

FIELD-EFFECT TRANSISTORS

The field-effect transistor is a semiconductor device which depends for its operation on the control of current by an electric field. There are two types of field-effect transistor

junction field-effect transistor (JFET) and metal-oxide-semiconductor field-effect transistor (MOSFET).

The FET enjoys several advantages over the conventional transistor:

- i. Its operation depends upon the flow of majority carriers only. It is therefore a "unipolar" (one type of carrier) device. The vacuum tube is another example of a unipolar device. The conventional transistor is a "bipolar" device.
- ii. It is relatively immune to radiation.
- iii. It exhibits a high input resistance, typically many megaohms.
- iv. It is less noisy than a tube or a bipolar transistor.
- v. It exhibits no offset voltage at zero drain current, and hence, makes an excellent signal chopper.
- vi. It has thermal stability.

The main disadvantage of the FET is its relatively small gain-bandwidth product in comparison with that which can be obtained with a conventional transistor.

MOSFET

The Enhancement- Type MOSFET

Physical structure

The physical structure of the n-channel enhancement-type is shown below. The transistor is fabricated on a p-type substrate, which is a single-crystal silicon wafer that provides physical support for the device. Two heavily doped n-type regions, as indicated by n^+ are created in the substrate as source and drain. A thin layer of silicon dioxide (SiO_2) of thickness, t_{ox} (typically 2-50 nm), which is an excellent electrical insulator, is grown on the face of substrate as shown in **Figure 3.29** that follows. Metal is deposited on top of the oxide layer to form the gate electrode of the device. Metal contacts are also made to the source region, the drain region, and the substrate (body). Thus, four terminals are brought out: the gate terminal (G), the source terminal (S), the drain terminal (D), and the substrate or body terminal (B).

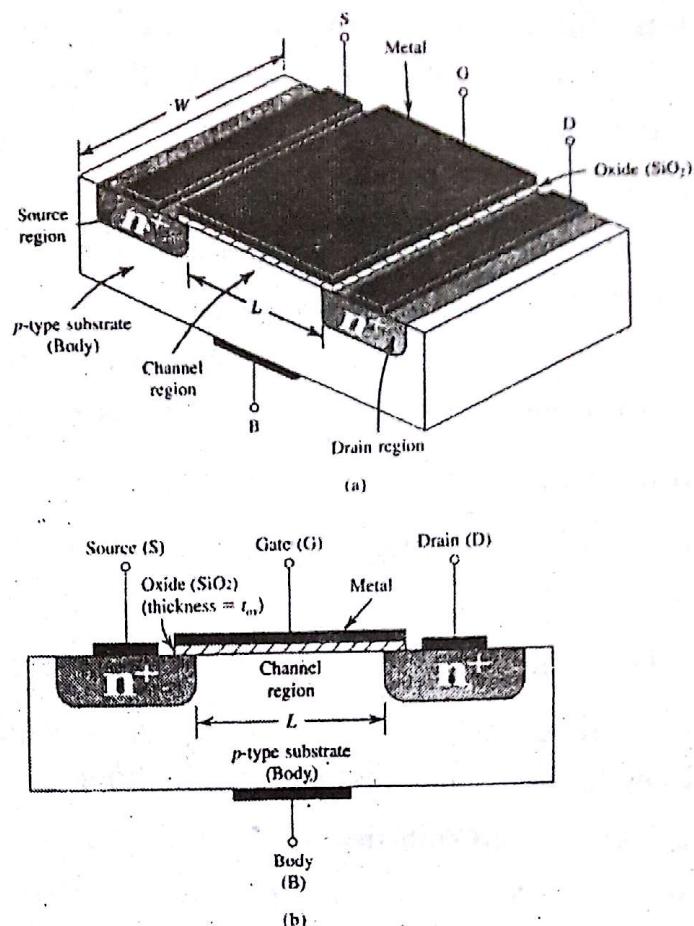


Figure 3.29 Physical structure of the enhancement-type NMOS transistor: (a) perspective view (b) cross section

Operation

i. Operation with no gate voltage

With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source. One diode is formed by the pn-junction between the n⁺ drain region and the p-type substrate, and the other diode is formed by the pn-junction between the p-type substrate and the n⁺ source region. These back-to-back diodes prevent current conduction from drain to source when a voltage v_{DS} is applied.

ii. Creating a channel for current flow

The source and the drain are grounded and a positive voltage is applied to the gate (since the source is grounded, the gate voltage appears in effect between gate and source and thus is denoted v_{GS}). This v_{GS} will induce n-type channel as shown in the **Figure 3.30** that follows. The value of v_{GS} at which a sufficient number of mobile electrons accumulate in the

channel region to form a conducting channel (that is, a channel is just induced) is called the threshold voltage and is denoted by V_t .

iii. Applying a small v_{DS}

Having induced a channel, we now apply a positive voltage v_{DS} between drain and source. A small v_{DS} causes a current i_D to flow through the induced n-channel. Note the graph shown below which depicts that the MOSFET is operating as a linear resistance whose value is controlled by v_{GS} .

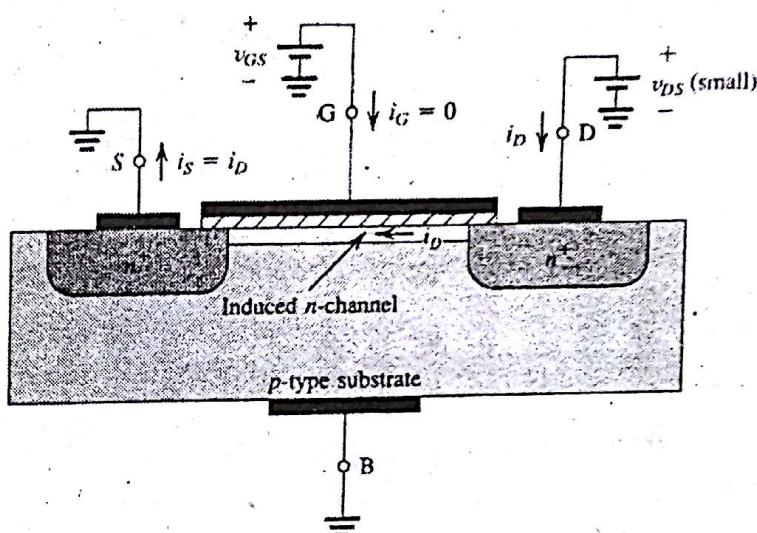


Figure 3.30 An NMOS transistor with $v_{GS} > V_t$ and with small v_{DS} applied

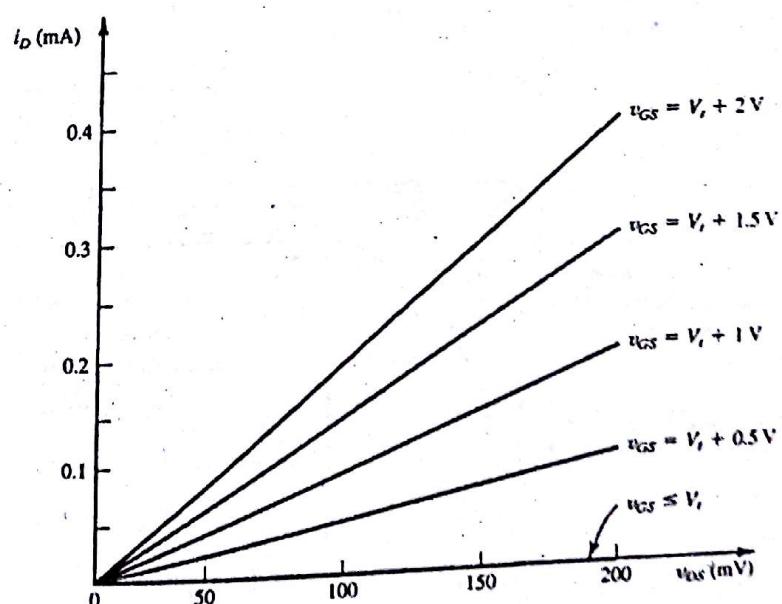


Figure 3.31 The $i_D - v_{DS}$ characteristics of the MOSFET when the voltage applied between drain and source, v_{DS} is kept small

Hence, for the MOSFET to conduct, a channel has to be induced. Then, increasing v_{GS} above V_t enhances the channel, hence, the names enhancement-mode operation and enhancement-type MOSFET.

iv. Operation as v_{DS} is increased

First we held v_{GS} constant at a value greater than V_t and increase v_{DS} . The voltage v_{DS} appears as a voltage drop across the length of the channel. Now, the channel becomes more tapered. Thus, the $i_D - v_{DS}$ curve does not continue as a straight line but bends as shown in the Figure 3.32.

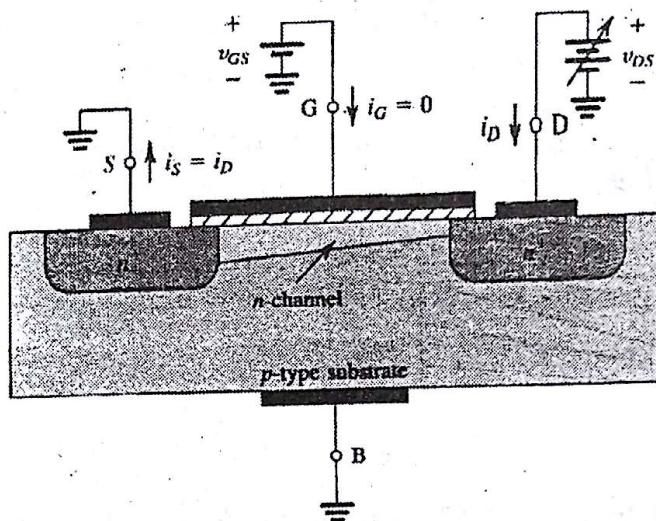


Figure 3.32 Operation of the enhancement NMOS transistor as v_{DS} is increased

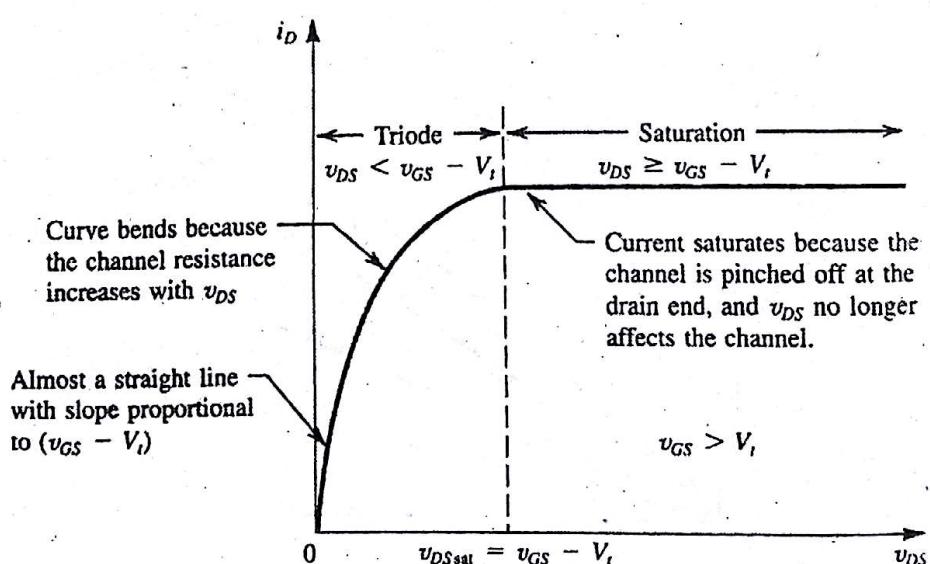


Figure 3.33 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$

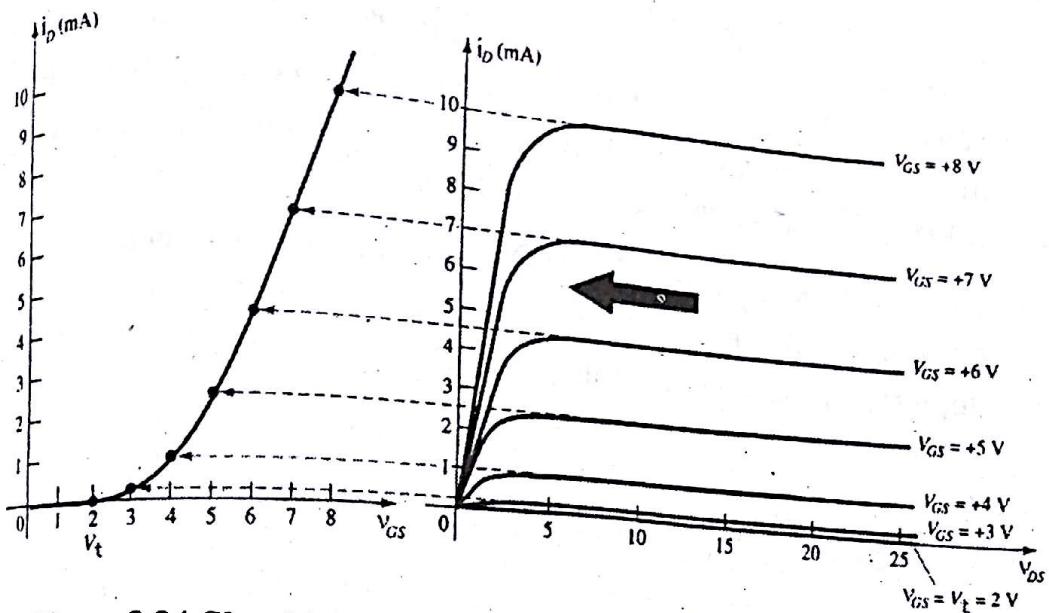


Figure 3.34 Sketching the transfer characteristics for an n-channel enhancement-type MOSFET from the drain characteristics

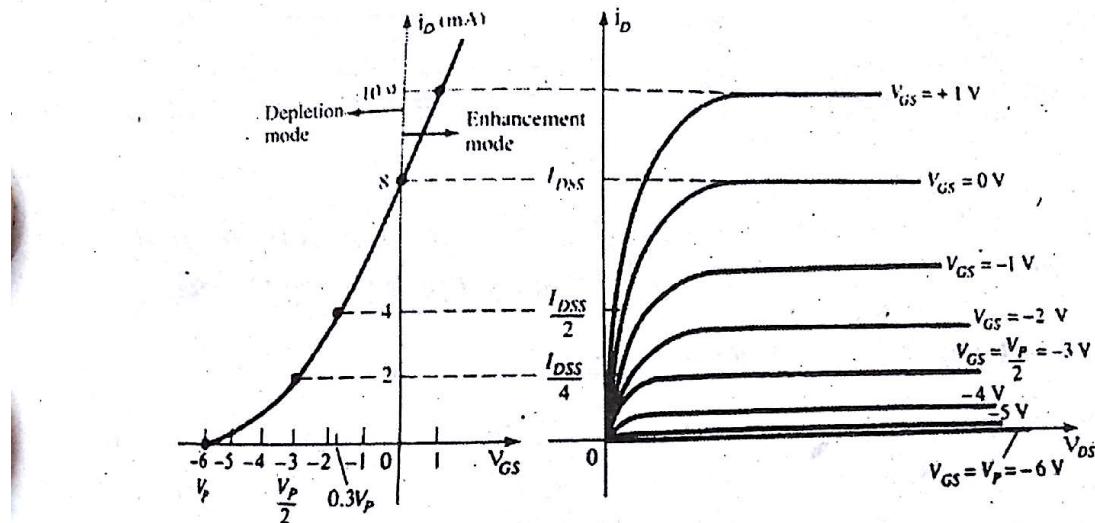
The Depletion-Type MOSFET

The structure of the depletion-type MOSFET is similar to that of the enhancement-type MOSFET with one important difference. The depletion MOSFET has a physically implanted channel. Thus, an n-channel depletion type MOSFET has an n-type silicon region connecting the n^+ source and the n^+ drain regions at the top of the p-type substrate. Thus, if a voltage V_{DS} is applied between drain and source, a current i_D flows for $V_{GS} = 0$. In other words, there is no need to induce a channel, unlike the case of the enhancement MOSFET.

The channel depth and hence, its conductivity can be controlled by V_{GS} in exactly the same manner as in the enhancement -type device. Applying a positive V_{GS} enhances the channel by attracting more electrons into it. Here, however, we also can apply a negative V_{GS} , which causes electrons to be repelled from the channel, and thus, the channel becomes shallower and its conductivity decreases. The negative V_{GS} is said to deplete the channel of its charge carriers, and this mode of operation (negative V_{GS}) is called depletion mode. As the magnitude of V_{GS} is increased in the negative direction, a value is reached at which the channel is

completely depleted of charge carriers and i_D is reduced to zero even though v_{DS} may be still applied. This negative value of v_{GS} is the threshold voltage of the n-channel depletion-type MOSFET and is called pinch-off voltage, V_p .

Hence, a depletion-type MOSFET can be operated in the enhancement mode by applying a positive v_{GS} and in the depletion mode by applying a negative v_{GS} .

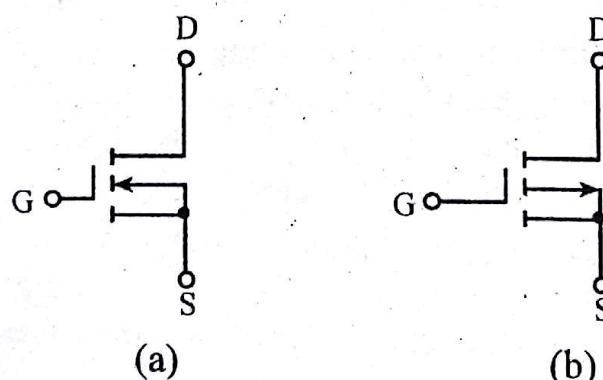


I_{DSS} is the saturation drain current defined by $v_{GS} = 0V$ and $v_{DS} > |V_p|$.

Figure 3.35 Drain and transfer characteristics for an n-channel depletion-type MOSFET

The application of a positive gate-to-source voltage enhances the level of free carriers in the channel compared to that encountered with $v_{GS} = 0V$. For this reason, the region of positive gate voltages on the drain or transfer characteristics is often referred to as the “enhancement region”, with the region between cutoff and the saturation level of I_{DSS} referred to as the “depletion region”.

The symbols of MOSFETs are shown below.



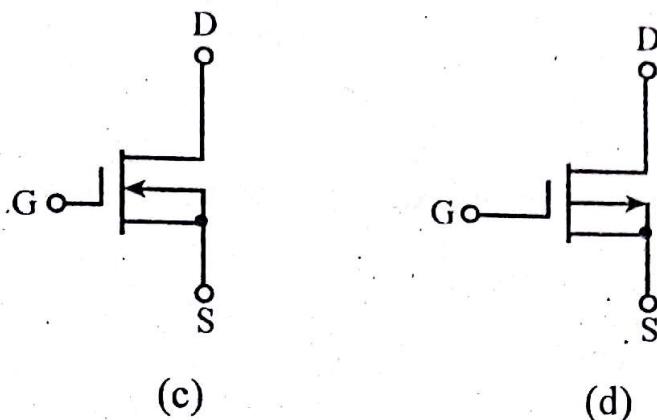


Figure 3.36 (a) n-channel enhancement-type MOSFET (b) p-channel enhancement-type MOSFET (c) n-channel depletion-type MOSFET (d) p-channel depletion-type MOSFET

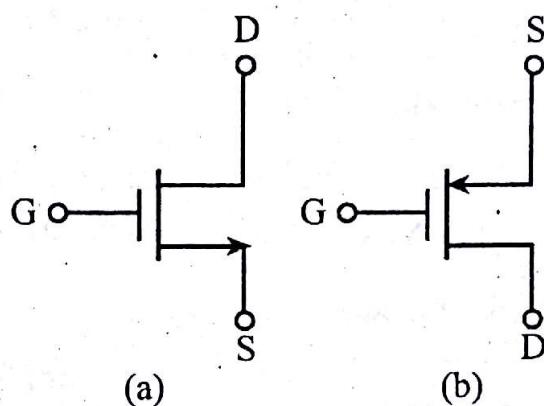


Figure 3.37 (a) Simplified circuit symbol of NMOS to be used when the source is connected to the body or when the effect of the body on device operation is unimportant. (b) Simplified circuit symbol of PMOS to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

NMOS as a Switch (Logic NOT Gate)

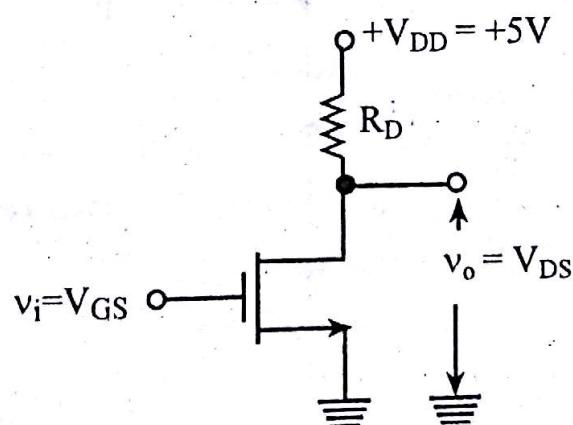


Figure 3.38 NMOS NOT gate

Case I: When $v_i = V_{GS} = 0V = \text{logic 0}$

$$V_{GS} < V_t.$$

\therefore No channel exists so that $R_{DS} \approx 10 \text{ G}\Omega$.

Let $R_D = 5 \text{ k}\Omega$.

We have,

$$V_{DS} = \frac{R_{DS}}{R_{DS} + R_D} V_{DD} = \frac{10\text{G}\Omega}{10\text{G}\Omega + 5 \text{ k}\Omega} \approx 5 \text{ V}$$

$\therefore v_o = V_{DS} = 5 \text{ V} = \text{logic 1.}$

Case II: When $v_i = V_{GS} = +5 \text{ V} = \text{logic 1}$

$$V_{GS} \gg V_t.$$

\therefore Large channel is created so that $R_{DS} \approx 100 \Omega$ (large channel = small resistance).

Let $R_D = 5 \text{ k}\Omega$. We have,

$$V_{DS} = \frac{R_{DS}}{R_{DS} + R_D} V_{DD} = \frac{100\Omega}{100\Omega + 5000 \Omega} \approx 0.1 \text{ V}$$

$\therefore v_o = V_{DS} = 0.1 \text{ V} = \text{logic 0.}$

NMOS NAND gate

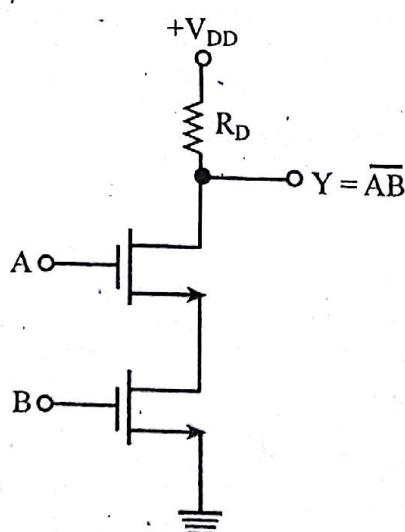


Figure 3.39 NAND gate

NMOS NOR gate

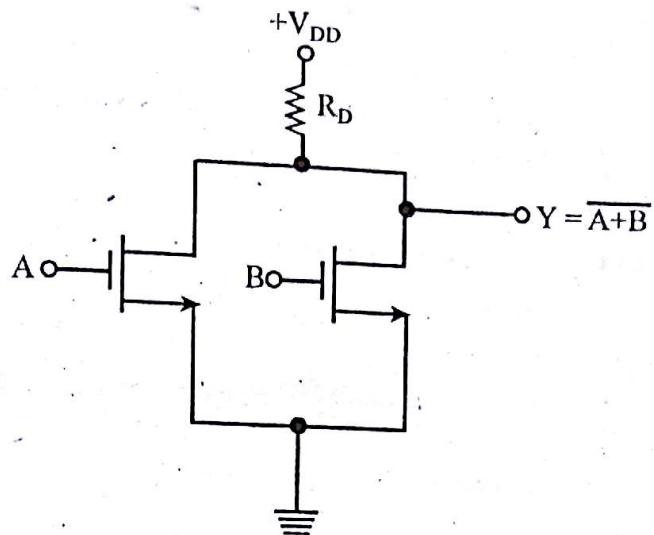


Figure 3.40 NOR gate

COMPLEMENTARY MOS OR CMOS

As the name implies, complementary MOS technology employs MOS transistors of both polarities; and is currently the dominant MOS technology. Although CMOS circuits are somewhat more difficult to fabricate than NMOS, the availability of complementary devices makes possible many powerful circuit-design possibilities.

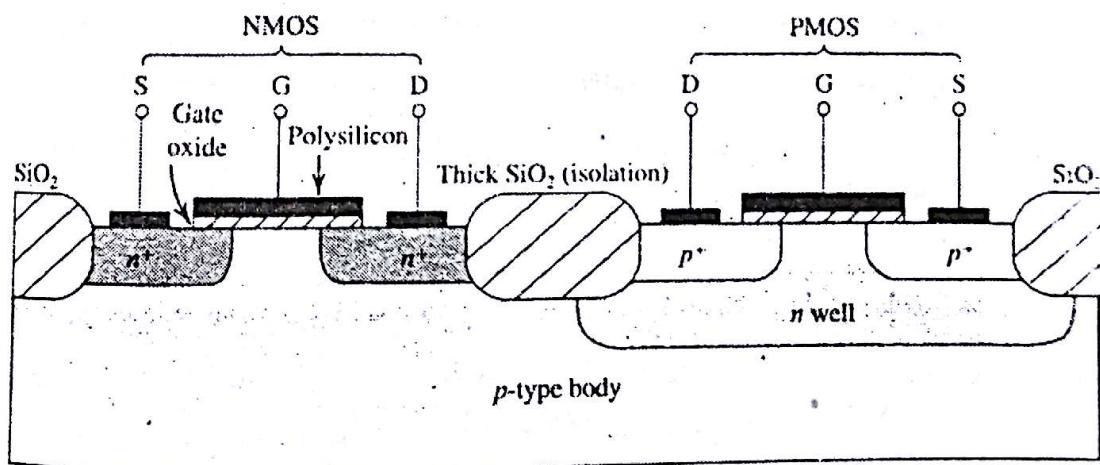


Figure 3.41 Cross-section of a CMOS integrated circuit

Figure 3.41 above shows a cross-section of a CMOS chip illustrating how the PMOS and NMOS transistors are fabricated. Note that, the NMOS transistor is implemented directly in the p-type substrate while the PMOS transistor is fabricated in a specially created n region, known as "n well".

The two devices are isolated from each other by a thick region of oxide that functions as an insulator. Not shown on the diagram are the connections made to the p-type body and to the n well. The latter connection serves as the body terminal for the PMOS transistor.

CMOS Inverter (Logic NOT Gate)

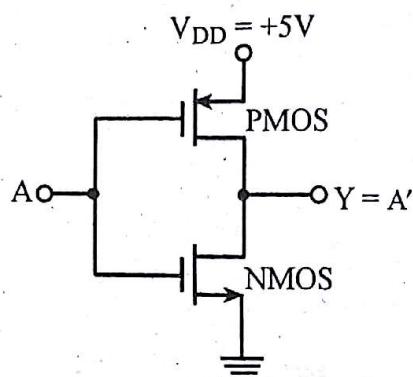


Figure 3.42 CMOS inverter

To understand the operation of the CMOS inverter, we must know that

1. The n-channel MOSFET conducts when its gate-to-source voltage is positive.
2. The p-channel MOSFET conducts when its gate-to-source voltage is negative.
3. Either type of device is turned off if its gate-to-source voltage is zero.

When the input is low, i.e., $A = 0V$, both gates are at zero potential. The input is at $-V_{DD}$ relative to the source of the p-channel MOSFET and at $0V$ relative to the source of the n-channel MOSFET. The result is that the p-channel MOSFET is turned on and the n-channel MOSFET is turned off. Under these conditions, there is a low-impedance path from V_{DD} to the output and a very-high-impedance path from output to ground. Therefore, the output voltage approaches the high level V_{DD} , i.e., $Y \approx 5V$ under normal loading conditions. When the input is high, i.e., $A = 5V$, both gates are at V_{DD} and the situation is reversed. The p-channel MOSFET is off and

the n-channel MOSFET is on. The result is that the output approaches the low level of 0V, i.e., $Y \approx 0V$.

CMOS NAND Gate

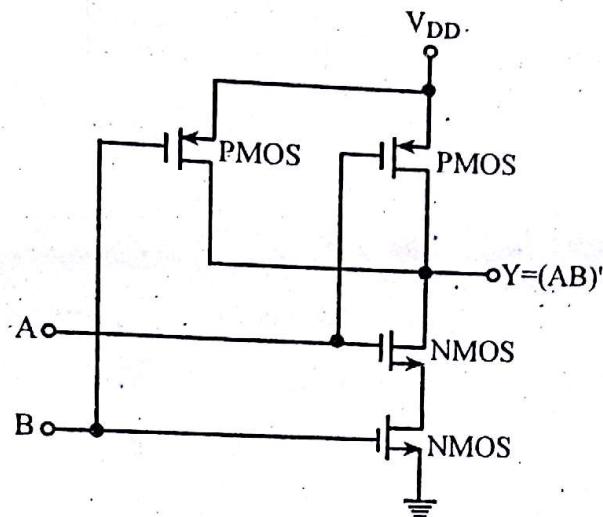


Figure 3.43 CMOS NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Table 3.7 Truth table

CMOS NOR Gate

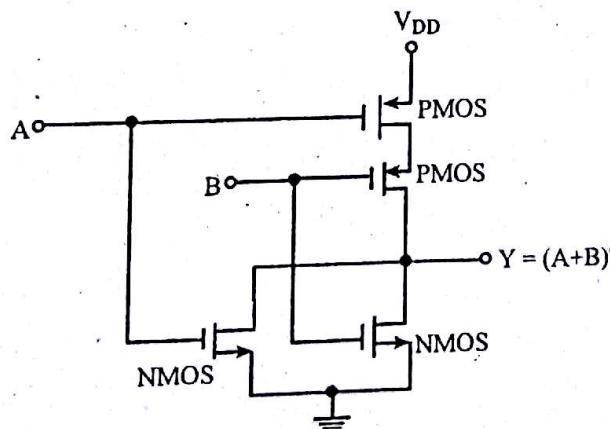


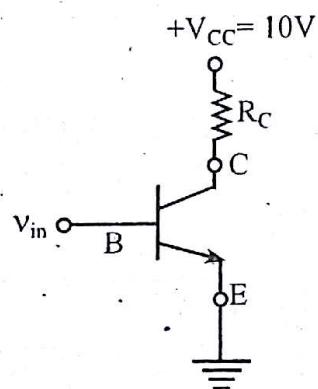
Figure 3.44 CMOS NOR gate

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Table 3.8 Truth table

Problem 3.1

In BJT circuit, if $V_{CC} = 10\text{ V}$, and $R_C = 8\text{ k}\Omega$, draw the dc load line. Determine the Q-point (operating point) for zero input signal if $I_B = 15\text{ }\mu\text{A}$ and $\beta = 40$. [2068 Bhadra]



Solution:

$$I_C = \beta I_B = 40 \times 15 \times 10^{-6} = 0.6 \times 10^{-3} \text{ A}$$

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\text{or, } V_{CC} - \beta I_B R_C - V_{CE} = 0$$

$$\text{or, } +10 - 40 \times 15 \times 10^{-6} \times 8 \times 10^3 - V_{CE} = 0$$

$$\therefore V_{CE} = 5.2 \text{ V} = V_{CEQ}$$

$$\therefore \text{Q-point} = (I_{CQ}, V_{CEQ}) = (6 \times 10^{-4} \text{ A}, 5.2 \text{ V})$$

To draw the dc load line, we use the equation

$$V_{CC} - I_C R_C - V_{CE} = 0$$

For $I_C = 0$,

$$V_{CE} = V_{CC} = 10 \text{ V}$$

For $V_{CE} = 0$,

$$I_C = \frac{V_{CC}}{R_C} = \frac{10}{8 \times 10^3} = 1.25 \times 10^{-3} \text{ A.}$$

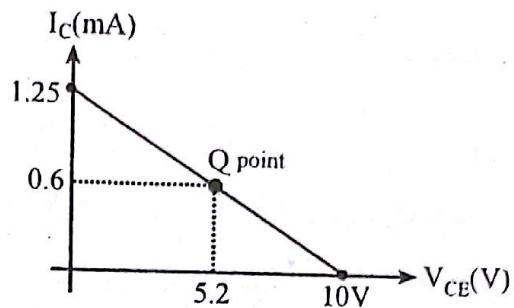
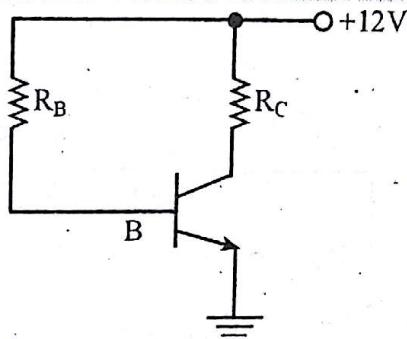


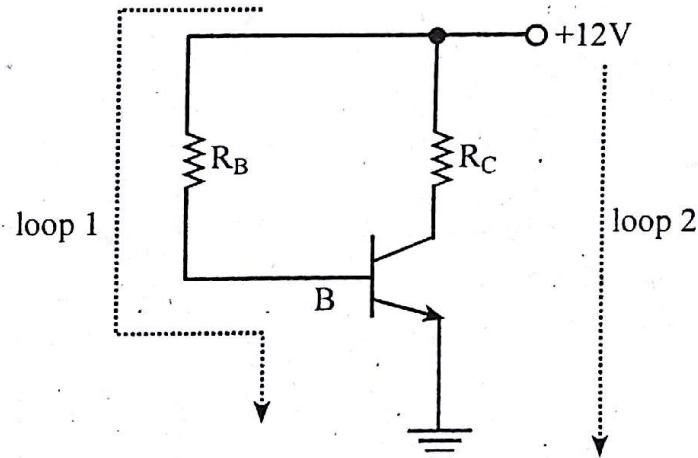
Fig.: Load line

Problem 3.2

Find R_B and R_C in the given circuit. Given data are: $I_C = 1.2$ mA, $V_{CE} = 6V$, and $\beta = 100$.



Solution:



Applying KVL in loop 2,

$$+12 - I_C R_C - V_{CE} = 0$$

$$\text{or, } +12 - 1.2 \times 10^{-3} R_C - 6 = 0 \Rightarrow R_C = 5000 \Omega = 5 \text{ k}\Omega$$

Applying KVL in loop 1,

$$+12 - I_B R_B - V_{BE} = 0$$

Here, $V_{BE} = 0.7 \text{ V}$

$$I_B = \frac{I_C}{\beta} (\because I_C = \beta I_B)$$

$$\therefore I_B = \frac{1.2 \times 10^{-3}}{100} = 1.2 \times 10^{-5} \text{ A}$$

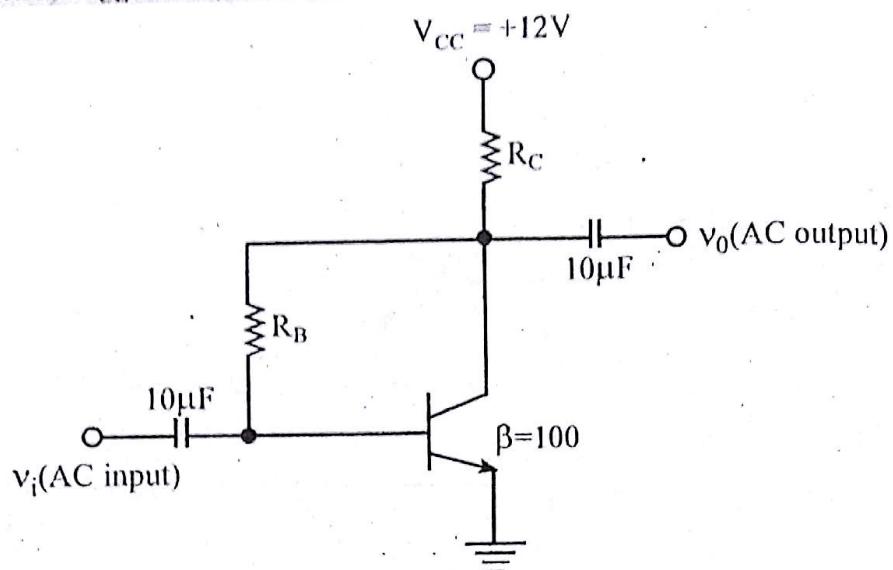
$$\text{So, } +12 - 1.2 \times 10^{-5} R_B - 0.7 = 0$$

$$\therefore R_B = 941666.666 \Omega = 941.666 \text{ k}\Omega$$

Hence, $R_B = 941.666 \text{ k}\Omega$, $R_C = 5 \text{ k}\Omega$

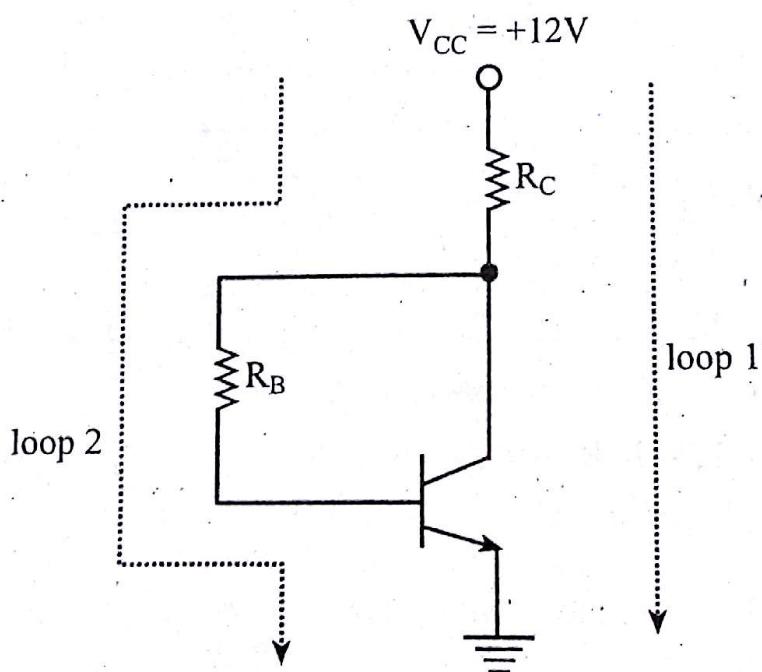
Problem 3.3

Find R_C and R_B in the given circuit. Given data are: $I_C = 1.2 \text{ mA}$, $V_{CE} = 6V$, and $\beta = 100$.



Solution:

Since the capacitor acts as an open circuit for DC, the circuit can be redrawn as



Applying KVL in loop 1,

$$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$$

$$I_C = 1.2 \times 10^{-3} \text{ A}, \quad I_B = \frac{I_C}{\beta} = \frac{1.2 \times 10^{-3}}{100} = 1.2 \times 10^{-5} \text{ A}$$

$$\text{or, } +12 - (1.2 \times 10^{-3} + 1.2 \times 10^{-5}) R_C - 6 = 0$$

$$\therefore R_C = 5000 \Omega = 5 \text{ k}\Omega$$

Applying KVL in loop 2,

$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0$$

$$V_{BE} = 0.7 \text{ V}, \quad I_B = 1.2 \times 10^{-5} \text{ A}$$

$$\text{So, } +12 - (1.2 \times 10^{-3} + 1.2 \times 10^{-5}) \times 5000 - 1.2 \times 10^{-5} R_B - 0.7 = 0$$

$$\therefore R_B = 441666.666 \Omega = 441.666 \text{ k}\Omega$$

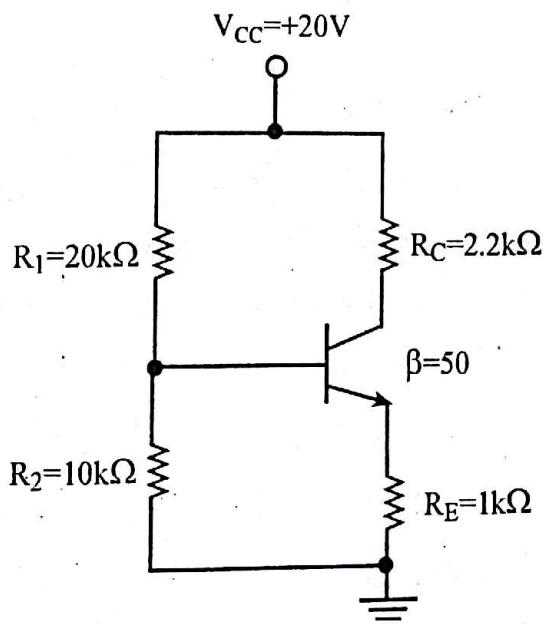
Hence,

$$R_C = 5 \text{ k}\Omega$$

$$R_B = 441.666 \text{ k}\Omega$$

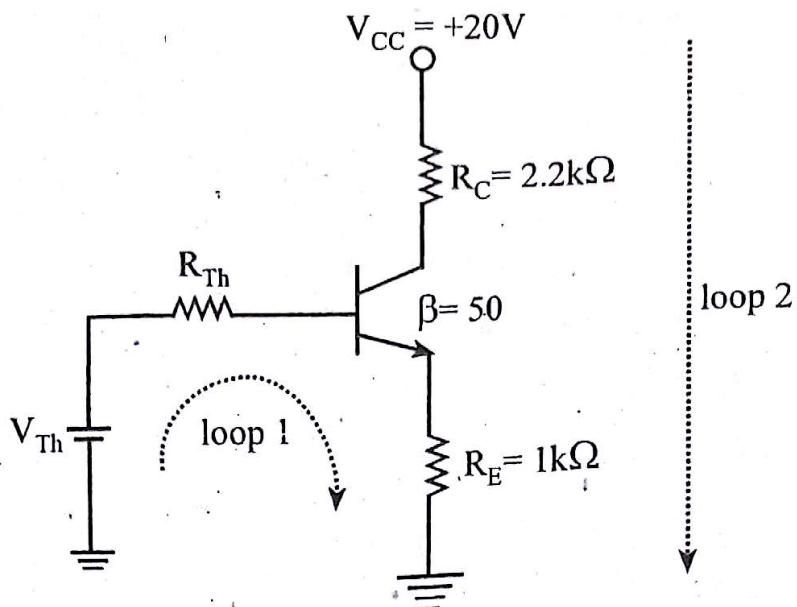
Problem 3.4

Find the value of I_C and V_{CE} for the given circuit.



Solution:

The DC circuit to the left of base terminal, B can be replaced by a Thevenin's equivalent circuit as shown in the figure below.



V_{Th} is determined from the original figure looking to the left from the base terminal, B.

$$V_{Th} = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} = \left(\frac{10}{20 + 10} \right) \times 20 = 6.67 \text{ V}$$

Looking back into the voltage divider with V_{CC} grounded in the original figure, we see R_1 in parallel with R_2 . So,

$$R_{Th} = R_1 \parallel R_2 = \frac{20 \times 10}{20 + 10} = 6.67 \text{ k}\Omega$$

Applying KVL in loop 1,

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$\text{or, } V_{Th} - I_B R_{Th} - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$\text{or, } +6.67 - I_B \times 6.67 \times 10^3 - 0.7 - 51 \times 1 \times 10^3 \times I_B = 0$$

$$\therefore I_B = 1.0352 \times 10^{-4} \text{ A}$$

$$I_C = \beta I_B = 50 \times 1.0352 \times 10^{-4} = 5.176 \times 10^{-3} \text{ A}$$

$$I_E = (\beta + 1) I_B = 51 \times 1.0352 \times 10^{-4} = 5.27952 \times 10^{-3} \text{ A}$$

Applying KVL in loop 2,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

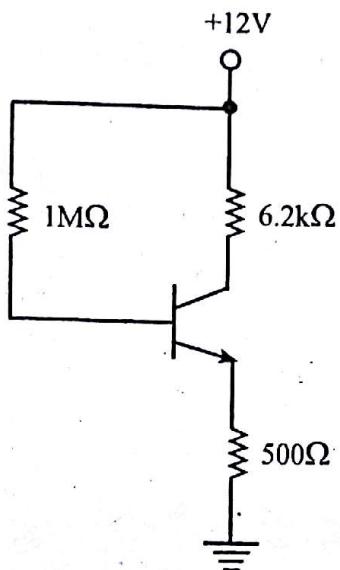
$$\text{or, } +20 - 5.176 \times 10^{-3} \times 2.2 \times 10^3 - V_{CE} - 5.2795 \times 10^{-3} \times 1 \times 10^3 = 0$$

$$\therefore V_{CE} = 3.33 \text{ V}$$

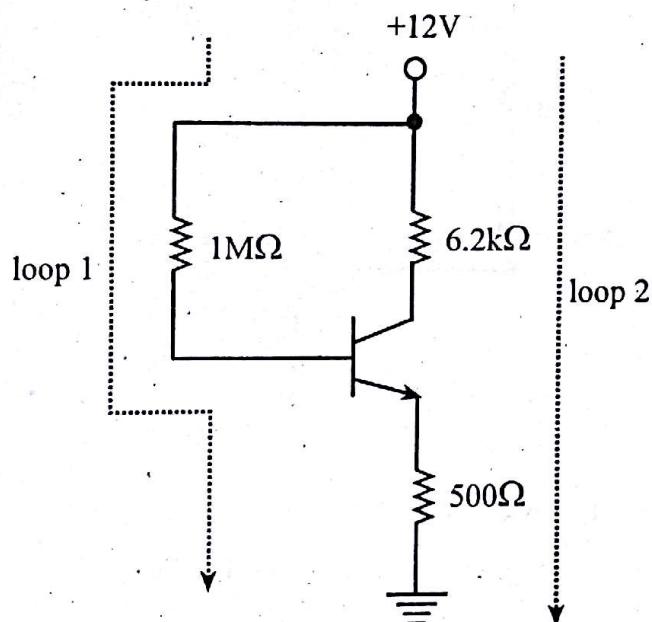
$$\text{Hence, } I_C = 5.176 \times 10^{-3} \text{ A}, V_{CE} = 3.33 \text{ V}$$

Problem 3.5

Find I_C and V_{CE} for the given circuit.



Solution:



Applying KVL in loop 1,

$$+12 - I_B \times 1 \times 10^6 - 0.7 - I_E \times 500 = 0$$

$$\text{or, } +12 - I_B \times 10^6 - 0.7 - (\beta + 1) I_B \times 500 = 0$$

Take $\beta = 100$

Solve and obtain the value of I_B .

Applying KVL in loop 2,

$$+12 - I_C \times 6.2 \times 10^3 - V_{CE} - I_E \times 500 = 0$$

Here, $I_C = \beta I_B$

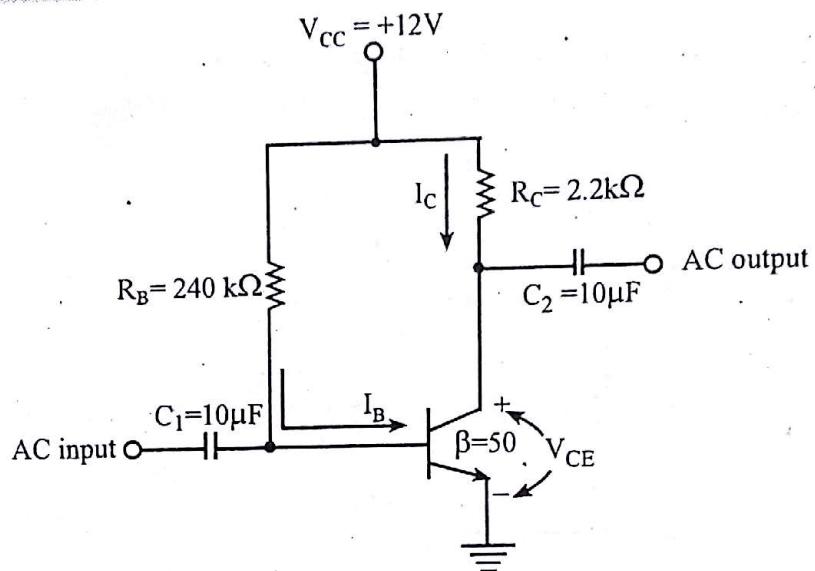
$$I_E = (\beta + 1) I_B$$

Solve and obtain the value of V_{CE} .

Problem 3.6

Determine the following for the fixed-bias configuration of figure shown below.

- I_{BQ} and I_{CQ}
- V_{CEQ}
- V_B and V_C
- V_{BC}



Solution:

a. $V_{CC} - I_{BQ} R_B - V_{BE} = 0$

$$\text{or, } 12 - I_{BQ} \times 240 \times 10^3 - 0.7 = 0 \Rightarrow I_{BQ} = 47.08 \times 10^{-6} \text{ A}$$

b. $V_{CC} - I_{CQ} R_C - V_{CEQ} = 0$

$$\text{Here, } I_{CQ} = \beta I_{BQ} = 50 \times 47.08 \times 10^{-6} = 2.35 \times 10^{-3} \text{ A}$$

$$\therefore V_{CEQ} = V_{CC} - I_{CQ} R_C = 12 - (2.35 \times 10^{-3}) (2.2 \times 10^3)$$
$$= 6.83 \text{ V}$$

c. $V_B = V_{BE} = 0.7 \text{ V}$

$$V_C = V_{CEQ} = 6.83 \text{ V}$$

d. $V_{BC} = V_B - V_C = 0.7 \text{ V} - 6.83 \text{ V} = -6.13 \text{ V}$

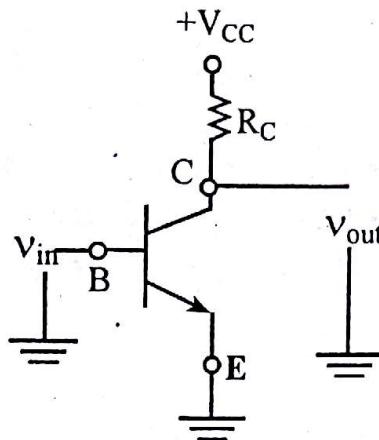
with the negative sign revealing that the junction is reversed – biased, as it should be for linear amplification.

Problem 3.7

Find the value of collector current, Q-point, dc load line for common-emitter circuit having $V_{CC} = 15V$, $R_C = 10K\Omega$, $I_B = 10\mu A$, and $\beta = 40$.

[2069 Bhadra]

Solution:



$$\begin{aligned} I_C &= \beta I_B \\ &= 50 \times 10 \times 10^{-6} = 5 \times 10^{-4} A = 0.5 \times 10^{-3} A \end{aligned}$$

Using,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\text{or, } +15 - 5 \times 10^{-4} \times 10 \times 10^3 - V_{CE} = 0$$

$$\therefore V_{CE} = 10V = V_{CEQ}$$

$$\text{Q-point} = (I_{CQ}, V_{CEQ}) = (0.5 \times 10^{-3} A, 10V)$$

To draw the dc load line, we use the equation

$$V_{CC} - I_C R_C - V_{CE} = 0$$

For $I_C = 0$,

$$V_{CE} = V_{CC} = 15V$$

For $V_{CE} = 0$,

$$I_C = \frac{V_{CC}}{R_C}$$

$$= \frac{15}{10 \times 10^3} = 1.5 \times 10^{-4} A$$

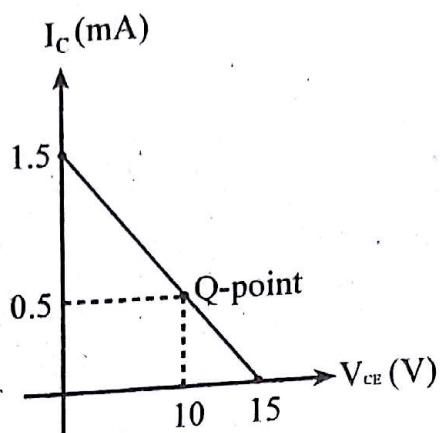


Fig.: Load line

Problem 3.8

Draw collector-feedback type dc biasing circuit. If $V_{CC} = 10V$, $R_B = 950 K\Omega$, $R_C = 2.2 K\Omega$, and $\beta = 150$, calculate the dc operating collector current (I_{CQ}). [2072 Magh]

Solution:

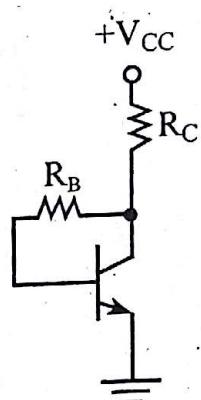
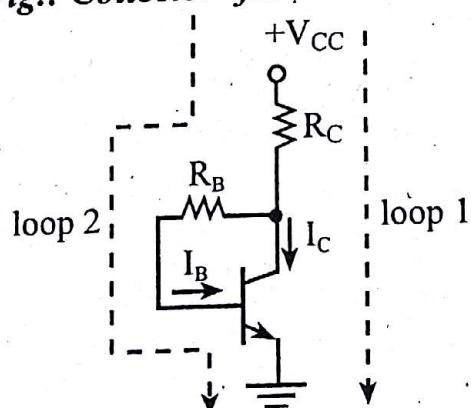


Fig.: Collector-feedback bias circuit



Using KVL in loop 2,

$$+V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0$$

$$\text{or, } +V_{CC} - \left(I_C + \frac{I_C}{\beta} \right) R_C - \frac{I_C}{\beta} R_B - V_{BE} = 0$$

$$\text{or, } 10 - \frac{\beta + 1}{\beta} I_C R_C - \frac{I_C}{\beta} R_B - V_{BE} = 0$$

$$\text{or, } 10 - \frac{151}{150} \times 2.2 \times 10^3 I_C - \frac{950 \times 10^3}{150} I_C - 0.7 = 0$$

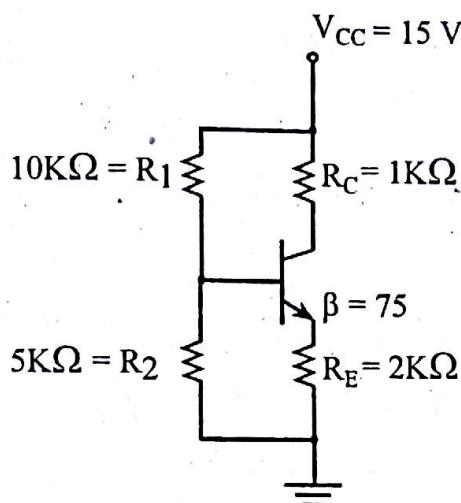
$$\therefore I_C = 1.0879 \times 10^{-3} \text{ A} = I_{CQ}$$

Problem 3.9

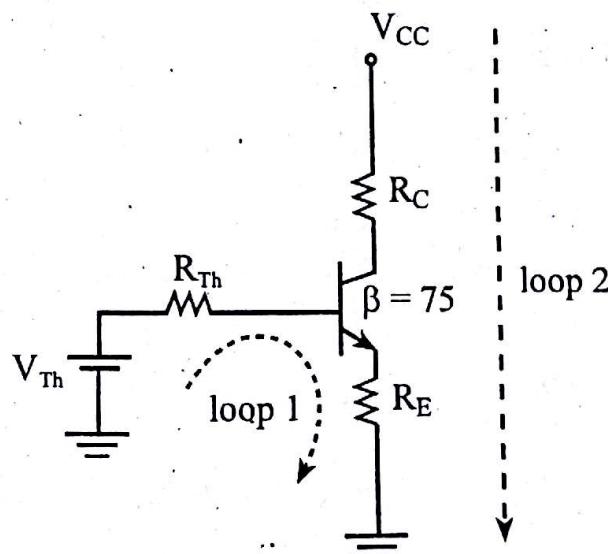
Draw the dc load line and determine the Q-point of the voltage divider biased transistor circuit having $V_{CC}=15V$, $R_C=1 K\Omega$, $R_1=10 K\Omega$, $R_2=5 K\Omega$, $R_E=2 K\Omega$ and $\beta=75$.

[2073 Bhadra]

Solution:



The DC circuit to the left of base terminal can be replaced by a Thevenin's equivalent circuit as shown in the figure below.



$$\text{where } V_{Th} = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} = \frac{5}{15} \times 15 = 5V$$

$$R_{Th} = R_1 \parallel R_2 = 10 \parallel 5 = \frac{10 \times 5}{10 + 5} = 3.33 \text{ K}\Omega$$

Applying KVL in loop 1,

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$\text{or, } V_{Th} - I_B R_{Th} - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$\text{or, } 5 - I_B \times 3.33 \times 10^3 - 0.7 - 76 \times I_B \times 2 \times 10^3 = 0$$

$$\text{or, } 4.3 - (3.33 \times 10^3 + 152 \times 10^3) I_B = 0$$

$$\therefore I_B = 2.768 \times 10^{-5} \text{ A}$$

$$I_C = \beta I_B = 75 \times 2.768 \times 10^{-5} = 2.076 \times 10^{-3} \text{ A}$$

$$I_E = (\beta + 1) I_B = 76 \times 2.768 \times 10^{-5} = 2.1036 \times 10^{-3} \text{ A}$$

Applying KVL in loop 2,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\text{or, } 15 - 2.076 \times 10^{-3} \times 1 \times 10^3 - V_{CE} - 2.1036 \times 10^{-3} \times 2 \times 10^3 = 0$$

$$\text{or, } 15 - 2.076 - V_{CE} - 4.2072 = 0$$

$$\text{or, } V_{CE} = 8.716 \text{ V}$$

Hence, Q-point = $(I_C, V_{CE}) = (2.076 \times 10^{-3} \text{ A}, 8.716 \text{ V}) = (I_{CQ}, V_{CEQ})$

To draw the load line, we use the equation

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\text{or, } V_{CC} - I_C R_C - V_{CE} - \frac{\beta+1}{\beta} I_C R_E = 0$$

For $I_C = 0$,

$$V_{CE} = V_{CC} = 15 \text{ V}$$

For $V_{CE} = 0$,

$$15 - I_C \times 1 \times 10^3 - 0 - \frac{76}{75} \times I_C \times 2 \times 10^3 = 0$$

$$\therefore I_C = 4.9559 \times 10^{-3} \text{ A}$$

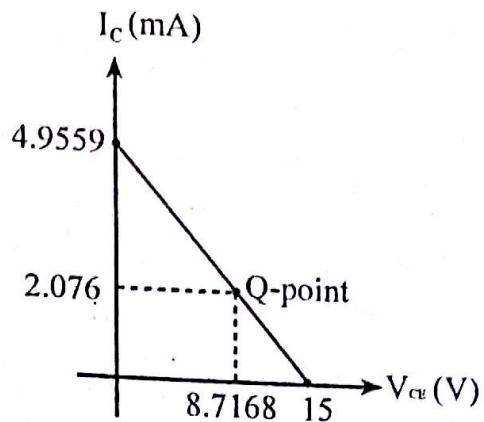


Fig.: Load line

Problem 3.10

Draw emitter-feedback bias circuit of BJT by labeling all the circuit components. Find I_C and V_{CE} in the circuit if $V_{CC} = +12V$, $R_B = 430 K\Omega$, $R_C = 2 K\Omega$, $R_E = 1 K\Omega$, and $\beta = 50$.

[2073 Magh]

Solution:

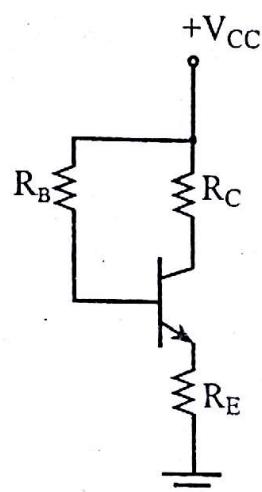
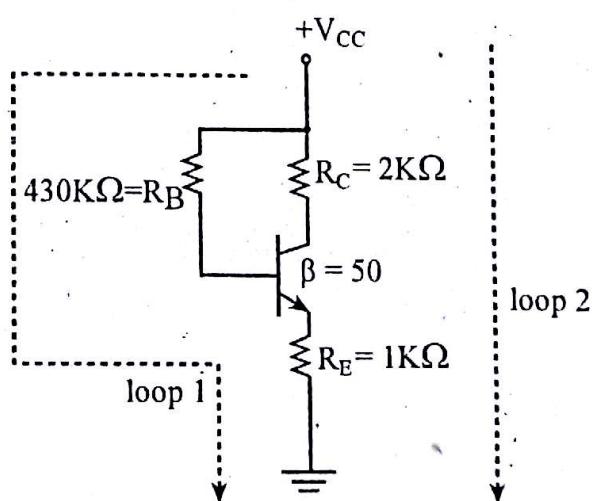


Fig.: Emitter-feedback bias circuit



Using KVL in loop 1,

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$\text{or, } V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$\text{or, } 12 - 430 \times 10^3 \times I_B - 0.7 - 51 \times 1 \times 10^3 I_B = 0$$

$$\therefore I_B = 23.4 \times 10^{-6} \text{ A}$$

$$I_C = \beta I_B = 50 \times 23.4 \times 10^{-6} = 1.17 \times 10^{-3} \text{ A}$$

$$I_E = (\beta + 1) I_B = 51 \times 23.4 \times 10^{-6} = 1.193 \times 10^{-3} \text{ A}$$

Using KVL in loop 2,

$$+V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\text{or, } +12 - 1.17 \times 10^{-3} \times 2 \times 10^3 - V_{CE} - 1.193 \times 10^{-3} \times 1 \times 10^3 = 0$$

$$\text{or, } V_{CE} = 8.467 \text{ V}$$

$$\text{Hence, } I_C = 1.17 \times 10^{-3} \text{ A}, V_{CE} = 8.467 \text{ V}$$

The Operational Amplifier and Oscillator

INTRODUCTION

The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for performing mathematical operations such as addition, subtraction, multiplication, and integration. Thus, the name "operational amplifier" stems from its original use for these mathematical operations and is abbreviated to op-amp. With the addition of suitable external feedback components, the modern day op-amp can be used for a variety of applications such as ac and dc signal amplification, active filters, oscillators, comparators, regulators, displays, testing and measuring systems, and others.

INTERNAL BLOCK DIAGRAM OF AN OP-AMP

A typical op-amp is made up of three types of amplifier circuit: a differential amplifier, a voltage amplifier, and a push-pull amplifier as shown in **Figure 4.1**.

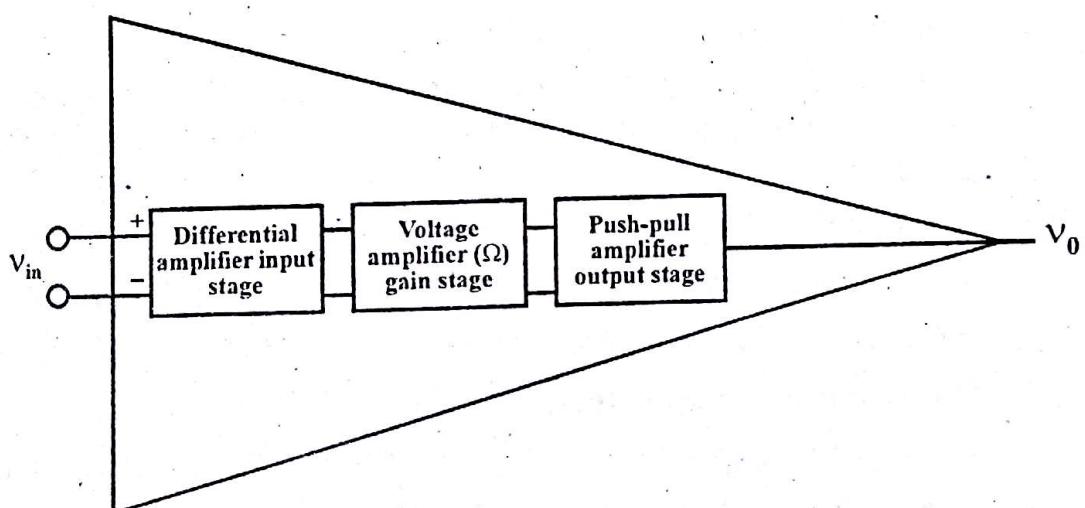


Figure 4.1 Internal block diagram of an op-amp

THE IDEAL OP-AMP

An ideal op-amp would exhibit the following electrical characteristics:

1. **Infinite voltage gain, A_o .**
2. **Infinite input resistance, R_i** so that almost any signal source can drive it and there is no loading of the preceding stage.
3. **Zero output resistance, R_o** so that the output can drive an infinite number of other devices.
4. **Zero output voltage when input voltage is zero.**
5. **Infinite bandwidth** so that any frequency signal from 0 to ∞ Hz can be amplified without attenuation.
6. **Infinite common-mode rejection ratio** so that the output common-mode noise voltage is zero.
7. **Infinite slew rate** so that output voltage changes occur simultaneously with input voltage changes.

SOME BASIC TERMS

1. Open-loop voltage gain and closed-loop voltage gain

The maximum possible voltage gain from a given op-amp is called *open-loop voltage gain* and is denoted by A_o . The term "open-loop" indicates a circuit condition when there is no feedback path from the output to the input of op-amp. The typical value of A_o for a 741 op-amp is 200000.

When a feedback path is present, the resulting circuit gain is referred to as *closed-loop voltage gain* and is denoted by the symbol A.

2. Bandwidth

All electronic devices work only over a limited range of frequencies. This range of frequencies is called *bandwidth*.

3. Gain-bandwidth product.

The *gain-bandwidth product* (GBW), or unity - gain bandwidth, of an operational amplifier is the open loop gain at a given frequency multiplied by the frequency.

4. Common-mode rejection ratio

The *common-mode rejection ratio* (CMRR) (expressed in dB) defines how good the amplifier is at attenuating common mode input voltages.

5. Slew rate

The *slew rate* of an op-amp is a measure of how fast the output voltage can change and is measured in volts per microsecond ($V/\mu s$).

6. Input bias current

The *input bias current* (I_{IB}) is the base current for the op-amp input stage transistors. The typical value of I_{IB} for a 741 op-amp 80 nA.

7. Input offset voltage and input offset current

Ideally, the input stage transistors should be perfectly matched, so that zero voltage difference between the two input (base) terminals should produce a zero output voltage. In practice, there is always some difference between the base-emitter voltages of the transistors and this result in an *input offset voltage* (V_{IO}) for a 741 op-amp is 1.0 mV. Similarly, because of mismatch of input transistors, there is also an *input offset current* (I_{IO}). The typical value of I_{IO} for a 741 op-amp is 20 nA.

8. Input and output resistance

The *input resistance* (R_i) and the *output resistance* (R_o) are the resistances at the op-amp terminals when no feedback is involved. The typical values of R_i and R_o for a 741 op-amp are $2M\Omega$ and 75Ω respectively.

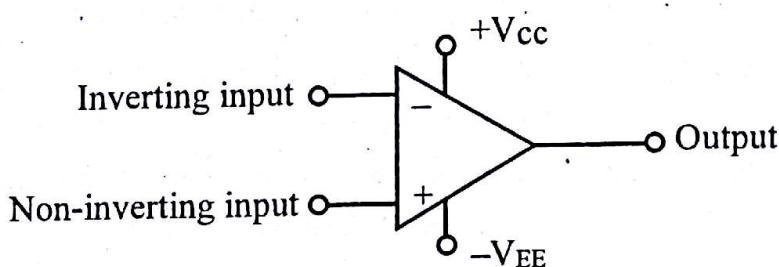


Figure 4.2 Op-amp circuit symbol

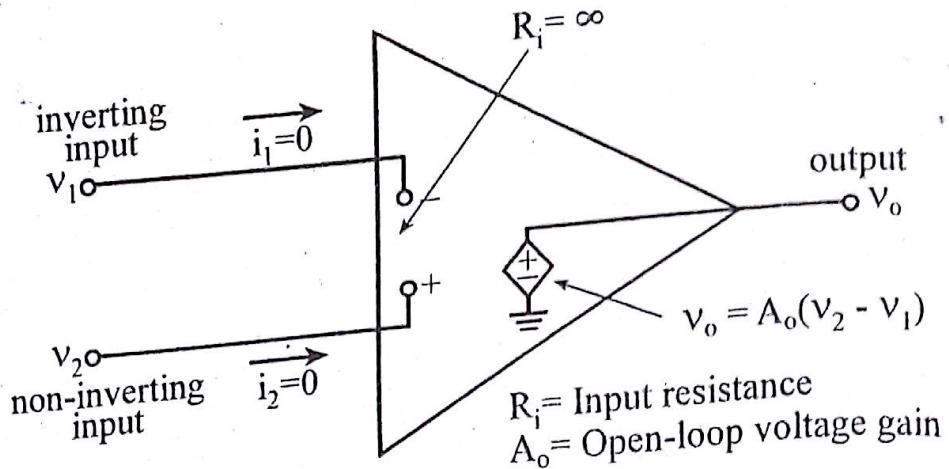


Figure 4.3 Model of an ideal op-amp

VIRTUAL GROUND

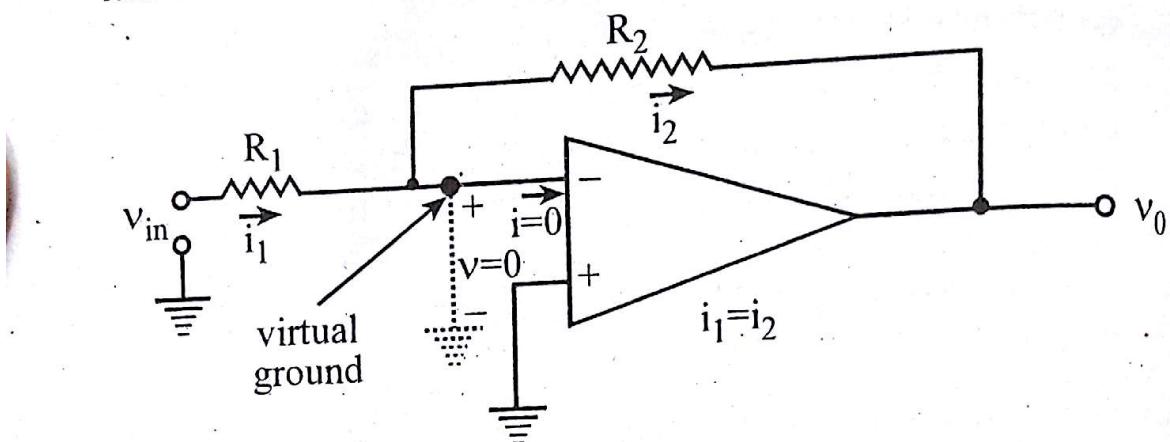


Figure 4.4 The concept of virtual ground

When we connect a piece of wire between some point in a circuit and ground, the voltage of the point becomes zero. Furthermore, the wire provides a path for current to flow to ground. A "mechanical ground" (a wire between a point and ground) is ground to both voltage and current.

A "virtual ground" is different. This type of ground is a widely used shortcut for analyzing an inverting amplifier. With a virtual ground, the analysis of an inverting amplifier and related circuits becomes incredibly easy.

The concept of a virtual ground is based on an ideal op-amp. When an op-amp is ideal, it has infinite open-loop voltage gain and infinite input resistance. Because of this, we can deduce the following ideal properties for the inverting amplifier of Figure 4.4.

1. Since R_i is infinite, $i = 0$.
2. Since A_o is infinite, $v = 0$.

Since i is 0, the current through R_2 must equal the input current through R_1 , as shown. Furthermore, since $v = 0$, the virtual ground shown means that the inverting input acts like a ground for voltage but an open for current.

Virtual ground is very unusual. It is like half of a ground because it is a short for voltage but an open for current. To remind us of this half-ground quality, Figure 4.4 uses a dashed line between the inverting input and ground. The dashed line means that no current can flow to ground. Although virtual ground is an ideal approximation, it gives very accurate answers when used with heavy negative feedback.

VIRTUAL SHORT

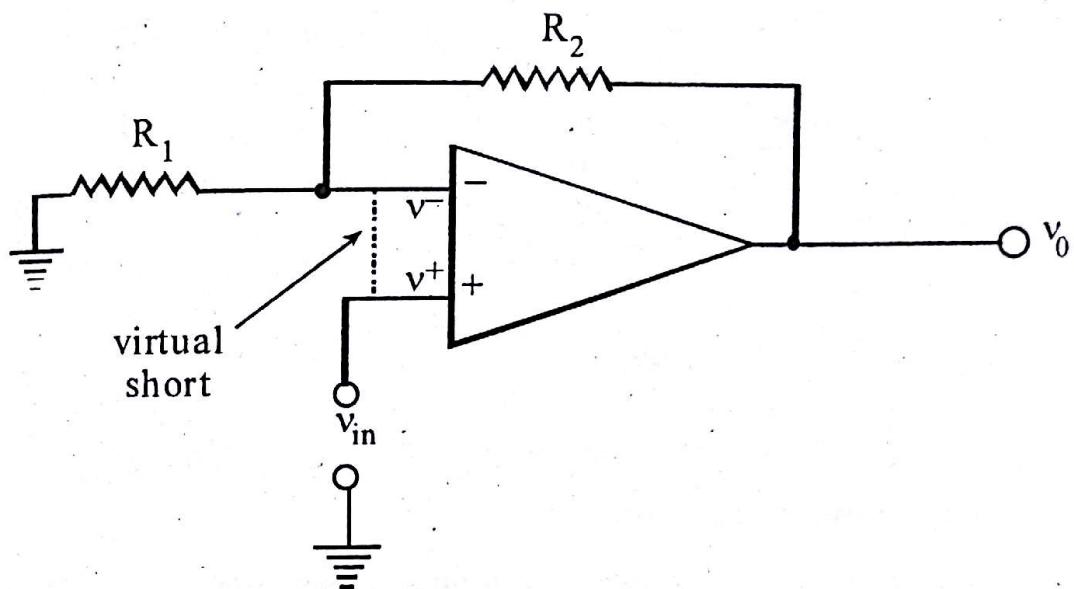


Figure 4.5 The concept of virtual short

When we connect a piece of wire between two points in a circuit, the voltage of both points with respect to ground is equal. Furthermore, the wire provides a path for current to flow between the two points. A "mechanical short" (a wire between two points) is a short for both voltage and current.

A "virtual short" is different. This type of short can be used for analyzing non-inverting amplifiers. With a virtual short,

we can quickly and easily analyze non-inverting amplifiers and related circuits.

The virtual short uses these two properties of an ideal op-amp:

1. Since R_i is infinite, both input currents are zero.
2. Since A_o is infinite, $v^+ - v^- = 0$.

Figure 4.5 shows a virtual short between the input terminals of the op-amp. The virtual short is a short for voltage but an open for current. As a reminder, the dashed line means that no current can flow through it. Although the virtual short is an ideal approximation, it gives very accurate answers when used with heavy negative feedback.

APPLICATIONS OF OP-AMPS

1. Inverting amplifier

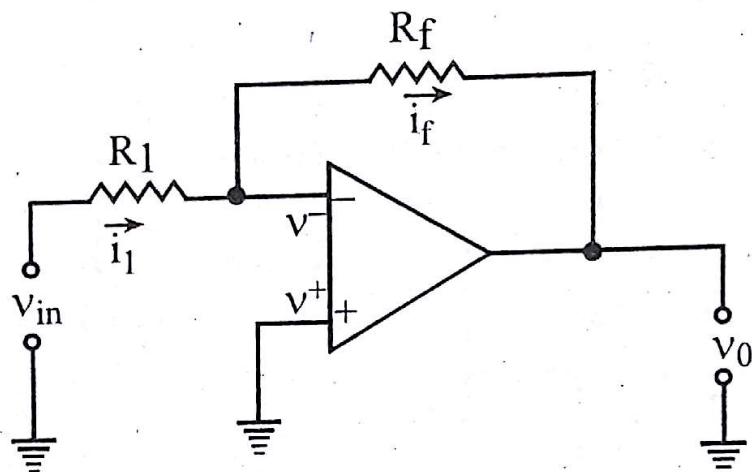


Figure 4.6 Circuit diagram of an inverting amplifier

Our assumptions are:

- i. The input resistance (i.e., the resistance that appears between the inverting and non-inverting input terminals, R_i) is infinite.
- ii. The open loop voltage gain (i.e., the ratio of v_o to v_{in} with no feedback applied) is infinite.

As a consequence,

- i. The voltage appearing between the inverting and non-inverting terminals will be zero. This will make v^- equals to v^+ .

- ii. The current flowing into the op-amp chip will be zero.
This will make i_1 equals to i_f .

Using, $i_1 = i_f$

$$\text{or, } \frac{v_{in} - v^-}{R_1} = \frac{v^- - v_o}{R_f}$$

$$\text{or, } \frac{v_{in} - v^+}{R_1} = \frac{v^+ - v_o}{R_f}$$

$$\text{or, } \frac{v_{in} - 0}{R_1} = \frac{0 - v_o}{R_f}$$

$$\text{or, } \frac{v_o}{v_{in}} = \frac{-R_f}{R_1}$$

$$\therefore \text{Closed - loop voltage gain (A)} = \frac{v_o}{v_{in}} = \frac{-R_f}{R_1}$$

Multiplier and divider

$$v_o = \frac{-R_f}{R_1} v_{in}$$

If $R_f > R_1$, the circuit acts as a multiplier.

If $R_f < R_1$, the circuit acts as a divider.

2. Non-inverting amplifier

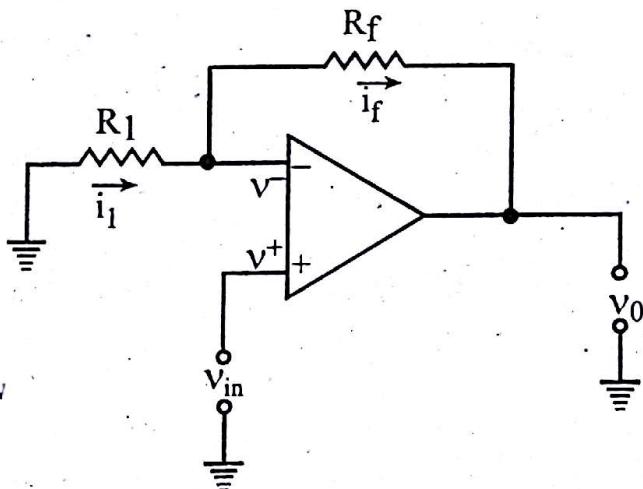


Figure 4.7 Circuit diagram of a non-inverting amplifier

Using, $i_1 = i_f$

$$\text{or, } \frac{0 - v^-}{R_1} = \frac{v^- - v_o}{R_f}$$

$$\text{or, } \frac{-v^+}{R_1} = \frac{v^+ - v_o}{R_f}$$

$$\text{or, } \frac{-v_{in}}{R_1} = \frac{v_{in} - v_o}{R_f}$$

$$\text{or, } \frac{v_o}{R_f} = \frac{v_{in}}{R_f} + \frac{v_{in}}{R_1}$$

$$\text{or, } \frac{v_o}{v_{in}} = R_f \left(\frac{1}{R_f} + \frac{1}{R_1} \right)$$

$$\text{or, } \frac{v_o}{v_{in}} = 1 + \frac{R_f}{R_1}$$

$$\therefore A = \frac{v_o}{v_{in}} = 1 + \frac{R_f}{R_1}$$

3. Adder

This circuit performs the addition of signals with amplification (if desired).

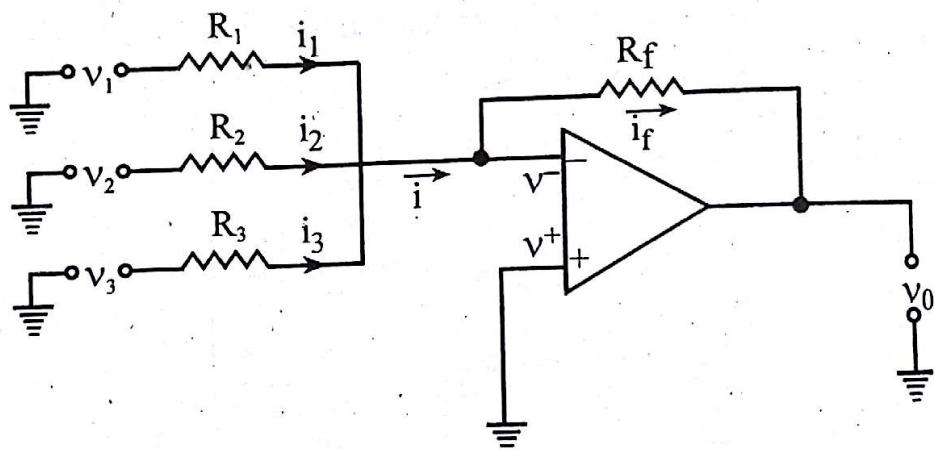


Figure 4.8 Circuit diagram of an adder

Using, $i = i_f$

$$\text{or, } i_1 + i_2 + i_3 = i_f$$

$$\text{or, } \left(\frac{v_1 - v^-}{R_1} \right) + \left(\frac{v_2 - v^-}{R_2} \right) + \left(\frac{v_3 - v^-}{R_3} \right) = \frac{v^- - v_o}{R_f}$$

$$\text{or, } \left(\frac{v_1 - v^+}{R_1} \right) + \left(\frac{v_2 - v^+}{R_2} \right) + \left(\frac{v_3 - v^+}{R_3} \right) = \frac{v^+ - v_o}{R_f}$$

$$\text{or, } \left(\frac{v_1 - 0}{R_1} \right) + \left(\frac{v_2 - 0}{R_2} \right) + \left(\frac{v_3 - 0}{R_3} \right) = \frac{0 - v_o}{R_f}$$

$$\text{or, } \frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} = -\frac{v_o}{R_f}$$

$$\text{or, } v_o = -\left[\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3 \right]$$

For $R_1 = R_2 = R_3 = R_f$, we have

$$v_o = -(v_1 + v_2 + v_3)$$

4. Subtractor

This circuit is used for subtraction of two input signals.

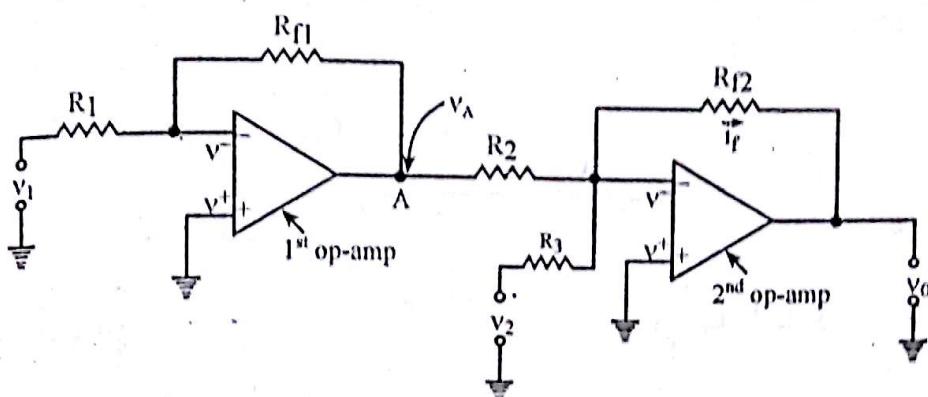


Figure 4.9 Circuit diagram of a subtractor

The output voltage due to first op-amp is

$$v_A = \frac{-R_{f1}}{R_1} v_1$$

For $R_{f1} = R_1$, $v_A = -v_1$

The second op-amp has two input signals $-v_1$ and v_2 fed to the inverting terminal.

For input signal $-v_1$, output voltage due to second op-amp is

$$v_O' = \frac{-R_{f2}}{R_2} (-v_1)$$

For $R_{f2} = R_2$, $v_O' = v_1$

For input signal v_2 , output voltage due to second op-amp is

$$v_O'' = \frac{-R_{f2}}{R_3} (v_2)$$

For $R_{f2} = R_3$, $v_O'' = -v_2$

Using superposition principle, the output voltage due to v_1 and v_2 is given as

$$v_o = v_o' + v_o''$$

$$\therefore v_o = v_1 - v_2$$

5. Integrator

A circuit that performs the mathematical integration of input signal is called an integrator. For example, if the input to the integrator is a square wave, the output will be a triangular wave.

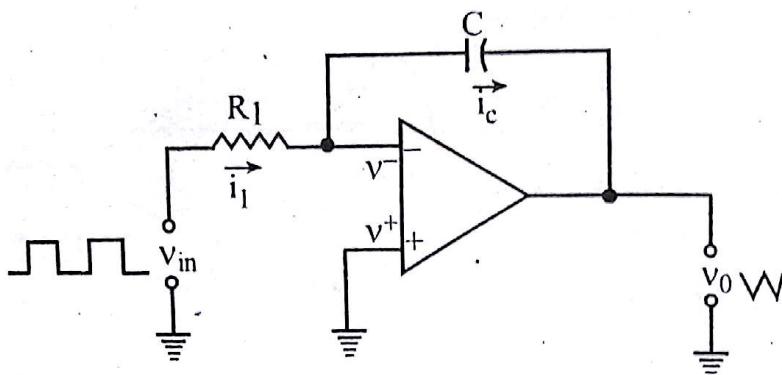


Figure 4.10 Circuit diagram of an integrator

Using, $i_1 = i_c$

$$\text{or, } \frac{v_{in} - v^-}{R_1} = C \frac{dv_c}{dt}$$

$$\text{or, } \frac{v_{in} - v^-}{R_1} = C \frac{d(v^- - v_o)}{dt}$$

$$\text{or, } \frac{v_{in} - v^+}{R_1} = C \frac{d}{dt} (v^+ - v_o)$$

$$\text{or, } \frac{v_{in} - 0}{R_1} = C \frac{d}{dt} (0 - v_o)$$

$$\text{or, } \frac{v_{in}}{R_1} = -C \frac{dv_o}{dt}$$

$$\text{or, } dv_o = \frac{-1}{R_1 C} v_{in} dt$$

$$\text{On integration, } v_o = \frac{-1}{R_1 C} \int v_{in} dt$$

Differentiator

6.

A circuit that performs the mathematical differentiation of input signal is called a differentiator. For example, if the input to the differentiator is a triangular wave, the output will be a square wave.

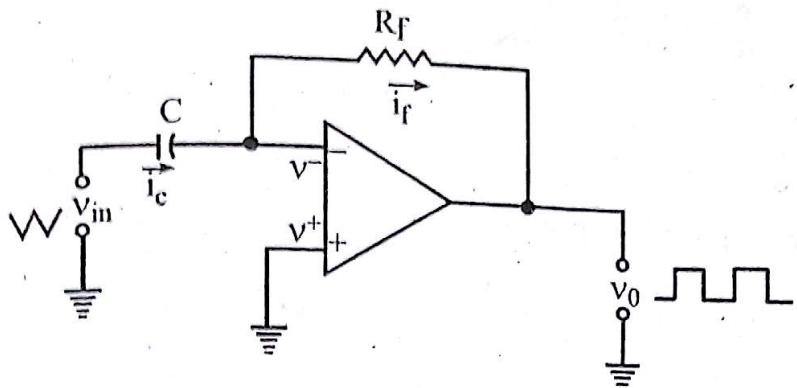


Figure 4.11 Circuit diagram of a differentiator

$$\text{Using, } i_c = i_f$$

$$\text{or, } C \frac{dv_c}{dt} = \frac{v^- - v_o}{R_f}$$

$$\text{or, } C \frac{d}{dt} (v_{in} - v^-) = \frac{v^- - v_o}{R_f}$$

$$\text{or, } C \frac{d}{dt} (v_{in} - v^+) = \frac{v^+ - v_o}{R_f}$$

$$\text{or, } C \frac{d}{dt} (v_{in} - 0) = \frac{0 - v_o}{R_f}$$

$$\text{or, } C \frac{dv_{in}}{dt} = \frac{-v_o}{R_f}$$

$$\therefore v_o = -R_f C \frac{dv_{in}}{dt}$$

Problem 4.1

Realize a circuit to obtain $v_o = -2v_1 + 3v_2 + 4v_3$ using an operational amplifier. Use minimum value of resistance as $10k\Omega$

Solution:

For adder circuit,

$$v_o = - \left[\frac{R_f}{R_1} (v_1) + \frac{R_f}{R_2} (v_2) + \frac{R_f}{R_3} (v_3) \right] \dots\dots \text{(i)}$$

Given,

$$v_o = -2v_1 + 3v_2 + 4v_3 = -[2v_1 - 3v_2 - 4v_3] \dots\dots (ii)$$

From equation (i) & (ii),

$$\frac{R_f}{R_1} = 2, \frac{R_f}{R_2} = 3, \frac{R_f}{R_3} = 4$$

$$\therefore R_f = 4R_3$$

$$\text{Let } R_3 = 10 \text{ k}\Omega$$

$$\therefore R_f = 4 \times 10 = 40 \text{ k}\Omega$$

$$R_f = 3R_2 \Rightarrow R_2 = \frac{R_f}{3} = \frac{40}{3} = 13.33 \text{ k}\Omega$$

$$R_f = 2R_1 \Rightarrow R_1 = \frac{R_f}{2} = \frac{40}{2} = 20 \text{ k}\Omega$$

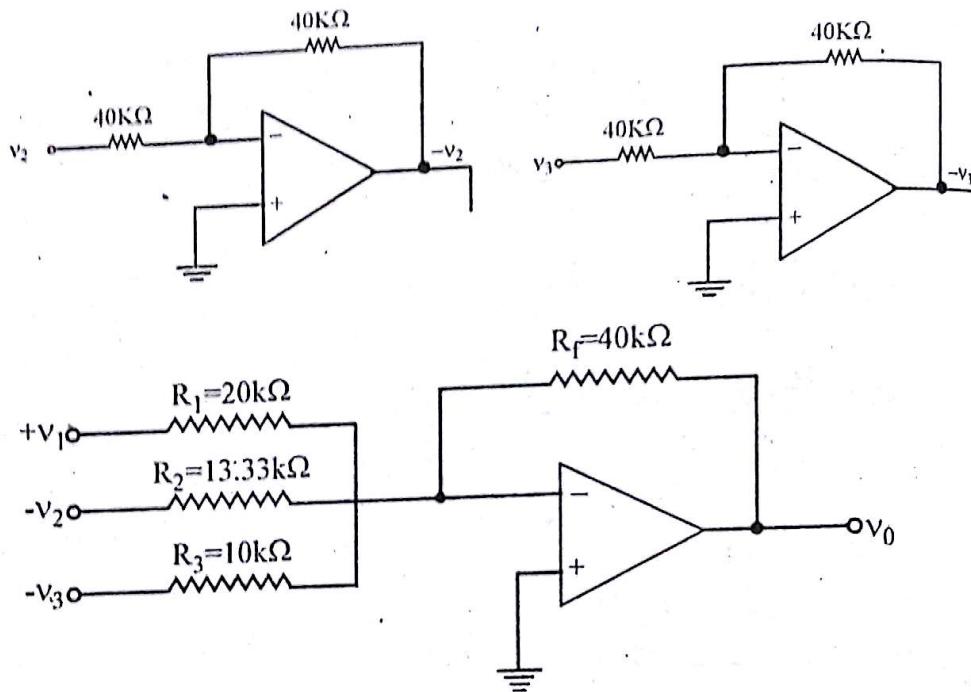


Fig.: Circuit realization of $v_o = -2v_1 + 3v_2 + 4v_3$

Problem 4.2

Design a summer circuit using op-amp to get the output voltage as: $v_o = -(v_1 + 10v_2 + 25v_3)$. [2070 Magh]

Solution:

For a summer circuit,

$$v_o = - \left[\frac{R_f}{R_1}(v_1) + \frac{R_f}{R_2}(v_2) + \frac{R_f}{R_3}(v_3) \right] \dots\dots (i)$$

Given,

From equations (i) and (ii), we get

$$\frac{R_f}{R_1} = 1, \frac{R_f}{R_2} = 10, \frac{R_f}{R_3} = 25$$

$$\therefore R_f = 25R_3$$

Let $R_3 = 10 \text{ k}\Omega$

$$\therefore R_f = 25 \times 10 = 250 \text{ k}\Omega$$

$$R_f = 10R_2 \Rightarrow R_2 = \frac{R_f}{10} = \frac{250}{10} = 25 \text{ k}\Omega$$

$$R_f = R_l \Rightarrow R_l = R_f = 250 \text{ k}\Omega$$

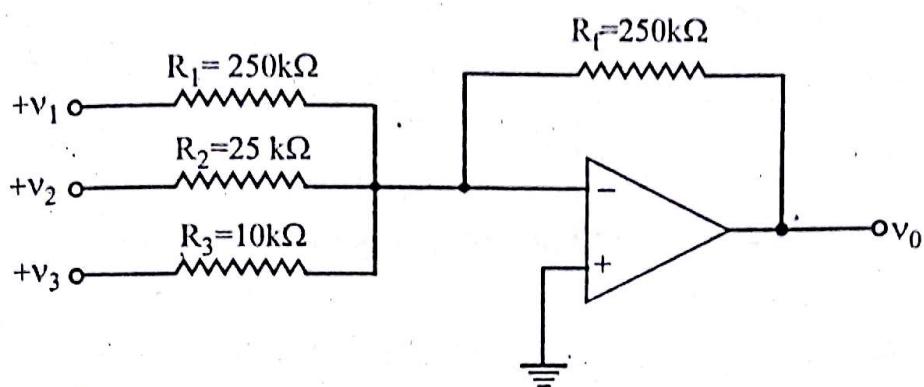


Fig.: Circuit realization of $v_o = -(v_1 + 10v_2 + 25v_3)$

FEEDBACK

The process of injecting a fraction of output energy of some device back to the input is known as feedback.

Positive Feedback

When the feedback energy (voltage or current) is in phase with the input signal and thus aids it, it is called positive feedback.

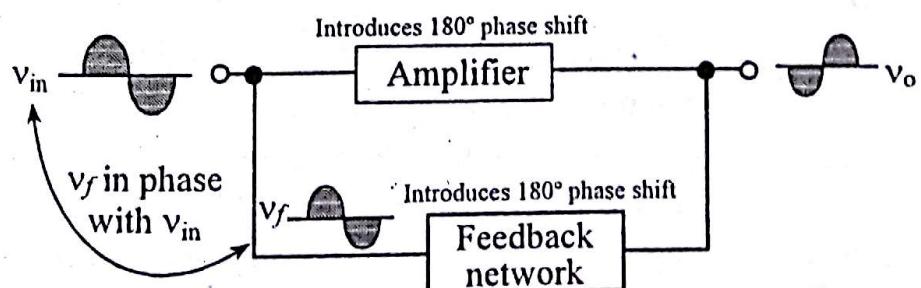


Figure 4.12 Illustration of positive feedback

One important use of positive feedback is in oscillators about which we will be discussing shortly.

Disadvantages of positive feedback

- i. Increased distortion
- ii. Instability

Negative Feedback

When the feedback energy (voltage or current) is out of phase with the input signal and thus opposes it, it is called negative feedback.

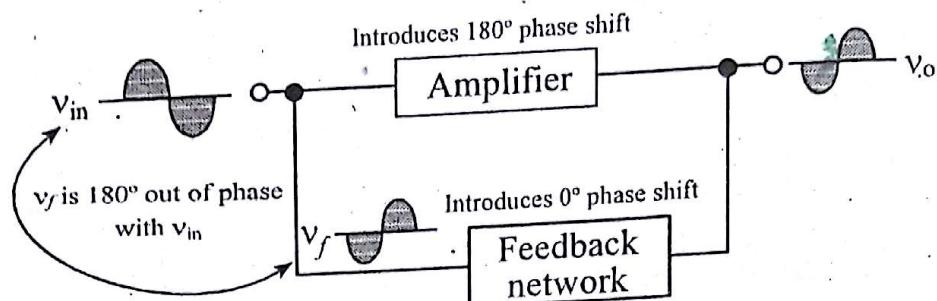


Figure 4.13 Illustration of negative feedback

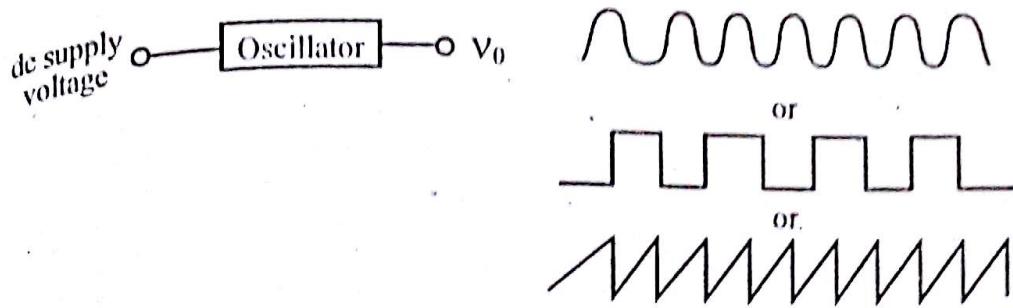
The concept of negative feedback is frequently employed in amplifiers.

Advantages of negative feedback

- i. Gain stability of the amplifier can be achieved.
- ii. Reduces non-linear distortion in large signal amplifiers.
- iii. Improves frequency response of the amplifier.
- iv. Increases circuit stability of the amplifier.
- v. Increases input impedance and decreases output impedance of the amplifier.

OSCILLATOR

An oscillator is a circuit that produces a periodic wave form on its output with only the dc supply voltage as an input. A repetitive input signal is not required except to synchronize oscillations in some applications. The output voltage can be either sinusoidal or non-sinusoidal, depending on the type of oscillator. Two major classifications for oscillators are feedback oscillators and relaxation oscillators.



FEEDBACK OSCILLATORS

One type of oscillator is the feedback oscillator, which returns a fraction of the output signal to the input with no net phase shift, resulting in a reinforcement of the output signal. After oscillations are started, the loop gain is maintained at 1.0 to maintain oscillations. A feedback oscillator consists of an amplifier for gain and a positive feedback circuit that produces phase shift and provides attenuation. Hence, feedback oscillator is based on the principle of positive feedback.

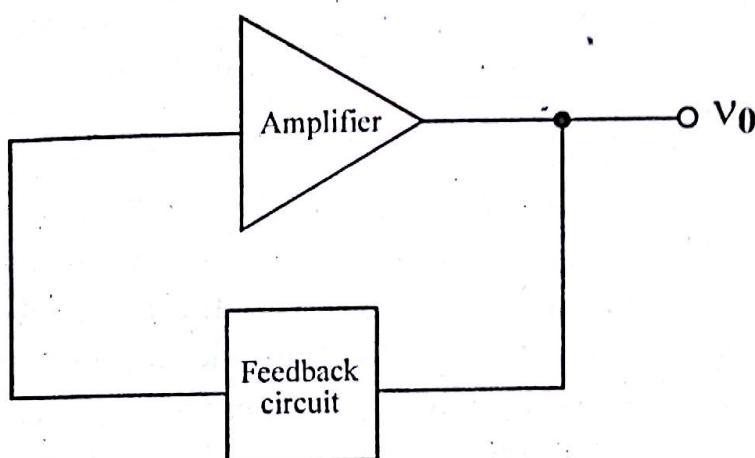


Figure 4.14 Basic elements of a feedback oscillator

BARKHAUSEN CRITERIA

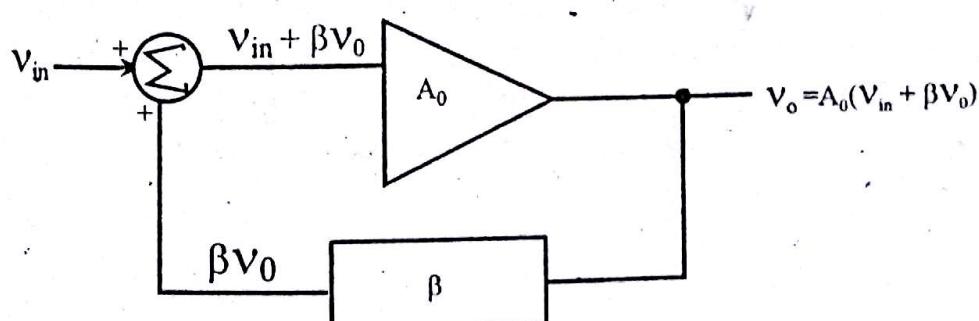


Figure 4.15 Block diagram of a positive feedback amplifier

The overall voltage gain of a positive feedback amplifier is calculated as

$$A_o = \frac{v_o}{v_{in} + \beta v_o}$$

$$\text{or, } v_o(1 - \beta A_o) = A_o v_{in}$$

$$\text{or, } \frac{V_o}{V_{in}} = \frac{A_0}{1 - \beta A_0}$$

$$\therefore A = \frac{A_0}{1 - \beta A_0} \dots \dots \dots \quad (i)$$

where A is closed-loop gain and A_o is open-loop gain. If the product (βA_o) is made equal to unity, then the denominator of equation (i) is zero. It means that the gain (A) will increase to infinity. Of course, the output of the feedback amplifier, in actual practice, cannot be infinite. Therefore, the condition $(1 - \beta A_o = 0)$ represents that there will be an output voltage, whose frequency is completely different from the input signal. In other words, the circuit has stopped amplifying and started oscillating. It may be noted that the oscillations will not be maintained if the value of βA_o is less than unity.

We know that an amplifier reverses the phase of an input signal at its output. It means that amplifier causes a phase shift of 180° between the input and output signals. In order to provide positive feedback, the feedback network must provide a phase shift of 180° , so as to provide a signal with a phase shift of 360° or 0° at the amplifier input.

The above two conditions for positive feedback i.e., $\beta A_o = 1$ and the net phase shift around the loop equal to 360° or 0° are called Barkhausen criterion for oscillation. Mathematically, the Barkhausen criterion may be stated as follows:

$$\beta A_0 = 1$$

$$\angle B A_0 = 0^\circ$$

Thus, if βA_0 is a complex quantity, then its real part must be equal to unity and imaginary part equal to zero i.e.,

If $\beta A_o = 1$, then $A \rightarrow \infty$. We know that we cannot achieve infinite gain in an amplifier. So, what does this result infer in physical terms? It means that a vanishing small input voltage would give rise to finite (i.e., a definite amount of) output voltage even when the input signal is zero. Thus, once the circuit receives the input trigger, it would become an oscillator; generating oscillations with no external signal source.

$$\beta A_0 = 1 + j0$$

However, an oscillator in which the quantity βA_0 is exactly unity is not realizable in practice. In every practical oscillator, the quantity βA_0 is slightly larger than unity.

SQUARE WAVE GENERATOR (ASTABLE MULTIVIBRATOR)

A simple op-amp square wave generator is shown in Figure

4.16. Also called a free running oscillator, the principle of generation of square wave output is to force an op-amp to operate in the saturation region. The fraction $\beta = R_2/(R_1 + R_2)$ of the output is fed back to the (+) input terminal. Thus,

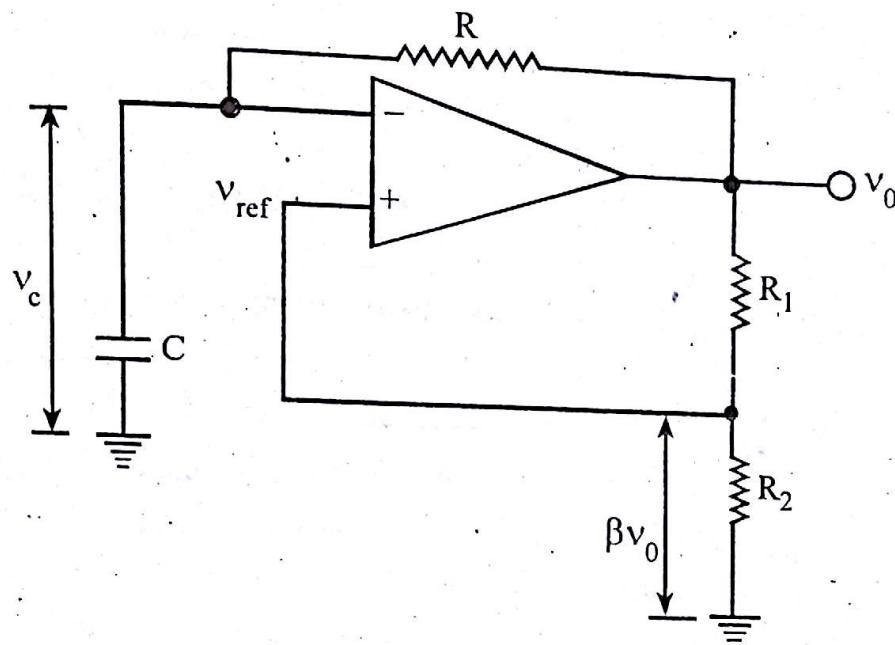


Figure 4.16 Square wave generator

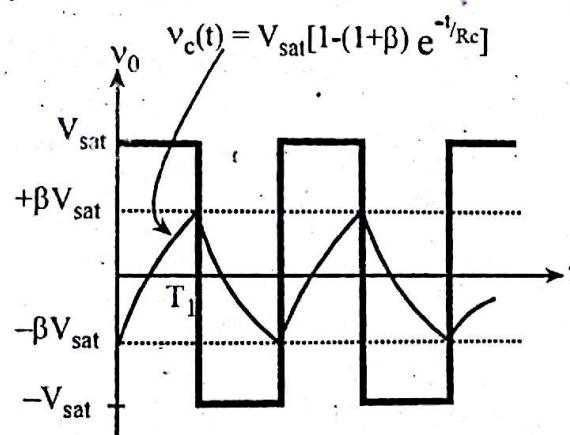


Figure 4.17 Waveforms

the reference voltage, v_{ref} is βV_0 fed back and may take values as $+ \beta V_{sat}$ or $- \beta V_{sat}$. The output is also fed back to the (-) input terminal after integrating by means of a low-pass RC combination. Whenever input at the (-) input terminal just exceeds v_{ref} , switching takes place resulting in a square wave output. In a stable multivibrator, both the states are quasi stable.

Consider an instant of time when the output is at $+ V_{sat}$. The capacitor now starts charging towards $+ V_{sat}$ through resistance R , as shown in Figure 4.17. The voltage at the (+) input terminal is held at $+ \beta V_{sat}$ by R_1 and R_2 combination. This condition continues as the charge on C rises, until it has just exceeded $+ \beta V_{sat}$, the reference voltage. When the voltage at the (-) input terminal becomes just greater than this reference voltage, the output is driven to $-V_{sat}$. At this instant, the voltage on the capacitor is $+ \beta V_{sat}$. It begins to discharge through R , that is, charges toward $-V_{sat}$. When the output voltage switches to $-V_{sat}$, the capacitor charges more and more negatively until its voltage just exceeds $- \beta V_{sat}$. The output switches back to $+V_{sat}$. The cycle repeats itself.

The frequency is determined by the time it takes the capacitor to charge from $- \beta V_{sat}$ to $+ \beta V_{sat}$ and vice versa. The voltage across the capacitor is given as

$$v_c(t) = V_{app} + (V_{initial} - V_{app}) e^{-t/RC}$$

where $V_{app} = +V_{sat}$ and $V_{initial} = - \beta V_{sat}$

$$\text{or, } v_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat}) e^{-t/RC} = V_{sat} - V_{sat}(1+\beta)e^{-t/RC} \dots\dots(i)$$

At $t = T_1$, voltage across the capacitor reaches βV_{sat} and switching takes places.

Therefore, from equation (i),

$$v_c(T_1) = V_{sat} - V_{sat}(1+\beta) e^{-T_1/RC}$$

$$\text{or, } \beta V_{sat} = V_{sat} - V_{sat}(1+\beta) e^{-T_1/RC}$$

After algebraic manipulation, we get

$$T_1 = RC \ln \frac{1+\beta}{1-\beta}$$

Total time period, $T = 2T_1 = 2RC \ln \frac{1+\beta}{1-\beta}$

Frequency of oscillation (f_0) = $\frac{1}{T} = \frac{1}{2RC \ln \frac{1+\beta}{1-\beta}}$

TRIANGULAR WAVE GENERATOR

A triangular wave can be simply obtained by integrating a square wave as shown in Figure 4.18. It is obvious that the frequency of the square wave and triangular wave is same. Although the amplitude of the square wave is constant at $\pm V_{sat}$, the amplitude of the triangular wave will decrease as the frequency increases. This is because the reactance of the capacitor C_2 in the feedback circuit decreases at high frequencies. A resistance R_4 is connected across C_2 to avoid the saturation problem at low frequencies as in the case of practical integrator.

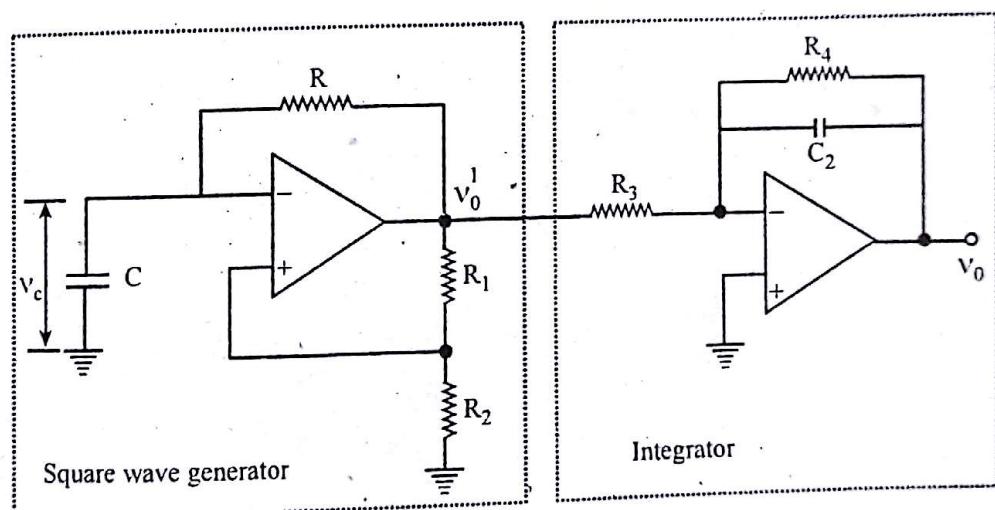


Figure 4.18 Circuit diagram of a triangular wave generator

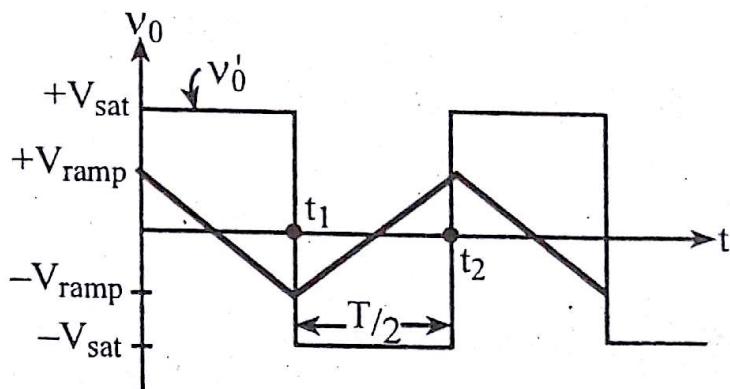


Figure 4.19 Triangular wave generated from square wave

WIEN-BRIDGE OSCILLATOR

The Wien-bridge oscillator is an oscillator circuit which is used to generate the sinusoidal waveform of desired frequency and amplitude. It is the standard oscillator circuit for low to moderate frequencies, in the range of 5Hz to about 1MHz. It is almost always used in commercial audio generators and is usually preferred for other low-frequency applications.

The basic circuit of Wien-bridge oscillator consists of an op-amp connected in the non-inverting configuration, with a closed-loop gain of $1+R_2/R_1$. In the feedback path of this positive-gain amplifier, an RC network is connected.

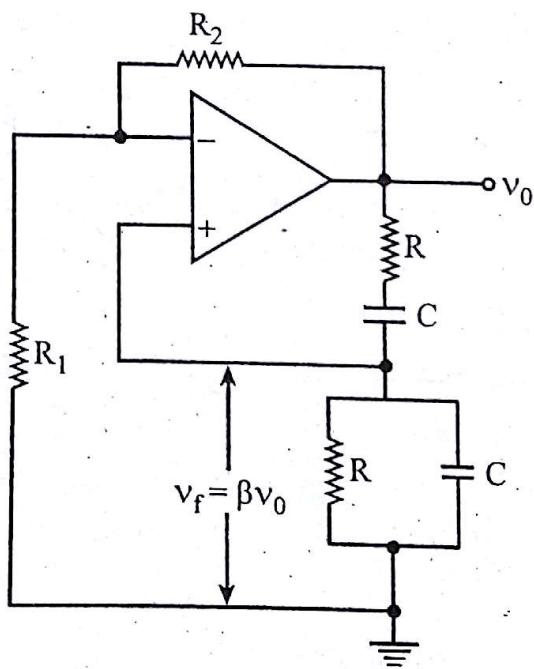


Figure 4.20 Basic Wien-bridge oscillator

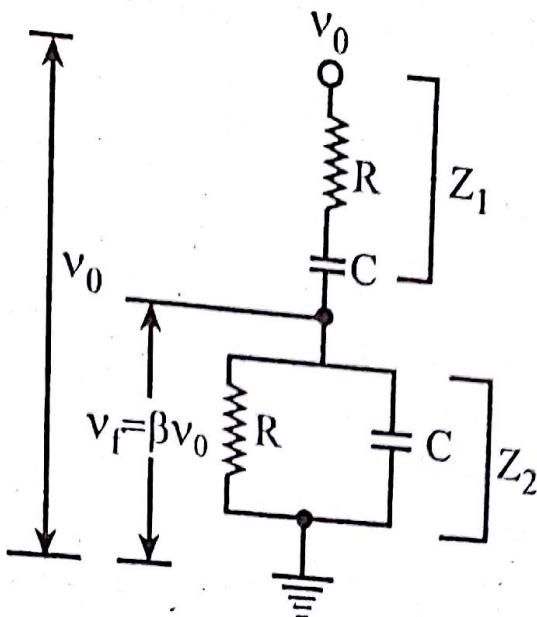


Figure 4.21 Frequency determining network

From Figure 4.21,

$$Z_1 = R - jX, Z_2 = \frac{(R)(-jX)}{R-jX} = \frac{-jRX}{R-jX}$$

Using voltage division rule,

$$v_f = \frac{Z_2}{Z_1 + Z_2} (v_o) = \frac{\frac{-jRX}{R-jX}}{(R-jX) + \frac{-jRX}{R-jX}} (v_o)$$

$$\text{or, } \frac{v_f}{v_o} = \frac{-jRX}{(R-jX)^2 - jRX}$$

$$\text{or, } \frac{v_f}{v_o} = \frac{-jRX}{(R^2 - X^2 - 2jRX) - jRX}$$

$$\text{or, } \frac{v_f}{v_o} = \frac{-jRX}{(R^2 - X^2) - 3jRX}$$

$$\text{or, } \frac{v_f}{v_o} = \frac{-j^2 RX}{j(R^2 - X^2) - 3j^2 RX}$$

$$\text{or, } \frac{v_f}{v_o} = \frac{RX}{j(R^2 - X^2) + 3RX} \dots\dots\dots (i)$$

For zero phase shift (to satisfy Barkhausen criteria), the j operator should vanish and hence, we have

$$R^2 - X^2 = 0$$

$$\text{or, } R^2 = X^2$$

$$\text{or, } R^2 = \left(\frac{1}{2\pi f C}\right)^2$$

$\therefore f = \frac{1}{2\pi R C}$ which is the expression for frequency of oscillation.

Therefore, equation (i) is reduced to

$$\frac{v_f}{v_o} = \frac{-RX}{0-3RX} = \frac{1}{3}$$

This means, there is a voltage attenuation of 3, so the amplifier should provide a voltage gain of at least 3 to produce oscillation.

For non-inverting configuration,

$$\text{Gain} = 1 + \frac{R_2}{R_1}$$

$$\text{or, } 3 = 1 + \frac{R_2}{R_1}$$

$$\text{or, } R_2 = 2R_1$$

Hence, R_2 should be selected twice R_1 in order to sustain oscillation.

COMMUNICATION SYSTEM

INTRODUCTION

Communication started with "wire telegraphy" in the eighteen forties, developing with telephony some decades later and radio at the beginning of 20th century. More recently, the use of "satellites" and "fiber optics" has made communications even more widespread with an increasing emphasis on computer and other data communications.

A modern "communication system" is first concerned with the sorting, processing, and sometimes storing of information before its transmission. Finally, we have reception, which may include processing steps such as decoding, storage, and interpretation.

In broad sense, the term "communication" refers to the sending, receiving, and processing of information by electronic means. Communication system is a system designed to send information from a source generating that information to one (point-to-point communication) or more (broadcasting) receivers of that information. Communication systems may be broadly divided into two types- analog communication systems and digital communication systems. In analog communication systems, the baseband message, which is to be transmitted, is in the form of an analog signal. In digital communication systems, the baseband message, which is to be transmitted, is in the form of a digital signal. The baseband message signal fed to the transmitter may be in digital form either because the source has produced it in that form or an analog waveform produced by the original source might have been sampled, quantized, and encoded to convert it into digital form before feeding to the transmitter as the baseband signal.

ANALOG AND DIGITAL SIGNALS

An analog signal is a signal with an amplitude (i.e., value of the signal at some fixed time) that varies continuously for all time. Electrical signals obtained from microphone, photo detector cell are examples of analog signals. Digital signals are those signals that are obtained when discrete time signals are quantized and then coded. The output of a digital computer is an example of a digital signal. Naturally, an analog signal may be converted into digital form by sampling in time, then quantizing, and coding.

MODULATION

It is defined as the process by which some characteristic of a carrier wave is varied in accordance with a modulating wave. The message signal is referred to as the modulating wave, and the result of the modulation process is referred to as the modulated wave.

Need for modulation

- i. The use of modulation permits multiplexing, that is, the simultaneous transmission of signals from several message sources over a common channel.
- ii. The size of the antenna needed for efficiently radiating electromagnetic energy is largely reduced due to modulation.
- iii. Modulation may be used to convert the message signal into a form less susceptible to noise and interference.

ANALOG MODULATION TECHNIQUES

i. Amplitude modulation (AM)

It is defined as the processes in which the amplitude of the carrier wave $c(t)$ is varied linearly with the message signal $m(t)$. For a sinusoidal carrier wave $c(t)$ defined by $c(t) = A_c \cos(2\pi f_c t)$, the standard form of an amplitude modulated (AM) wave is expressed as

$$s(t) = A_c [1 + k_a m(t)] \cos(2\pi f_c t)$$

where k_a = amplitude sensitivity of the modulator.

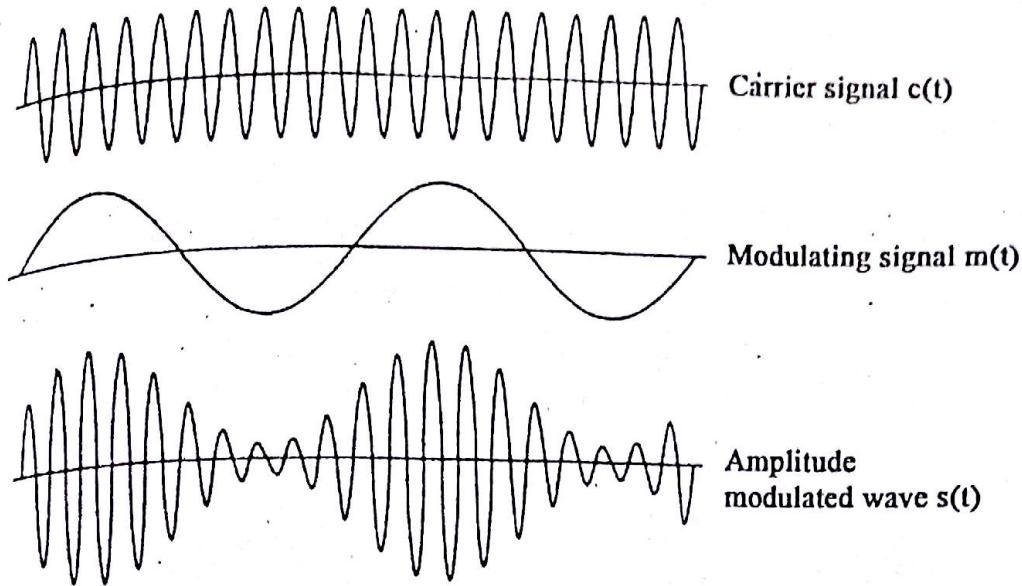


Figure 5.1 AM output with its waveforms

ii. Angle modulation

Either the phase or frequency of the carrier wave is varied according to the message signal. The angle modulated wave may be expressed as

$$s(t) = A_c \cos[\theta(t)] \text{ for } c(t) = A_c \cos(2\pi f_c t)$$

The instantaneous frequency of this wave is

$$f_i(t) = \frac{1}{2\pi} \frac{d\theta(t)}{dt}$$

a. Phase modulation (PM)

It is that form of angle modulation in which the angular argument $\theta(t)$ is varied linearly with the message signal $m(t)$, as shown by

$$\theta(t) = 2\pi f_c t + k_p m(t)$$

where k_p = phase sensitivity of the modulator.

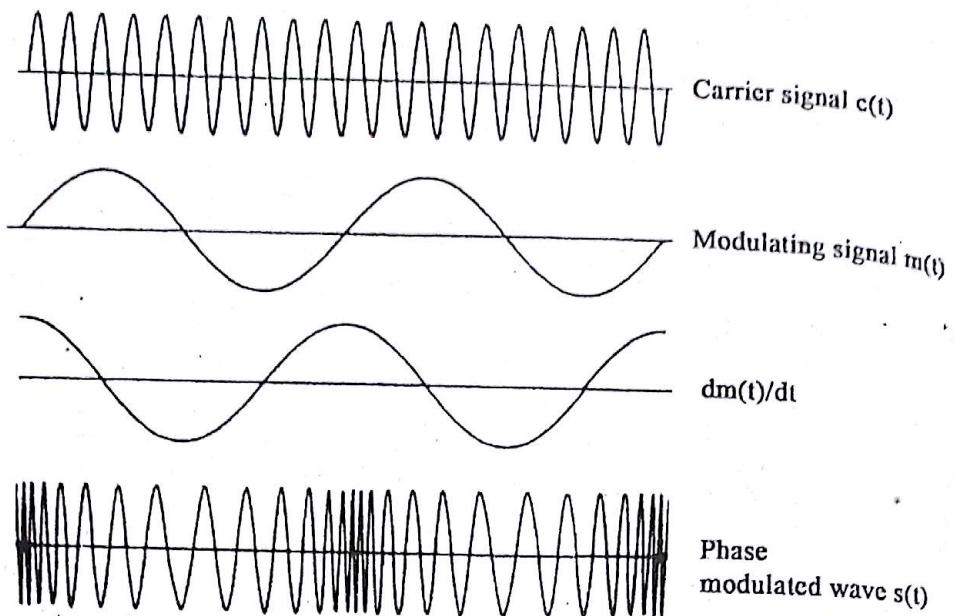


Figure 5.2 PM output with its waveforms

b. Frequency modulation (FM)

It is that form of angle modulation in which the instantaneous frequency $f_i(t)$ is varied linearly with the message signal $m(t)$, as shown by

$$f_i(t) = f_c + k_f m(t)$$

where k_f = frequency sensitivity of the modulator.

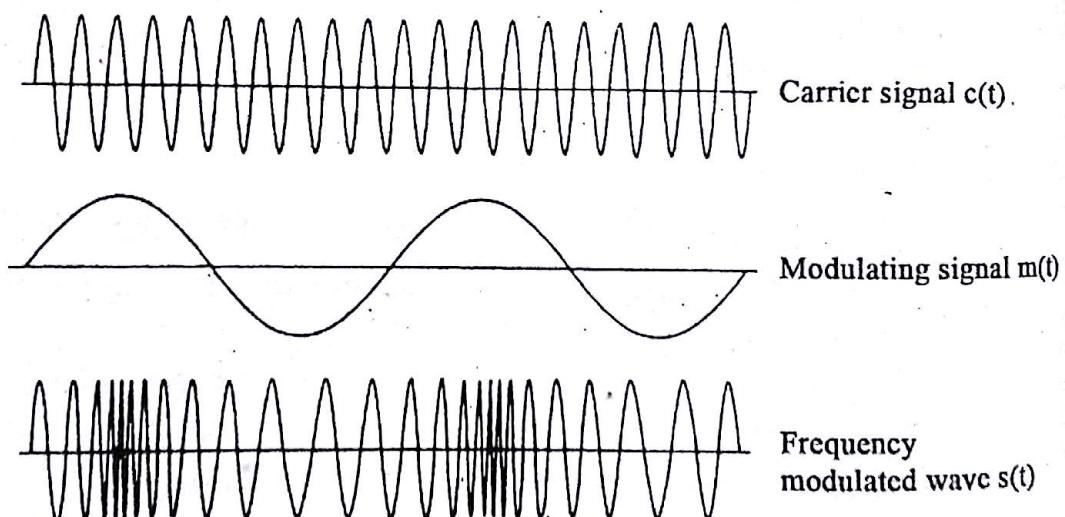


Figure 5.3 FM output with its waveforms

DIGITAL MODULATION TECHNIQUES

- i. Amplitude – shift keying (ASK)
- ii. Frequency – shift keying (FSK)
- iii. Phase – shift keying (PSK)

COMPONENTS OF A COMMUNICATION SYSTEM

The basic components of a communication system are:

i. Transmitter

This portion processes the message signal into a form suitable for transmission over the channel. Such an operation is called modulation.

ii. Communication channel

The function of the channel is to provide a physical connection between the transmitter output and the receiver input. There are two types of channels namely point-to-point channels, and broadcast channels. Examples of point-to-point channels include wire lines, microwave links, and optical fibers. An example of a broadcast channel is a satellite in geostationary orbit.

iii. Receiver

This portion processes the received signal to get message signal. Such an operation is called demodulation.

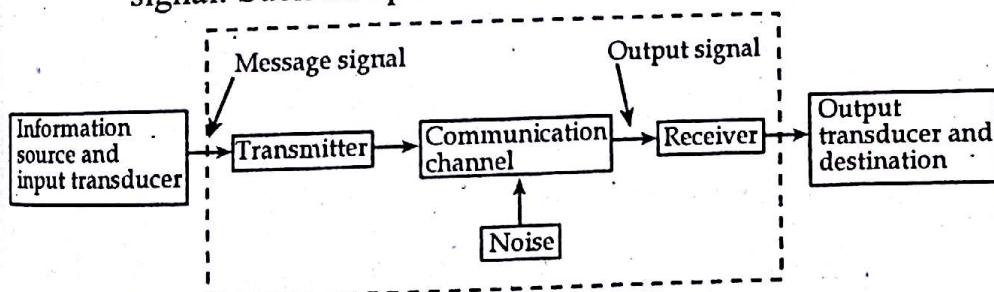


Figure 5.4 Block diagram of a communication system

DIGITAL COMMUNICATION SYSTEM

Digital communication system (DCS) is meant to transmit information that can be either analog signals or sequence of

symbols in digital form coming out from a source to a pre-assigned destination with maximum possible rate and accuracy.

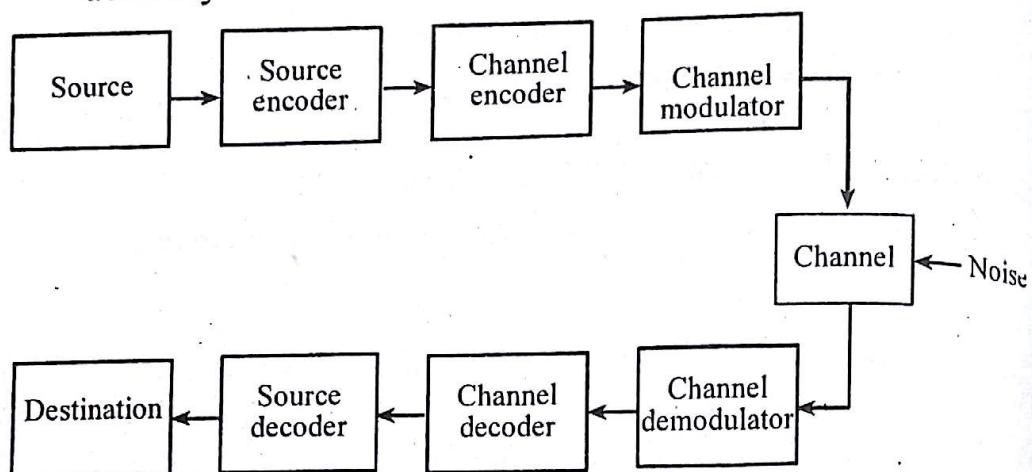


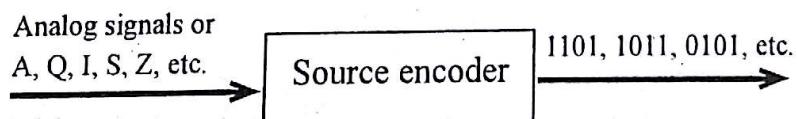
Figure 5.5 Functional block diagram of a digital communication system

i. **Source**

The source is where the information to be transmitted originates. This information/message may be available in digital form, as for instance, in the case of the output of a teletype system (sequence of symbols), or it may be available in an analog form (audio or video signal).

ii. **Source encoder**

Source encoder converts the analog signals or sequence of symbols into binary sequence of 1's and 0's.



iii. **Source decoder**

Source decoder converts the binary output of the channel decoder into its original analog form or sequence of symbols.

iv. **Channel encoder**

The channel encoder adds some error control bits (redundancy) to the bit streams of source encoder output. This is done in order to provide some amount of error-correction capability to the data being transmitted.

v. **Channel decoder**

The output sequence of digits from the channel demodulator are fed to the channel decoder. Using its knowledge of the type of coding performed by the channel encoder of the transmitting end, and using the redundancy introduced by the channel encoder, it produces as its output, the output of source coder of the transmitter with as few errors as possible.

vi. **Channel modulator**

Channel modulator is intended to convert bit streams from channel encoder to electrical waveform suitable for transmission over communication channel.

vii. **Channel demodulator**

Channel demodulator converts received electrical signal into sequence of bits with minimum error & maximum efficiency.

viii. **Channel**

The communication channel is a physical media (cable for wired communication or free space for wireless communication).

Advantages of digital communication over analog communication

- i. Increased immunity to channel noise and external interference.
- ii. Improved security of communication through the use of encryption.
- iii. A common format for the transmission of different kinds of message signals (e.g. voice signals, video signals, computer data).
- iv. It is easier and more efficient to multiplex several digital signals.
- v. Digital signal storage is relatively easy and inexpensive.

Optical Fibre

It is a flexible optically transparent fibre, usually made of glass or plastic, through which light can be transmitted by successive total internal reflections. Optical fibre consists of three parts namely protective layer, cladding, and core. The refractive index of the core is greater than that of the cladding.

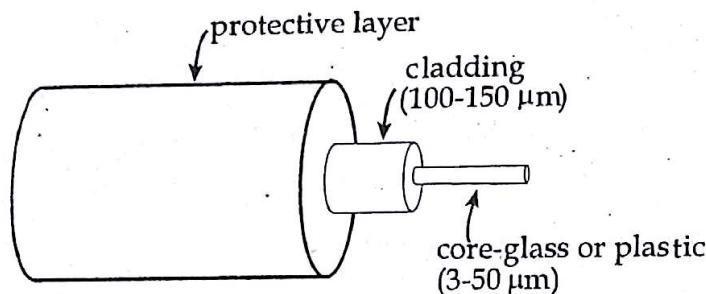


Figure 5.6 Optical fibre

A worthwhile information is that each optical fibre can carry as many as 2000 telephone conversations with less signal loss than in conventional telephone cables.

Basis of light propagation in optical fibre

The refractive index of the core, η_2 is greater than that of the cladding, η_1 . When light entering into the core from air is incident on the core-cladding interface at an angle greater than the critical angle, total internal reflection occurs and the light is propagated along the fibre.

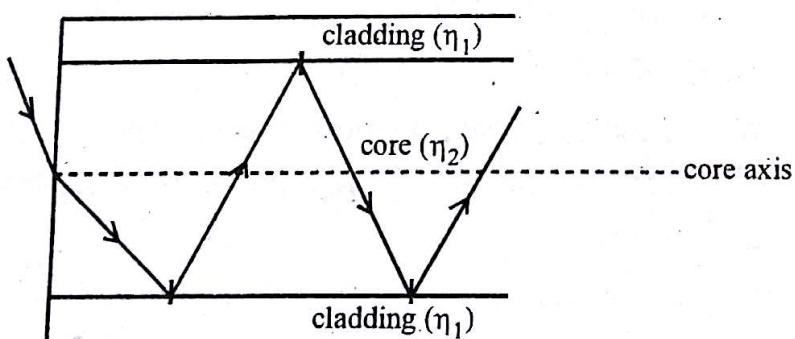


Figure 5.7 Propagation of light in optical fibre through total internal reflections

COMPONENTS OF OPTICAL FIBRE COMMUNICATION

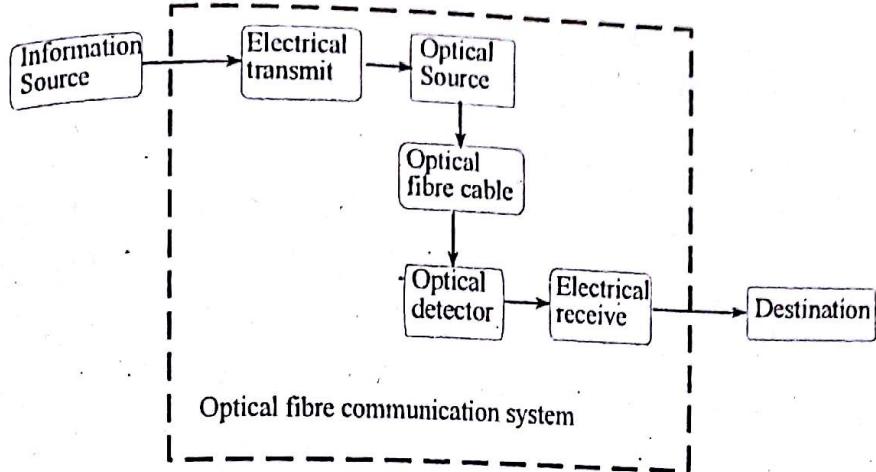


Figure 5.8 Functional block diagram of an optical fibre communication system

The information source provides an electrical signal to a transmitter comprising an electrical stage which drives an optical source to give modulation of the lightwave carrier. The optical source which provides the electrical-optical conversion may be either a semiconductor laser or light-emitting diode (LED). The transmission medium consists of an optical fibre cable and the receiver consists of an optical detector which drives a further electrical stage and hence, provides demodulation of the optical carrier. Photodiodes (p-n, p-i-n or avalanche) and, in some instances, phototransistors and photoconductors are utilized for the detection of the optical signal and the optical-electrical conversion. Thus, there is a requirement for electrical interfacing at either end of the optical link and at present, the signal processing is usually performed electrically.

The optical carrier may be modulated using either an analog or digital information signal. Analog modulation involves the variation of the light emitted from the optical source in a continuous manner. With digital modulation, however, discrete changes in the light intensity are obtained (i.e., on-off pulses).

Advantages of optical fibre communication

i. Enormous potential bandwidth

Optical fibre communication system provides a bandwidth of around 100 GHz.

ii. Small size and weight

Optical fibres are far smaller and much lighter than corresponding copper cables.

iii. Electrical isolation

Optical fibres are fabricated from glass or plastic polymer and are therefore insulators. As a result, optical fibres do not exhibit any electrical hazards.

iv. Immunity to interference

Optical fibres are free from electromagnetic interference (EMI).

v. Signal security

The light from optical fibres does not radiate significantly and therefore they provide a high degree of signal security.

vi. Low transmission loss

The losses in optical fibre are as low as 0.2 dB km^{-1} . Thus, it requires wider repeater spacing.

vii. Ruggedness and flexibility

Optical fibres have very high tensile strengths.

viii. System reliability and ease of maintenance

Few repeaters are needed and also the life time of the optical components is around 20 to 30 years. These factors make optical fibre to have higher system reliability and make the maintenance easier and cheaper.

ix. Potential low cost

The glass which is used for the fabrication of optical fibre is extracted from sand. So, optical fibre communication offers the potential for low cost communication in comparison with the copper conductors.

Disadvantages

- i. Joining fibre is difficult and expensive.
- ii. Fibre is not as mechanically robust as copper wire.
- iii. High investment cost.

ELECTROMAGNETIC WAVE

A wave of energy having a frequency within the electromagnetic spectrum and propagated as a periodic disturbance of the electromagnetic field when an electric charge oscillates or accelerates is called an electromagnetic wave. Electromagnetic waves can be imagined as a self-propagating transverse oscillating waves of electric and magnetic fields. Examples include radio waves, infrared, visible light, ultraviolet, x-rays, and gamma rays.

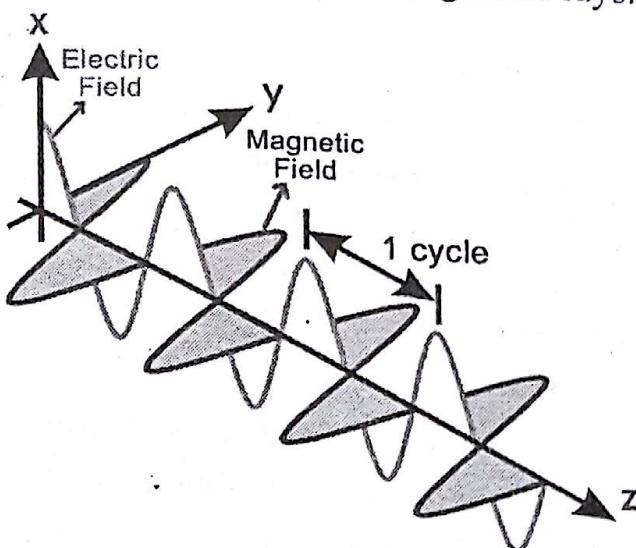


Figure 5.9 A plane linearly-polarized transverse electromagnetic wave

Consider an electromagnetic wave as shown in Fig. in which electric field vector is along x-axis and magnetic field vector along y-axis. The direction of propagation of electromagnetic wave (and thus, direction of the instantaneous power flow) is given by the Poynting vector \vec{S} which is expressed as

$$\vec{S} = \vec{E} \times \vec{H} \quad \left(\frac{\text{W}}{\text{m}^2} \right)$$

For $\vec{E} = E_x \hat{a}_x$, $\vec{H} = H_y \hat{a}_y$, we have

$$\vec{S} = E_x \hat{a}_x \times H_y \hat{a}_y = (E_x H_y) \hat{a}_z = S_z \hat{a}_z$$

The unit vector, \hat{a}_z in the expression for \vec{S} suggests electromagnetic wave is propagating along +z direction. Since we are dealing with a sinusoidal signal, the time-average

power density $\langle S_z \rangle$ is the quantity that has to be measured.

$$\langle S_z \rangle = \frac{1}{T} \int_0^T S_z dt; T = \text{time period of one cycle.}$$

Propagation of an electromagnetic wave

Electromagnetic waves are waves which can travel through the vacuum of outer space. Mechanical waves, unlike electromagnetic waves, require the presence of a material medium in order to transport their energy from one location to another.

Electromagnetic waves are created by the vibration of an electric charge. This vibration creates a wave which has both an electric and a magnetic component. An electromagnetic wave transports its energy through a vacuum at a speed of 3.00×10^8 m/s. The propagation of an electromagnetic wave through a material medium occurs at a net speed which is less than 3.00×10^8 m/s.

The mechanism of energy transport through a medium involves the absorption and reemission of the wave energy by the atoms of the material. When an electromagnetic wave impinges upon the atoms of a material, the energy of that wave is absorbed. The absorption of energy causes the electrons within the atoms to undergo vibrations. After a short period of vibrational motion, the vibrating electrons create a new electromagnetic wave with the same frequency as the first electromagnetic wave. While these vibrations occur for only a very short time, they delay the motion of the wave through the medium. Once the energy of the electromagnetic wave is reemitted by an atom, it travels through a small region of space between atoms. Once it reaches the next atom, the electromagnetic wave is absorbed, transformed into electron vibrations and then reemitted as an electromagnetic wave. While the electromagnetic wave will travel at a speed of c (3×10^8 m/s) through the vacuum of interatomic space, the absorption and reemission process causes the net speed of the electromagnetic wave to be less than c .

ANTENNAS

An antenna is a structure that is generally a metallic object, often a wire or group of wires, used to convert high-frequency current into electromagnetic waves, and vice-versa. An antenna may also be defined as any device that radiates electromagnetic energy into space, where the energy originates from a source that feeds the antenna through a transmission line or waveguide. The antenna thus serves as an interface between the confining line and space when used as a transmitter or between space and the line when used as a receiver. Apart from their different functions, transmitting and receiving antennas have similar characteristics, which means that their behaviour is reciprocal.

For wireless communication systems, the antenna is one of the most critical components. A good design of the antenna can relax system requirements and improve overall system performance. A typical example is TV for which the overall broadcast reception can be improved by utilizing a high-performance antenna. The antenna serves to a communication system the same purpose that eye and eyeglasses serve to a human.

Regardless of antenna type, all involve the same basic principle that radiation is produced by accelerated (or decelerated) charge. The basic equation of radiation may be expressed simply as

$$\dot{I}L = Q\dot{v}(A \text{ m s}^{-1})$$

where

\dot{I} = time-changing current, $A \text{ s}^{-1}$

L = length of current element, m

Q = charge, C

\dot{v} = time change of velocity which equals the acceleration of the charge, m s^{-2}

Thus, time-changing current radiates and accelerated charge radiates. For steady-state harmonic variation, we usually focus

on current. For transients or pulses, we focus on charge. The radiation is perpendicular to the acceleration, and the radiated power is proportional to the square of $\dot{I} L$ or Qv .

Types of antennas

1. Wire antennas
2. Aperture antennas
3. Micro strip antennas
4. Array antennas
5. Reflector antennas
6. Lens antennas

Basic antenna parameters

1. Radiation pattern
2. Radiation power density
3. Radiation intensity
4. Directivity
5. Gain
6. Antenna efficiency
7. Half - power beam width
8. Beam efficiency
9. Bandwidth
10. Polarization
11. Input impedance
12. Antenna vector effective length and equivalent areas
13. Antenna temperature

BROADCASTING AND COMMUNICATION

Broadcasting may be defined as the distribution of audio and/or video signals that is used to transmit programs to an audience. It can also be defined as the transmission of information through radio waves from a radio or television station, to the audience in far and near, through their receivers,

which help in decoding such information. Broadcasting can be "recorded" or "live" ..

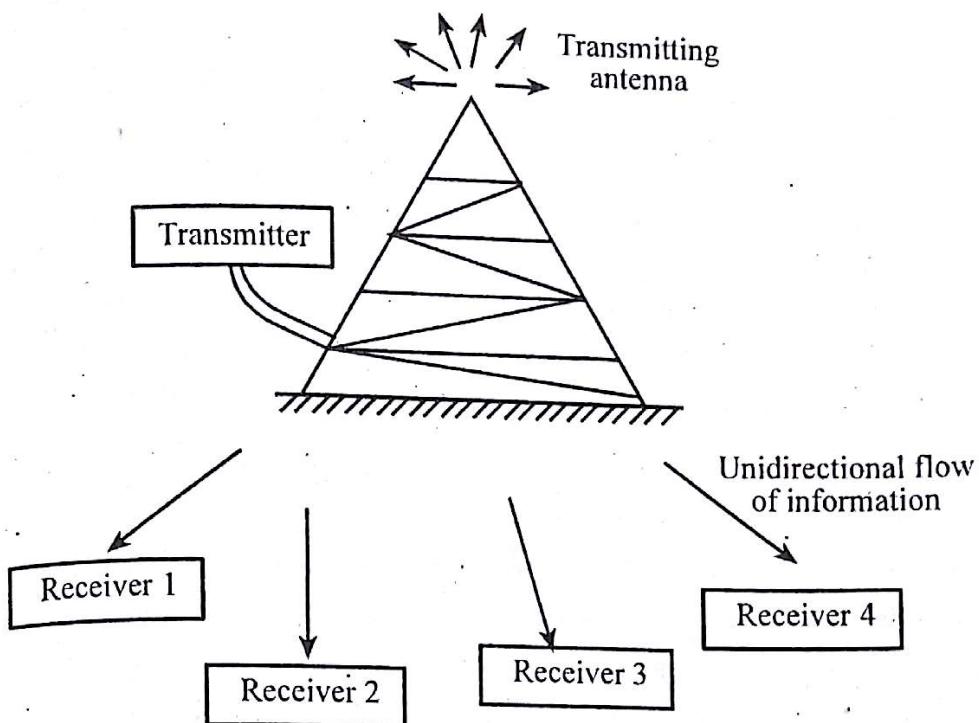


Figure 5.10 Broadcasting

Basically, broadcasting serves three broad purposes: to inform, educate, and entertain the audience. However, broadcast stations such as radio and television perform the following functions:

- i. **News function:** The broadcast station surveys the environment and provides information about things, happenings or going on in the environment. These are then reported in news form to the public.
- ii. **Opinion function:** The broadcast media provide an ample avenue for different shades of opinion to be aired in the society..
- iii. **Education function:** Through the broadcast media, people acquire new knowledge, attitudes, and skills, thus enabling them cope better with the society and life in general.

iv. **Commercial function:** Radio and television are often used for advertisements which help inform audiences about the existence of certain goods and services.

v. **Entertainment function:** Drama, comic, and musical programmes are aired on the stations to ease boredom.

WIRED & WIRELESS COMMUNICATION

To understand wired and wireless communication, it's wise we make a comparative study.

Wired communication	Wireless communication
i. Wired communication is a broad term that is used to describe any type of communication process that relies on the direct use of cables and wiring to transmit audio and visual data. Examples: traditional home telephone, internet access from desktop computer, cable television, etc.	i. Wireless communication is used to describe communication process using radio-frequency, infrared, microwave, or other types of electromagnetic or acoustic waves in place of wires, cables, or fibre optics to transmit signals or data. Examples: cell phones, cordless phones, wireless LANs, paging system, television remote control, etc.
ii. There is no mobility in wired communication.	ii. Wireless communication allows mobility.
iii. Wired communications have better transmission speeds and security.	iii. Wireless communications have lesser transmission speeds and security.
iv. It is expensive to set up infrastructure and is fixed once set up.	iv. It is much cheaper and easier to deploy, change, and upgrade infrastructure.

INTERNET & INTRANET

Internet is a global system of interconnected computer networks that use the standard Internet protocol suite (often

called TCP/IP, although not all applications use TCP) to serve billions of users worldwide. It is a network of networks that consists of millions of private, public, academic, business, and government networks, of local to global scope, that are linked by a broad array of electronic, wireless and optical networking technologies. Put it another way, the Internet is a society of thousands of organizations and networks that work together without government or centralized management.

The Internet is now used by many people: educators, telecommuters, librarians, hobbyists, researchers, government officials, and business personnel. It is used for a variety of purposes: from communicating with each other to accessing valuable information and resources. The Internet provides connectivity for a wide range of application processes called "network services". One can exchange electronic mail, access and participate in discussion forums, search databases, browse indexes, transfer files, and so forth.

Intranet is the generic term for a collection of private computer networks within an organization. It may consist of many interlinked local area networks and also use leased lines in the wide area network. Typically, an intranet includes connections through one or more gateway computers to the outside Internet. The intranet is an inexpensive yet very effective alternative to other forms of internal communication in that it provides the mechanism to eliminate paper while increasing accessibility to information. Examples of applications of intranet-based information include internal telephone books, procedure manuals, training materials, and requisition forms. All of this information can be converted to electronic form on the Web and updated in a low-cost manner. To prepare for a meeting, an executive could tap into the finance department's home page, which has hyperlinks to information such as revenues and forecasts. Employees can order supplies from an electronic catalog maintained by the purchasing department. Thus, the main purpose of an intranet is to share company information and computing resources

among employees. An intranet can also be used to facilitate working in groups and for teleconferences. In many organizations, intranets are protected from unauthorized external access by means of a network gateway and firewall.

Similarities in Internet and Intranet

1. Intranet uses the Internet protocols such as TCP/IP and FTP.
2. Intranet sites are accessible via web browser in similar way as websites in Internet.
3. In Intranet, own instant messengers can be used as similar to yahoo messenger/gtalk over the Internet.

Differences between Internet and Intranet

1. Internet is general to PCs all over the world whereas Intranet is specific to few PCs.
2. Internet is wider access and provides a better access to websites to large population whereas Intranet is restricted.
3. Internet is not as safe as Intranet as Intranet can be safely privatized as per the need.

ANSWERS TO SOME QUESTIONS

1. Draw a block diagram of AM super-heterodyne radio receiver. [2067 Chaitra]

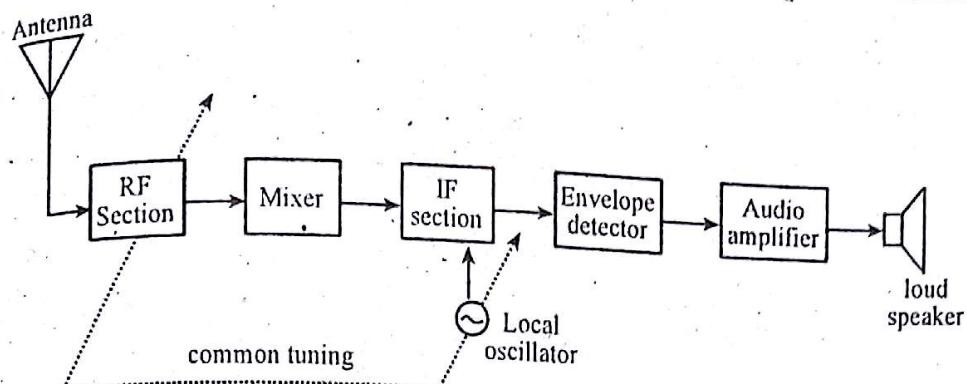


Fig.: Block diagram of an AM super-heterodyne radio receiver

2. Write short notes on: $\lambda/2$ dipole antenna (Half-wave dipole antenna) [2067 Mangsir].

The length of this antenna is equal to half of its wavelength as the name itself suggests. Dipoles can be shorter or longer than half the wavelength, but a tradeoff exists in the performance and hence, the half wave length dipole is widely used. It is made up of a wave element that is half the wavelength of the waves being transmitted and received. These types of antennas are only used with frequencies that are greater than 2MHz (any frequency below this has too large a wavelength for such an antenna to be constructed) and may be mounted either horizontally or vertically. The name dipole means two poles and the antenna does in fact consist of two "poles" or sections. These are normally equal in length, making the antenna what is termed a centre fed antenna. The power is applied to the dipole antenna itself through a feeder. Conversely, if the dipole antenna is used for receiving, the received signals are taken away to the receiver through a feeder. The feeder serves to transfer the power to or from the antenna with as little loss as possible.

The most common form of dipole has an electrical length of half a wavelength. As a result, this antenna is called a half-wave dipole.

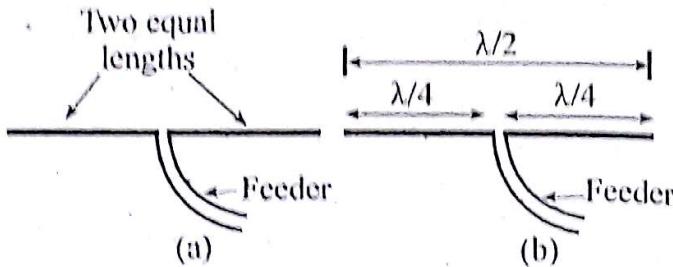


Fig.: (a) The basic dipole antenna (b) The basic half wave dipole antenna

Characteristics of $\lambda/2$ dipole antenna

- i. Directivity - 1.64
- ii. Gain, dB_i - 2.15
- iii. Half power bandwidth - 78°
- iv. Effective aperture - 0.13
- v. Radiation resistance - 73Ω

3. What is polarization?

Polarization is the characteristic that describes how the tip of a sinusoidally time-varying field vector at a point in space changes position with time. In the case of waves, when we talk about polarization, we refer to the electric field associated with the wave.

For fields having more than one component, the polarization can be linear, circular, or elliptical.

4. Comparison of FM and AM

1. FM receivers are more immune to noise than AM receivers.
2. There is less adjacent-channel interference in FM than in AM due to provision of a guard band between commercial FM stations.
3. In FM, all the transmitted power is useful whereas in AM, most of the transmitted power is carrier power, which does not contain any information.
4. FM transmitters, and receivers are more complex and costly than that of AM.

5. FM broadcast requires a much wider channel (typically 200 kHz) in comparison to AM broadcast requiring 10 kHz.

5. Block diagram of an AM transmitter

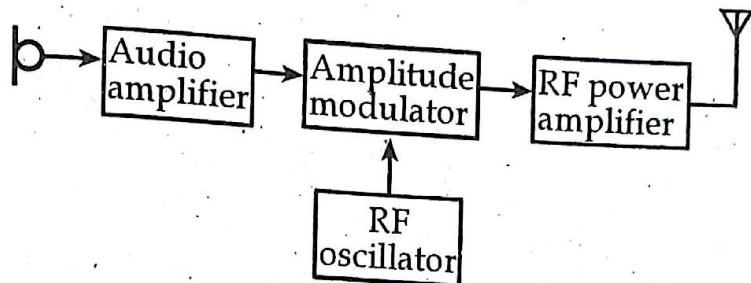
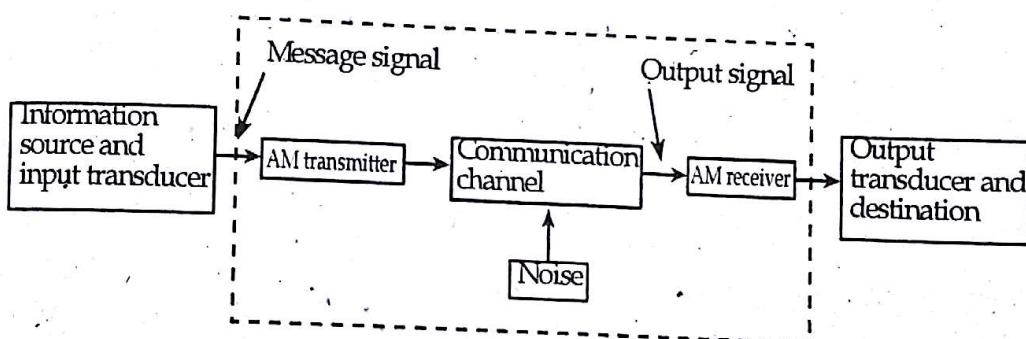


Fig.: Block diagram of an AM transmitter.

6. Explain amplitude modulation communication system with the help of necessary block diagrams. [2070 Bhadra]

Solution:



[Explain yourself]

Digital Electronics

INTRODUCTION

Digital systems have prominent role in everyday life. Digital systems are used in communication, business transactions, traffic control, medical treatment, the Internet, and many other commercial, industrial, and scientific enterprises. We have digital telephones, digital television, digital versatile discs, digital cameras, handheld devices, and of course digital computers.

A digital circuit operates in a binary manner i.e., only in two states. The output of such a circuit is either a low or a high voltage; no other values of the output voltage are allowed. The exact value of the output voltage is unimportant if the voltage is distinguishable as low or high. The two states of the output of a digital circuit are designated 0 (zero) and 1 (one). In most digital circuits, diodes and transistors are used as switches to change from one voltage level to another. Since a switch may be open or closed, the two output states of a digital circuit may also be designated 'off' or 'on' states.

NUMBER SYSTEMS

Arithmetic operations using decimal numbers are quite common. However, in logical design, it is necessary to perform manipulations in the so-called binary system of numbers. Hexadecimal number system is a compact way of displaying or writing binary numbers because long binary numbers are difficult to read and write. So, while writing a 16-bit instruction for a microprocessor system, it is much more efficient to use hexadecimal or octal rather than writing it in 1s and 0s.

The fundamental concepts involved in dealing with number systems other than decimal will be studied with the help of a table that follows.

Decimal (base 10)	Binary (base 2)	Octal (base 8)	Hexadecimal (base 16)
00	0000	00	0
01	0001	01	1
02	0010	02	2
03	0011	03	3
04	0100	04	4
05	0101	05	5
06	0110	06	6
07	0111	07	7
08	1000	10	8
09	1001	11	9
10	1010	12	A
11	1011	13	B
12	1100	14	C
13	1101	15	D
14	1110	16	E
15	1111	17	F

Table 6.1 List of the first 16 numbers in the decimal, binary, octal, and hexadecimal number systems.

Binary-Coded Decimal (BCD)

Binary codes for decimal digits require a minimum of 4-bits. It is a straight assignment of binary equivalent to each digit. For example, 95 when converted into binary is equal to 1011111. But, when same number is represented in BCD code, each decimal digit is represented by 4-bits as: 1001 for 9 and 0101 for 5. Thus, the BCD equivalent will be 1001 0101.

Now, we will switch our mind to learning conversion techniques with the help of examples.

Problem 6.1

Convert decimal 41 to binary

Solution:

Conversion of a decimal number into its binary equivalent consists of progressive division of the decimal number by 2 until a quotient of 0 is obtained. Writing the remainders after each division in the reverse order, as indicated by the arrow, will give the binary equivalent.

Integer	Remainder
41	
20	1
10	0
5	0
2	1
1	0
0	1

$= (101001)_2$

Problem 6.2

Convert decimal 153 to octal

Solution:

Conversion of a decimal number into its octal equivalent consists of progressive division of the decimal number by 8 until a quotient of 0 is obtained. Writing the remainders after each division in the reverse order, as indicated by the arrow, will give the octal equivalent.

Integer	Remainder
153	
19	1
2	3
0	2

$= (231)_8$

Problem 6.3

Convert $(235)_{10} \rightarrow (\)_{16}$

Solution:

Conversion of a decimal number into its hexadecimal equivalent consists of progressive division of the decimal number by 16 until a quotient of 0 is obtained. Writing the remainders after each division in the reverse order, as indicated by the arrow, will give the hexadecimal equivalent. Also, note that numbers 10-15 in the hexadecimal number system are denoted by corresponding alphabets.

Integer	Remainder
235	
14	11 (B) ↑
0	14 (E)
$= (EB)_{16}$	

Problem 6.4

Convert $(0.6875)_{10}$ to binary

Solution:

In order to accomplish this conversion, the number is multiplied by 2 and the result is separated as integer and fraction. The fraction is considered as a new number and is again multiplied by 2 separating the result as integer and fraction. This process continues until we get zero in the fraction or certain level of accuracy is achieved. Finally, collecting all the integers in the direction shown by arrow will give binary equivalent.

Integer	Fraction
$0.6875 \times 2 = 1$	+ 0.3750
$0.3750 \times 2 = 0$	+ 0.7500
$0.7500 \times 2 = 1$	+ 0.5000
$0.5000 \times 2 = 1$	+ 0.0000
$= (0.1011)_2$ ↓	

Problem 6.5

Convert $(0.513)_{10}$ to octal

Solution:

In this conversion, we repeat the process as done in Problem 6.4 but the number is multiplied by 8 instead of 2.

Integer	Fraction
$0.513 \times 8 = 4$	+ 0.104
$0.104 \times 8 = 0$	+ 0.832
$0.832 \times 8 = 6$	+ 0.656
$0.656 \times 8 = 5$	+ 0.248
$= (0.4065)_8$	

Problem 6.6Convert $(0.85)_{10}$ to $(\cdot)_{16}$ **Solution:**

Integer	Fraction
0.85×16	13(D)
0.60×16	9
0.60×16	9
	$= (0.D99)_{16}$

Problem 6.7Convert $(41.6875)_{10}$ to $(\cdot)_{2}$ **Solution:**

We convert integer part (41) & fraction part (0.6875) separately as

Integer	Remainder
41	
20	1
10	0
5	0
2	1
1	0
0	1

$$\therefore (41)_{10} = (101001)_2$$

Integer Fraction

$0.6875 \times 2 =$	1	+	0.3750
$0.3750 \times 2 =$	0	+	0.7500
$0.7500 \times 2 =$	1	+	0.5000
$0.5000 \times 2 =$	1	+	0.0000

$$\therefore (0.6875)_{10} = (0.1011)_2$$

$$\text{Hence, } (41.6875)_{10} = (101001.1011)_2$$

Problem 6.8

Convert $(153.513)_{10}$ to $()_8$

Solution:

We convert integer part (153) & fraction part (0.513) separately as done before.

$$\text{Hence, } (153.513)_{10} = (231.4065)_8$$

Problem 6.9

Convert $(65.35)_{10}$ to $()_{16}$

Solution:

We convert integer part (65) & fraction part (0.35) separately as

Integer Remainder

$$\begin{array}{r} 65 \\ 4 \quad \quad 1 \uparrow \\ 0 \quad \quad 4 \end{array}$$

$$\therefore (65)_{10} = (41)_{16}$$

Integer Fraction

$$\begin{array}{l} 0.35 \times 16 = \left| \begin{array}{r} 5 \\ 9 \end{array} \right. + 0.60 \\ 0.60 \times 16 = \downarrow 9 + 0.60 \\ 0.60 \times 16 = \downarrow 9 + 0.60 \end{array}$$

$$\therefore (0.35)_{10} = (0.599)_{16}$$

$$\text{Hence, } (65.35)_{10} = (41.599)_{16}$$

Problem 6.10

$(165)_{10} \rightarrow ()_{BCD}$

Solution:

$$(165)_{10} = (0001 \ 0110 \ 0101)_{BCD}$$

Note: In BCD system, we shouldn't omit the leftmost 0s.

Problem 6.11

$$(110101)_2 \rightarrow ()_{10}$$

Solution:

The rightmost digit of the binary number has the weightage of 2^0 and the power of 2 will increase by 1 for each successive digit from right to left. It is also called as the place value of binary digits. The sum of products of binary digits and place value provides its equivalent decimal value.

$$\begin{aligned}(110101)_2 &= 1 \times 2^5 + 1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 \\ &= (53)_{10}\end{aligned}$$

Problem 6.12

$$(11011.11)_2 \rightarrow ()_{10}$$

Solution:

The first binary digit to the left of binary point has a place value of 2^0 . The place value of binary digits is increased by 1 for each successive digit towards left. The first binary digit to the right of binary point has a place value of 2^{-1} . The place value of binary digits is decreased by 1 for each successive digit towards right. The sum of products of binary digits and place value provides its equivalent decimal value.

$$\begin{aligned}(11011.11)_2 &= 1 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 1 \times 2^{-2} \\ &= (27.75)_{10}\end{aligned}$$

Problem 6.13

$$(4021.2)_5 \rightarrow ()_{10}$$

Solution:

We apply the same process as done in **Problem 6.12** but noting that place value of digits are 5 raised to different numbers corresponding to the position of digits.

$$\begin{aligned}(4021.2)_5 &= 4 \times 5^3 + 0 \times 5^2 + 2 \times 5^1 + 1 \times 5^0 + 2 \times 5^{-1} \\ &= (511.4)_{10}\end{aligned}$$

Problem 6.14

$$(123.4)_8 \rightarrow ()_{10}$$

Solution:

$$\begin{aligned}(123.4)_8 &= 1 \times 8^2 + 2 \times 8^1 + 3 \times 8^0 + 4 \times 8^{-1} \\ &= (83.5)_{10}\end{aligned}$$

Problem 6.15

$$(B44B)_{16} \rightarrow ()_{10}$$

Solution:

$$\begin{aligned}(B44B)_{16} &= 11 \times 16^3 + 4 \times 16^2 + 4 \times 16^1 + 11 \times 16^0 \\ &= (46155)_{10}\end{aligned}$$

Hexadecimal and Binary Number System**1. Hexadecimal to binary****Problem 6.16**

$$(2BF.29B)_{16} \rightarrow ()_2$$

Solution:

The conversion from hexadecimal to binary number is achieved by replacing each hexadecimal digit with its 4-bit binary equivalent.

$$\begin{array}{ccccccc} 2 & B & F & 2 & 9 & B \\ \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ 0010 & 1011 & 1111 & 0010 & 1001 & 1011 \\ = (00101011\ 1111.0010100011011)_2 \\ = (1010\ 111111.0010100.11011)_2 \end{array}$$

Problem 6.17

$$(1CD.2A)_{16} \rightarrow ()_2$$

Solution:

The conversion from binary to hexadecimal is accomplished by grouping the binary number into groups of 4-bits each, starting from the binary point and proceeding to the right as well as to the left. Each group is then replaced by its hexadecimal equivalent.

$$\begin{array}{ccccc} 1 & C & D & 2 & A \\ \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ 0001 & 1100 & 1101 & 0010 & 1010 \\ = (000111001101.00101010)_2 \\ = (111001101.0010101)_2 \end{array}$$

2. Binary to hexadecimal

Problem 6.18

$$(110\ 110111.\ 1011110)_2 \rightarrow ()_{16}$$

Solution:

$$\begin{array}{ccccc} 0001 & 1011 & 0111 & 1011 & 1100 \\ \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ 1 & B & 7 & B & C \\ \end{array}$$
$$= (1B7.BC)_{16}$$

Octal and Binary Number System

1. Octal to binary

Problem 6.19

$$(21)_8 \rightarrow ()_2$$

Solution:

$$\begin{array}{cc} 2 & 1 \\ \downarrow & \downarrow \\ 010 & 001 \\ \end{array}$$
$$= (0100001)_2 = (10001)_2$$

Problem 6.20

$$(1745.\ 246)_8 \rightarrow ()_2$$

Solution:

$$\begin{array}{ccccccc} 1 & 7 & 4 & 5. & 2 & 4 & 6 \\ \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow & \downarrow \\ 001 & 111 & 100 & 101 & 010 & 100 & 110 \\ \end{array}$$
$$= (00111100101.010100110)_2$$
$$= (111100101.01010011)_2$$

2. Binary to octal

Problem 6.21

$$(10110001101011.\ 111100\ 00011)_2 \rightarrow ()_8$$

Solution:

$$\begin{array}{ccccccccc}
 010 & 110 & 001 & 101 & 011 & 1111 & 100 & 000 & 110 \\
 \downarrow & \downarrow \\
 2 & 6 & 1 & 5 & 3 & 7 & 4 & 0 & 6 \\
 \end{array}
 \stackrel{\text{Ans}}{=} (26153.7406)_8$$

Octal and Hexadecimal Number System

1. Octal to hexadecimal

Problem 6.22 $(1745.246)_8 \rightarrow ()_{16}$

Ans: $(3E5.530)_{16}$

Hint: First change to binary system & then to hexadecimal system

2. Hexadecimal to octal

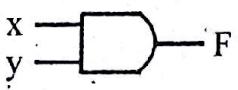
Problem 6.23 $(3E5.530)_{16} \rightarrow ()_8$

Ans: $(1745.246)_8$

Hint: First change to binary system and then to octal system

LOGIC GATES

The logic gates are the basic elements which form the building blocks for complex digital systems. A logic gate is a digital circuit with one or more inputs but with one output.

Name	Graphic Symbol	Algebraic function OR, Boolean function	Truth Table															
AND	 $F = xy$		<table border="1"> <thead> <tr> <th>x</th><th>y</th><th>F</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td></tr> <tr> <td>0</td><td>1</td><td>0</td></tr> <tr> <td>1</td><td>0</td><td>0</td></tr> <tr> <td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	x	y	F	0	0	0	0	1	0	1	0	0	1	1	1
x	y	F																
0	0	0																
0	1	0																
1	0	0																
1	1	1																

OR		$F = x + y$	<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	x	y	F	0	0	0	0	1	1	1	0	1	1	1	1
x	y	F																
0	0	0																
0	1	1																
1	0	1																
1	1	1																
Inverter or NOT		$F = x'$	<table border="1"> <thead> <tr> <th>x</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> </tr> </tbody> </table>	x	F	0	1	1	0									
x	F																	
0	1																	
1	0																	
Buffer		$F = x$	<table border="1"> <thead> <tr> <th>x</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> </tr> </tbody> </table>	x	F	0	0	1	1									
x	F																	
0	0																	
1	1																	
NAND		$F = (xy)'$	<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	x	y	F	0	0	1	0	1	1	1	0	1	1	1	0
x	y	F																
0	0	1																
0	1	1																
1	0	1																
1	1	0																
NOR		$F = (x+y)'$	<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	x	y	F	0	0	1	0	1	0	1	0	0	1	1	0
x	y	F																
0	0	1																
0	1	0																
1	0	0																
1	1	0																
Exclusive-OR (X-OR)		$F = xy' + x'y$ $= x \oplus y$	<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	x	y	F	0	0	0	0	1	1	1	0	1	1	1	0
x	y	F																
0	0	0																
0	1	1																
1	0	1																
1	1	0																
Exclusive NOR (X-NOR)		$F = xy + x'y'$ $= \overline{(x \oplus y)}$ $= x \odot y$	<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	x	y	F	0	0	1	0	1	0	1	0	0	1	1	1
x	y	F																
0	0	1																
0	1	0																
1	0	0																
1	1	1																

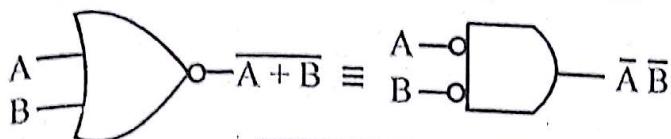
Table 6.2 Illustration of different logic gates

DE MORGAN'S FIRST LAW

It says that the complement of two or more variables ORed is equivalent to the AND of the complements of individual variables.

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

Diagrammatically, it can be expressed as



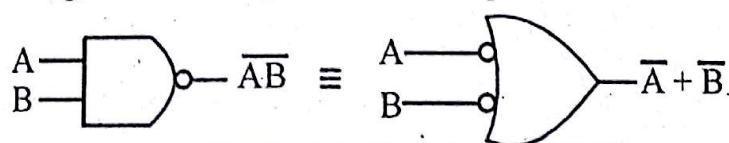
Inputs		Outputs	
A	B	$\overline{A+B}$	$\overline{\overline{A} \cdot \overline{B}}$
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

DE MORGAN'S SECOND LAW

It says that the complement of two or more variables ANDed is equivalent to the OR of the complements of individual variables.

$$\overline{AB} = \overline{A} + \overline{B}$$

Diagrammatically, it can be expressed as



Inputs		Outputs	
A	B	\overline{AB}	$\overline{\overline{A} + \overline{B}}$
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

UNIVERSAL GATES

1. NOR
2. NAND

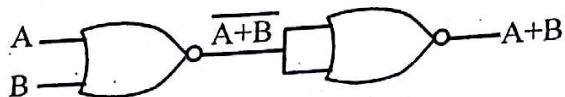
NOR gate

NOR gate is a universal gate because the basic logic gates (NOT, OR, AND) can be realized from NOR gates.

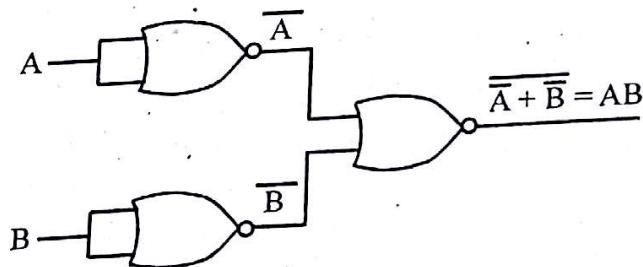
i. NOT from NOR



ii. OR from NOR



iii. AND from NOR



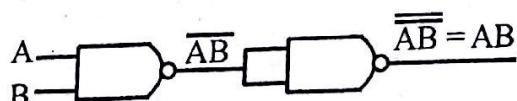
NAND gate

NAND gate is a universal gate because the basic logic gates (NOT, OR, AND) can be realized from NAND gates.

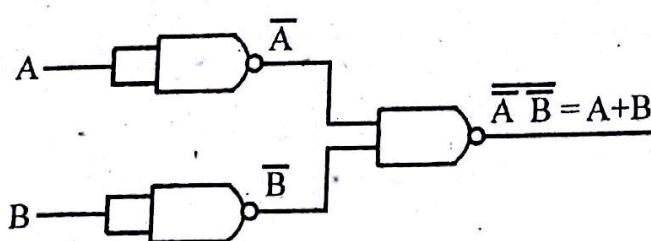
i. NOT from NAND



ii. AND from NAND



iii. OR from NAND



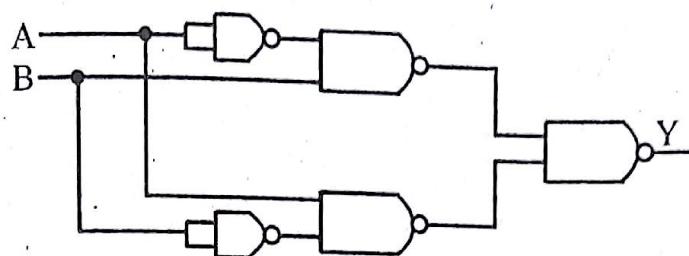
problem 6.24

Draw the circuit of X-OR gate using NAND gates only.

[2070 Bhadra]

Solution:

$$\begin{aligned} Y &= A'B + AB' \\ &= (A'B + AB')'' \\ &= [(A'B)' \cdot (AB')']' \end{aligned}$$

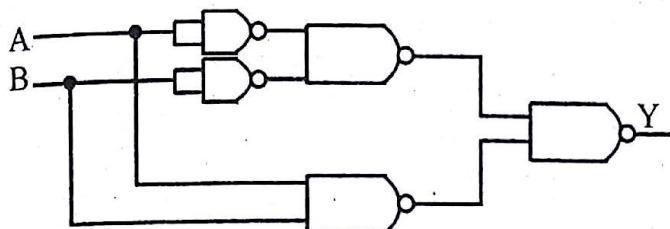


problem 6.25

Draw the circuit of X-NOR gate using NAND gates only.

Solution:

$$\begin{aligned} Y &= A'B' + AB \\ &= (A'B' + AB)'' \\ &= [(A'B')' \cdot (AB)']' \end{aligned}$$



BOOLEAN ALGEBRA

It is an algebra that deals with binary variables and logic operations. A Boolean function described, by an algebraic expression consists of binary variables, the constants 0 and 1, and the logic operation symbols.

COMBINATIONAL CIRCUIT

A combinational circuit consists of logic gates whose outputs at any time are determined from only the present combination of inputs.

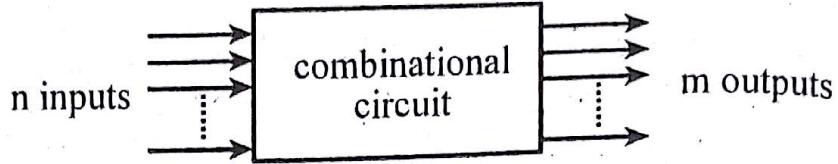


Figure 6.1 Block diagram of a combinational circuit

1. Adder

i. Half Adder

A combinational circuit that performs the addition of two bits is called a half adder.

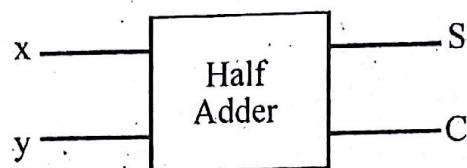


Figure 6.2 Block diagram

x	y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 6.3 Truth table

$$S = x'y + xy' = x \oplus y$$

$$C = xy$$

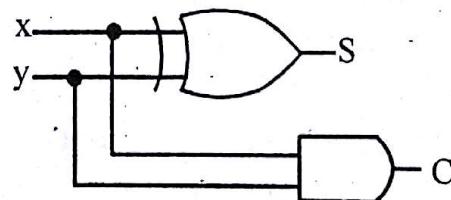


Figure 6.3 Circuit diagram

ii. Full Adder

A combinational circuit that performs the addition of three bits (two significant bits and a previous carry) is called a full adder. The name of the circuit stems from the fact that two half adders can be employed to implement a full adder.

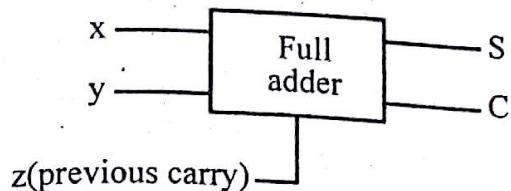


Figure 6.4 Block diagram

x	y	z	s	c
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 6.4 Truth table

$$S = x'y'z + x'yz' + xy'z' + xyz$$

$$= (x \oplus y) \oplus z$$

$$C = (x \oplus y)z + xy$$

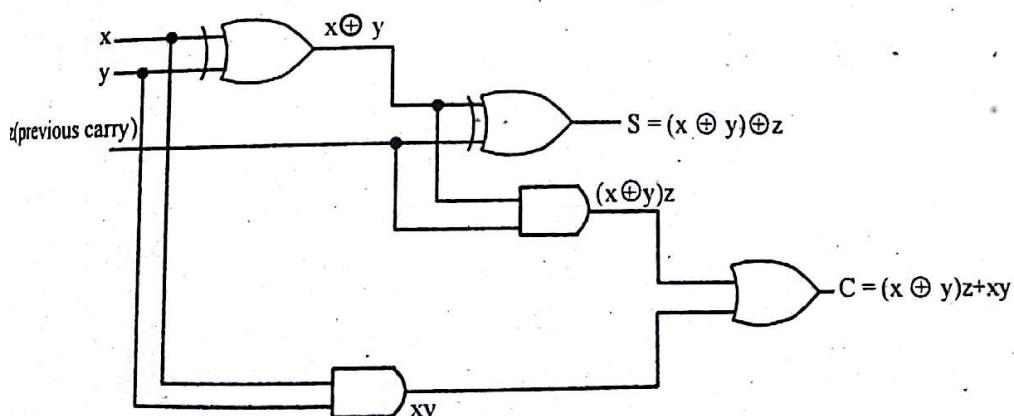


Figure 6.5 Circuit diagram

iii. Binary Adder/Parallel Binary Adder

A binary adder is a combinational circuit that produces the arithmetic sum of two binary numbers. It can be constructed

with full adders connected in cascade, with the output carry from each full adder connected to the input carry of the next full adder in chain.

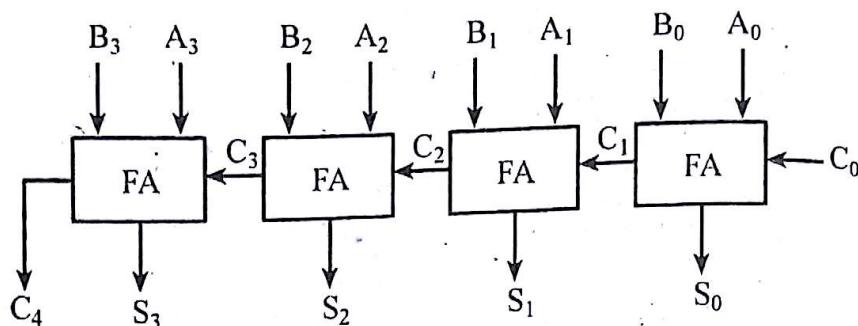


Figure 6.6 Binary adder (4 bit)

2. Subtractor

i. Half subtractor

A half subtractor is a combinational circuit that subtracts two bits and produce their difference. It also has an output to specify if a 1 has been borrowed.

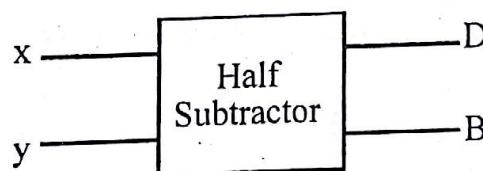


Figure 6.7 Block diagram

x	y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Table 6.5 Truth table

$$D = x'y + xy' = x \oplus y$$

$$B = x'y$$

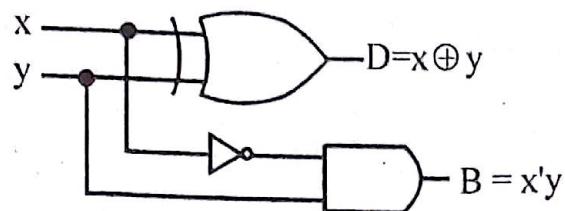


Figure 6.8 Circuit diagram

ii. Full subtractor

A full subtractor is a combinational circuit that performs a subtraction between two bits, taking into account that a 1 may have been borrowed by a lower significant stage. This circuit has three inputs and two outputs. The three inputs, x, y and z denote the minuend, subtrahend, and previous borrow respectively. The two outputs, D and B represent the difference and output borrow respectively.

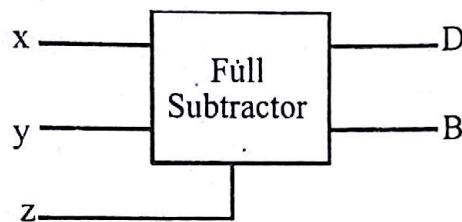


Figure 6.9 Block diagram

x	y	z	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Table 6.6 Truth table

$$D = x'y'z + x'yz' + xy'z' + xyz$$

$$B = x'y + x'z + yz$$

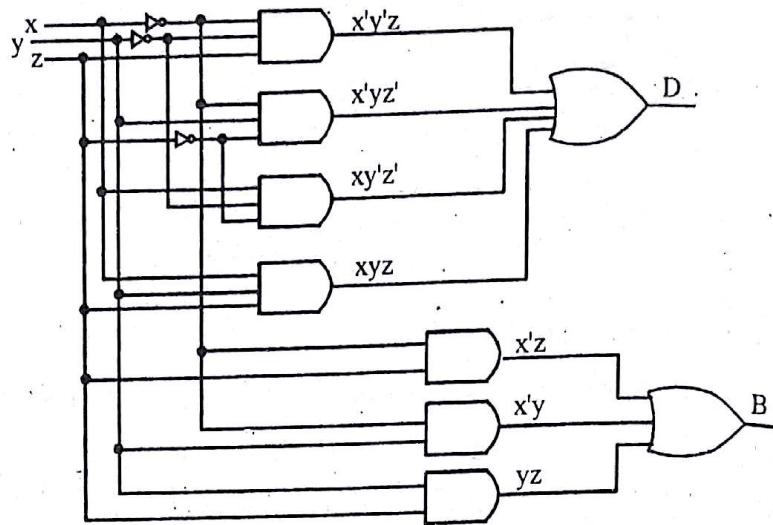


Figure 6.10 Circuit diagram

3. Binary Adder-Subtractor

A binary adder-subtractor is a combinational circuit that performs the arithmetic operations of addition and subtraction with binary numbers.

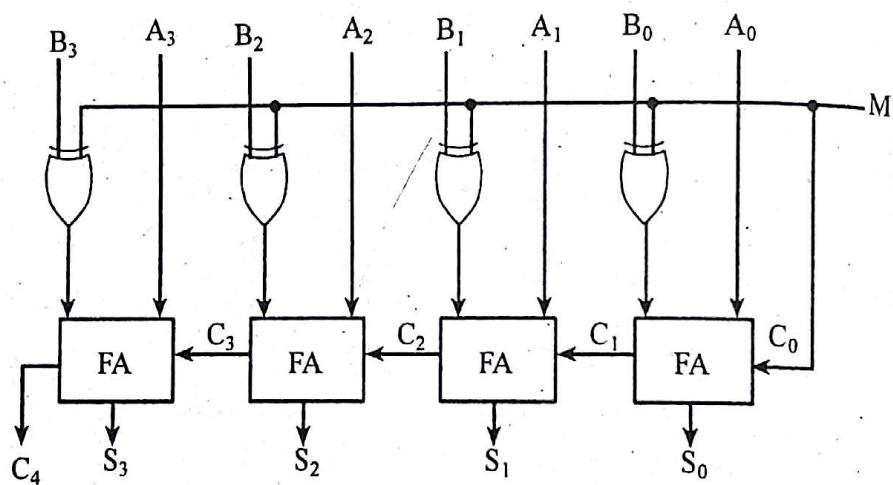


Figure 6.11 Binary adder-subtractor (4 bit)

When $M = 0$, we have $B \oplus 0 = B$ and hence, circuit acts as an adder.

When $M = 1$, we have $\underline{B \oplus 1} = B$ and $C_0 = 1$.

$$(A + \underline{B + 1})$$

2's complement

Hence, circuit acts as a subtractor.

4. Decoders

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. If the n -bit coded information has unused combinations, the decoder may have fewer than 2^n outputs.

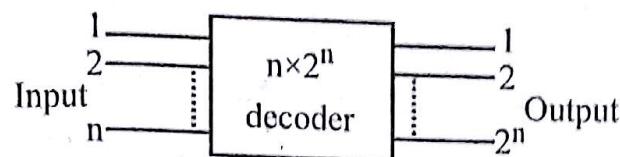


Figure 6.12 Block diagram of a decoder

3x8 Decoder

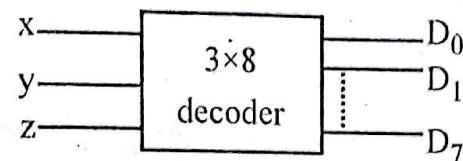


Figure 6.13 Block diagram of a 3×8 decoder

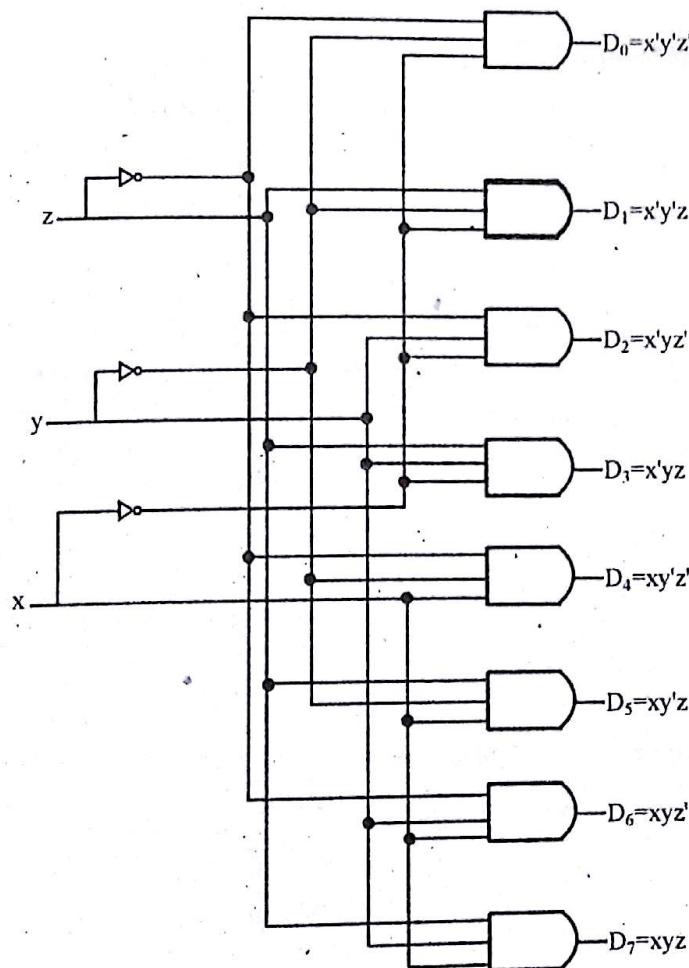


Figure 6.14 Three-to-eight line decoder

Inputs						Outputs				
x	y	z	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	0	1	0
1	1	0	0	0	0	0	0	0	0	1
1	1	1	0	0	0	0	0	0	0	1

Table 6.7 Truth table of a three-to-eight-line decoder

5. Encoder

An encoder is a combinational circuit that performs the inverse operation of a decoder. An encoder has 2^n (or fewer) input lines and n output lines. The output lines, as an aggregate, generate the binary code corresponding to the input value.

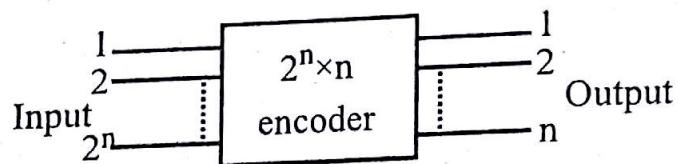


Figure 6.15 Block diagram of an encoder

Octal to binary (8×3) encoder

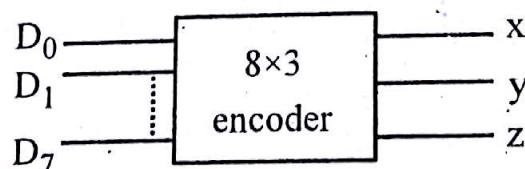


Figure 6.16 Block diagram of a 8×3 encoder

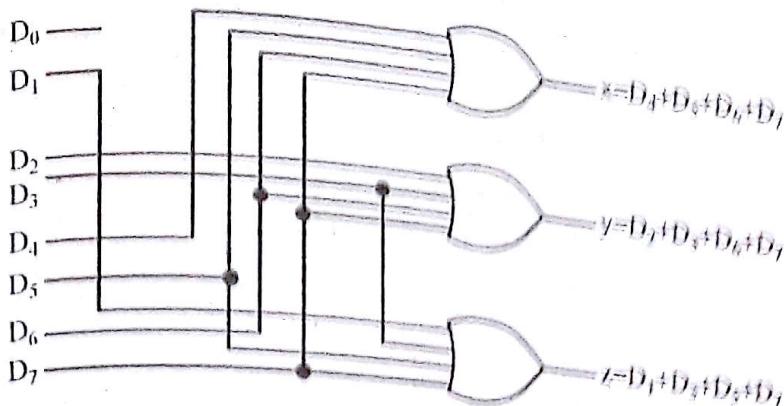


Figure 6.17 Octal-to-binary encoder

Inputs								Outputs		
D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	z	y	t
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	0	0	0	1	0	0	1	0
0	0	0	0	0	0	1	0	0	1	0
0	0	0	0	0	0	0	1	0	1	0
0	0	0	0	0	0	0	1	1	1	1

Table 6.8 Truth table of an octal-to-binary encoder

6. Multiplexers

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Thus, a multiplexer is also called a data selector. Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected.

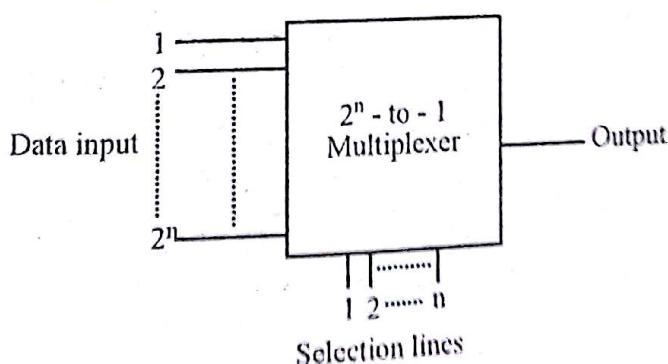


Figure 6.18 Block diagram of a multiplexer

2×1 Multiplexer

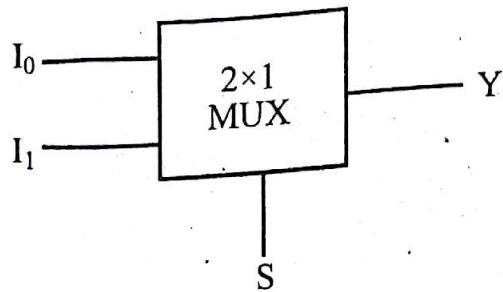


Figure 6.19 Block diagram of a two-to-one line multiplexer

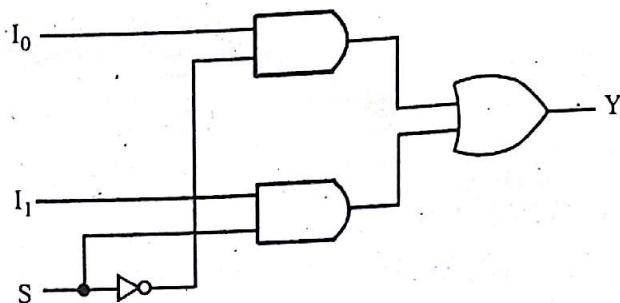


Figure 6.20 Logic diagram of a two-to-one line multiplexer

I_0	I_1	S	Y
1	0	0	1
0	1	1	1

Table 6.9 Truth table of a 2×1 multiplexer

Explanation:

When $S = 0$, $Y = I_0$

When $S = 1$, $Y = I_1$

4×1 Multiplexer

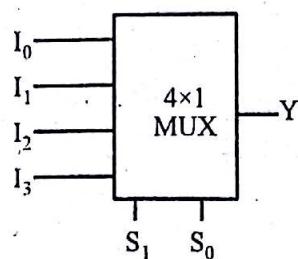


Figure 6.21 Block diagram of a four-to-one line multiplexer

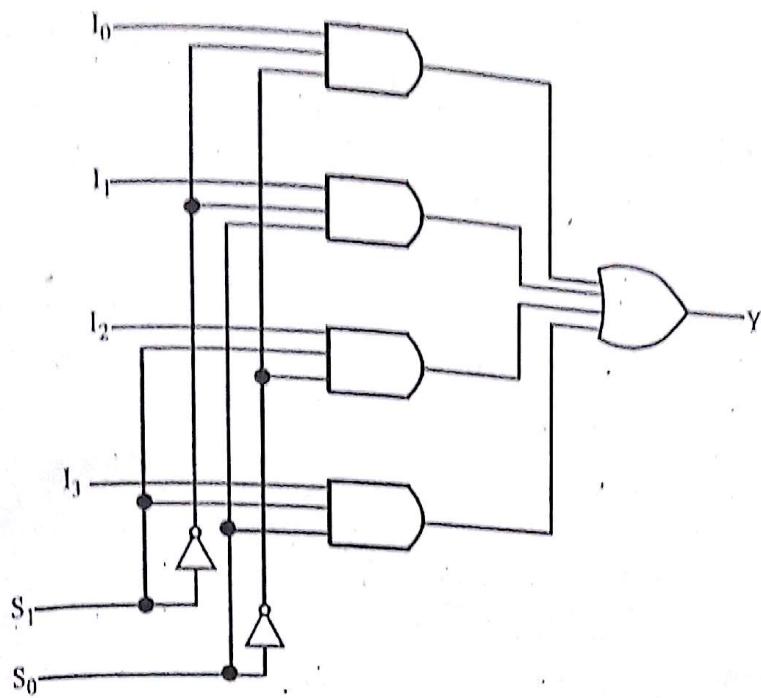


Figure 6.22 Logic diagram of a four-to-one line multiplexer

I ₀	I ₁	I ₂	I ₃	S ₁	S ₀	Y
1	0	0	0	0	0	1
0	1	0	0	0	1	1
0	0	1	0	1	0	1
0	0	0	1	1	1	1

Table 6.10 Truth table of a 4X1 multiplexer

Explanation:

When S₁ S₀ = 00, Y = I₀

When S₁ S₀ = 01, Y = I₁

When S₁ S₀ = 10, Y = I₂

When S₁ S₀ = 11, Y = I₃

7. Demultiplexers

"Demultiplex" means "one into many". A demultiplexer is a combinational circuit that receives information from a single line and directs it to one of 2^n possible output lines. The selection of a specific output is controlled by the bit combination of n selection lines.

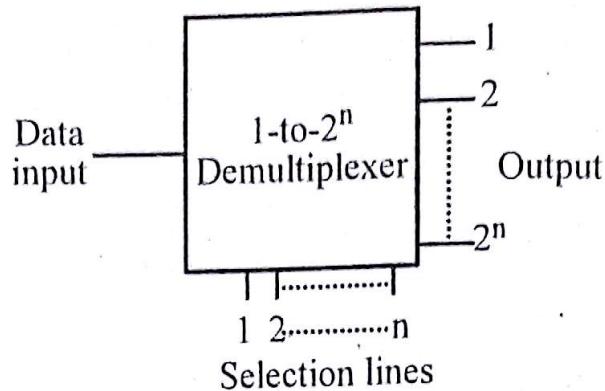


Figure 6.23 Block diagram of a demultiplexer

1×2 Demultiplexer

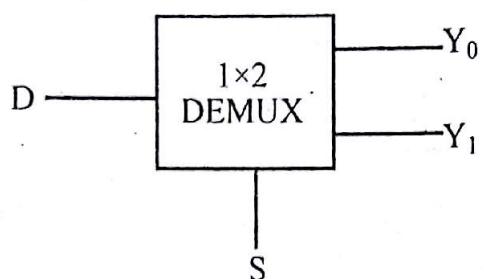


Figure 6.24 Block diagram of a 1×2 demultiplexer

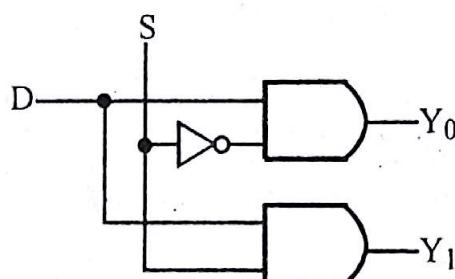


Figure 6.25 Logic diagram of 1-to-2 demultiplexer

D	S	Y ₀	Y ₁
1	0	1	0
1	1	0	1

Table 6.11 Truth table of a 1×2 demultiplexer

Explanation:

When S = 0, Y₀ = D

When S = 1, Y₁ = D

1x4 Demultiplexer

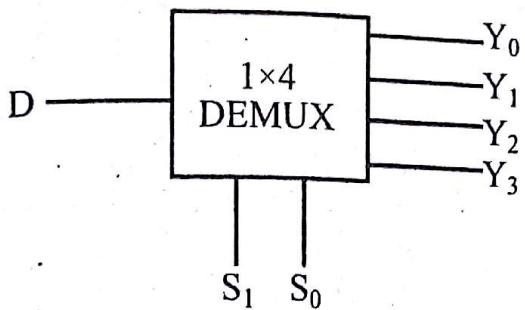


Figure 6.26 Block diagram of a 1x4 demultiplexer

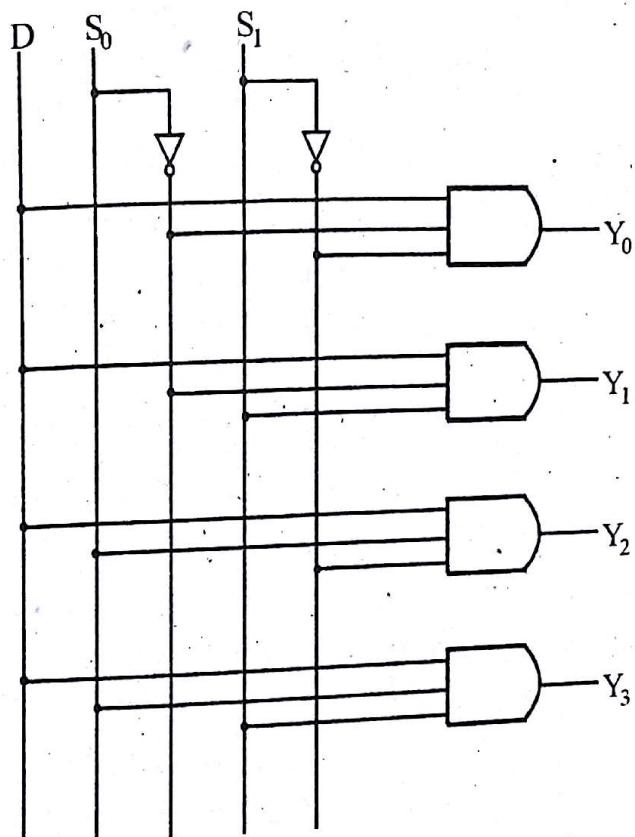


Figure 6.27 Logic diagram of 1-to-4 demultiplexer

D	S ₁	S ₀	Y ₀	Y ₁	Y ₂	Y ₃
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

Table 6.12 Truth table of a 1x4 demultiplexer

Explanation:

When $S_1 S_0 = 00$, $Y_0 = D$

When $S_1 S_0 = 01$, $Y_1 = D$

When $S_1 S_0 = 10$, $Y_2 = D$

When $S_1 S_0 = 11$, $Y_3 = D$

BINARY ARITHMETIC

Binary Addition

The four basic rules for adding binary digits are as follows;

$0 + 0 = 0$ Sum of 0 with a carry of 0

$0 + 1 = 1$ Sum of 1 with a carry of 0

$1 + 0 = 1$ Sum of 1 with a carry of 0

$1 + 1 = 10$ Sum of 0 with a carry of 1

Problem 6.26

Add $(110011)_2$ to $(101101)_2$

Solution:

1st column: $1 + 1 = 0$ with carry 1

2nd column: $1 + 0 = 1$ combined with carry 1
= 0 with carry 1

3rd column: $0 + 1 = 1$ combined with carry 1
= 0 with carry 1

4th column: $0 + 1 = 1$ combined with carry 1
= 0 with carry 1

5th column: $1 + 0 = 1$ combined with carry 1
= 0 with carry 1

6th column: $1 + 1 = 10$ combined with carry 1 = 11

$$\begin{array}{r} 110011 \\ +101101 \\ \hline 1100000 \\ = (1100000)_2 \end{array}$$

Binary subtraction

The four basic rules for subtracting bits are as follows:

$$0 - 0 = 0$$

$$1 - 1 = 0$$

$$1 - 0 = 1$$

$$10 - 1 = 1 \quad 0 - 1 \text{ with a borrow of } 1$$

Problem 6.27

Subtract $(0111)_2$ from $(1001)_2$

Solution:

$$1^{\text{st}} \text{ column: } 1 - 1 = 0$$

$$2^{\text{nd}} \text{ column: } 0 - 1 = 1 \text{ with a borrow of } 1$$

$$3^{\text{rd}} \text{ column: } 1 \text{ (after borrow)} - 1 = 0$$

$$4^{\text{th}} \text{ column: } 0 \text{ (after borrow)} - 0 = 0$$

$$\begin{array}{r} 1001 \\ +0111 \\ \hline 0010 \\ = (0010)_2 \end{array}$$

Binary Multiplication

The four basic rules for multiplying bits are as follows:

$$0 \times 0 = 0$$

$$0 \times 1 = 0$$

$$1 \times 0 = 0$$

$$1 \times 1 = 1$$

Problem 6.28

Multiply $(1011)_2$ by $(101)_2$

Solution:

$$\begin{array}{r} 1011 \\ \times 101 \\ \hline 1011 \\ 0000\times \\ 1011\times\times \\ \hline 110111 \quad = (110111)_2 \end{array}$$

Problem 6.29**Multiply $(11010)_2$ by $(11011)_2$** **Solution:**

$$\begin{array}{r}
 11010 \\
 \times 11011 \\
 \hline
 11010 \\
 11010\times \\
 00000\times\times \\
 11010\times\times\times \\
 \hline
 11010\times\times\times \\
 \hline
 1010111110 = (1010111110)_2
 \end{array}$$

Binary Division

Division in binary follows the same procedure as division in decimal.

$$0 \div 1 = 0$$

$$1 \div 1 = 1$$

Problem 6.30**Divide $(110110)_2$ by $(101)_2$** **Solution:**

$$\begin{array}{r}
 1010 \\
 101) \overline{110110} \\
 101 \\
 \hline
 0011 \\
 000 \\
 \hline
 111 \\
 101 \\
 \hline
 100 \text{ Remainder}
 \end{array}$$

Problem 6.31**Divide $(110)_2$ by $(10)_2$** **Solution:**

$$\begin{array}{r}
 11 \\
 10) \overline{110} \\
 10 \\
 \hline
 10 \\
 10 \\
 \hline
 00 = (11)_2
 \end{array}$$

COMPLEMENTS

Complements are used in digital computers to simplify the subtraction operation and for logical manipulation. Simplifying operations leads to simpler, less expensive circuits to implement the operations. For base- r system, there are two types of complement.

- i. The radix complement (r 's complement)
- ii. The diminished radix complement (($r-1$)'s complement)

i. Diminished Radix Complement

The $(r - 1)$'s complement of a number N in base r having n digits is defined as $(r^n - 1) - N$.

For $r = 10$, $(r - 1) = 9$

$$\begin{aligned}\text{The 9's complement of } 546700 &= 999999 - 546700 \\ &= 453299\end{aligned}$$

$$\begin{aligned}\text{The 9's complement of } 012398 &= 999999 - 012398 \\ &= 987601\end{aligned}$$

For $r = 2$, $(r - 1) = 1$

The 1's complement of 1011000 = 0100111

The 1's complement of 0101101 = 1010010

ii. Radix Complement

The r 's complement of an n -digit number N in base r is defined as $r^n - N$ for $N \neq 0$ and as 0 for $N = 0$.

For $r = 10$, the 10's complement of 012398 = 987602

The 10's complement of 246700 = 753300

For $r = 2$, the 2's complement of 1101100 = 0010100

The 2's complement of 0110111 = 1001001

Problem 6.32

Using 10's complement, subtract: 52532–3250

Solution:

Let $M = 52532$, $N = 3250$

10's complement of $N (= 03250)$ is 96750

$$\begin{array}{r}
 & 5 & 2 & 5 & 3 & 2 \\
 + & 9 & 6 & 7 & 5 & 0 \\
 \hline
 \text{sum} = & 1 & 4 & 9 & 2 & 8 & 2
 \end{array}$$

Discarding end carry,

Answer = 49282

Problem 6.33

Using 10's complement, subtract: 3250 - 72532

Solution:

Let M = 03250, N = 72532

10's complement of N (= 72532) is 27468

$$\begin{array}{r}
 & 0 & 3 & 2 & 5 & 0 \\
 + & 2 & 7 & 4 & 6 & 8 \\
 \hline
 & 3 & 0 & 7 & 1 & 8
 \end{array}$$

There is no end carry. Therefore, the answer is -(10's complement of 30718) = -69282

Problem 6.34

Using 2's complement, subtract $(1000011)_2$ from $(1010100)_2$

Solution:

Let X = 1010100, Y = 1000011

2's complement of Y (= 1000011) is 0111101

$$\begin{array}{r}
 & 1 & 0 & 1 & 0 & 1 & 0 & 0 \\
 + & 0 & 1 & 1 & 1 & 1 & 0 & 1 \\
 \hline
 & 1 & 0 & 0 & 1 & 0 & 0 & 1
 \end{array}$$

There is end carry, so we discard it. The answer is $(0010001)_2$

Problem 6.35

Using 2's complement perform $(1000011)_2 - (1010100)_2$

Solution:

Let X = 1000011, Y = 1010100

2's complement of Y (= 1010100) is 0101100

$$\begin{array}{r}
 1 \ 0 \ 0 \ 0 \ 0 \ 1 \ 1 \\
 + \ 0 \ 1 \ 0 \ 1 \ 1 \ 0 \ 0 \\
 \hline
 1 \ 1 \ 0 \ 1 \ 1 \ 1 \ 1
 \end{array}$$

There is no end carry. Therefore, the answer is -(2's complement of 1101111) = -(0010001)₂

Problem 6.36

Using 1's complement, perform $(1010100)_2 - (1000011)_2$

Solution:

Let X = 1010100, Y = 1000011

1's complement of Y (= 1000011) = 0111100

$$\begin{array}{r}
 1 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0 \\
 + \ 0 \ 1 \ 1 \ 1 \ 1 \ 0 \ 0 \\
 \hline
 1 \ 0 \ 0 \ 1 \ 0 \ 0 \ 0
 \end{array}$$

There is end carry, so discard it and add 1.

$$\begin{array}{r}
 0 \ 0 \ 1 \ 0 \ 0 \ 0 \ 0 \\
 + \ 1 \\
 \hline
 0 \ 0 \ 1 \ 0 \ 0 \ 0 \ 1
 \end{array}$$

∴ (0010001)₂ Ans.

Problem 6.37

Perform $(1000011)_2 - (1010100)_2$ using 1's complement.

Solution:

Let X = 1000011, Y = 1010100

1's complement of Y (= 1010100) is 0101011

$$\begin{array}{r}
 1 \ 0 \ 0 \ 0 \ 0 \ 1 \ 1 \\
 + \ 0 \ 1 \ 0 \ 1 \ 0 \ 1 \ 1 \\
 \hline
 1 \ 1 \ 0 \ 1 \ 1 \ 1 \ 0
 \end{array}$$

There is no end carry. Therefore, the answer is - (1's complement of 1101110) = -(0010001)₂

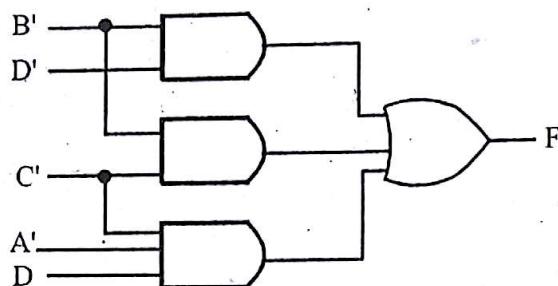
Problem 6.38

Draw the circuit for the following functions, OR,
Implement the given function with gates.

- $F = B'D' + B'C' + A'C'D$
- $F = (A' + B')(C' + D')(B' + D)$

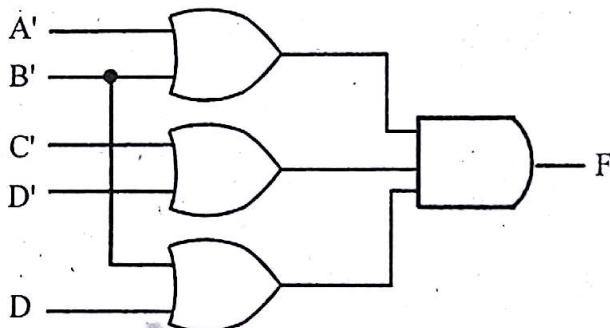
Solution:

a.



$$F = B'D' + B'C' + A'C'D$$

b.



$$F = (A' + B')(C' + D')(B' + D)$$

CANONICAL AND STANDARD FORMS

Minterms and Maxterms

Consider two binary variables x and y combined with an AND operation. Since each variable may appear in either (normal or in its complement) form, there are four possible combinations: $x'y'$, $x'y$, xy' , and xy . Each of these four AND terms is called a minterm, or a standard product. Thus, the n variables can be combined to form 2^n minterms.

In a similar fashion, n variables forming an OR term, with each variable being primed or unprimed, provide 2^n possible combinations, called maxterms, or standard sums.

Minterms				Maxterms		
x	y	z	Term	Designation	Term	Designation
0	0	0	$x'y'z'$	m_0	$x+y+z$	M_0
0	0	1	$x'y'z$	m_1	$x+y+z'$	M_1
0	1	0	$x'yz'$	m_2	$x+y'+z$	M_2
0	1	1	$x'yz$	m_3	$x+y'+z'$	M_3
1	0	0	$xy'z'$	m_4	$x'+y+z$	M_4
1	0	1	$xy'z$	m_5	$x'+y+z'$	M_5
1	1	0	xyz'	m_6	$x'+y'+z$	M_6
1	1	1	xyz	m_7	$x'+y'+z'$	M_7

Table 6.13 Minterms and maxterms for three variables

Canonical form

Boolean functions expressed as a sum of minterms or a product of maxterms are said to be in canonical form.

Standard form

The two canonical forms of Boolean algebra are basic forms that one obtains from reading a given function from the truth table. These forms are very seldom the ones with the least number of literals, because each minterm or maxterm must contain, by definition, all the variables, either complemented or uncomplemented. Another way to express Boolean functions is in standard form. In this configuration, the terms that form the function may contain one, two, or any number of literals. There are two types of standard forms: the sum of products and product of sums.

Problem 6.39

Express the Boolean function $F = A + B'C$ as a sum of minterms.

Solution:

$$\begin{aligned}
 F &= A + B'C \\
 &= A(B+B')(C+C') + (A+A')B'C \quad : x+x'=1
 \end{aligned}$$

$$\begin{aligned}
&= (AB + AB')(C + C') + AB'C + A'B'C \\
&= ABC + ABC' + AB'C + AB'C' + AB'C + A'B'C \\
&= ABC + ABC' + AB'C + AB'C' + A'B'C \\
&= A'B'C + AB'C' + AB'C + ABC' + ABC \\
&= m_1 + m_4 + m_5 + m_6 + m_7 \\
\therefore F(A,B,C) &= \Sigma(1,4,5,6,7)
\end{aligned}$$

Problem 6.40

Express the Boolean function $F = xy + x'z$ as a product of maxterms.

Solution:

First, convert the function into OR terms by using the distributive law [$A+BC = (A+B)(A+C)$]

$$\begin{aligned}
F &= xy + x'z = (xy+x')(xy+z) \\
&= (x+x')(y+x')(x+z)(y+z) \\
&= (x'+y)(x+z)(y+z) \quad (\because x+x' = 1)
\end{aligned}$$

Each OR term is missing one variable, therefore

$$\begin{aligned}
F &= (x' + y + zz')(x+z+yy')(y+z+xx') \quad (\because AA' = 0) \\
&= (x'+y+z)(x'+y+z')(x+z+y)(x+z+y')(y+z+x)(y+z+x') \\
&= (x'+y+z)(x'+y+z')(x+y+z)(x+y'+z) \\
&= (x+y+z)(x+y'+z)(x'+y+z)(x'+y+z') \\
&= M_0 M_2 M_4 M_5
\end{aligned}$$

$\therefore F(x,y,z) = \pi(0,2,4,5)$; π denotes the ANDing of maxterms

KARNAUGH MAP OR K - MAP

The map method that provides a simple, straightforward procedure for minimizing Boolean functions is known as the Karnaugh map or K - map. This method may be regarded as a pictorial form of a truth table.

Simplifying Boolean expressions with the help of K-map can be understood with the help of examples that follows.

problem 6.41

Simplify the Boolean function $F(x, y, z) = \Sigma(2,3,4,5)$

Solution:

x	y	z	00	01	11	10
0					1	1
1			1	1		

$$\therefore F(x, y, z) = x'y + xy'$$

Problem 6.42

Simplify the Boolean function $F(x, y, z) = \Sigma(3,4,6,7)$

Solution:

x	y	z	00	01	11	10
0					1	
1	1	1			1	1

$$\therefore F(x, y, z) = yz + xz'$$

Problem 6.43

Simplify the Boolean function $F(x, y, z) = \Sigma(0,2,4,5,6)$

Solution:

x	y	z	00	01	11	10
0	1					1
1	1	1				1

$$\therefore F(x, y, z) = z' + xy'$$

Problem 6.44

Simplify the Boolean expression $S(x, y, z) = \Sigma(1,2,4,7)$

Solution:

x	y	z	00	01	11	10
0				1		1
1	1	1	1		1	

Since, there is no adjacency existing among the elements,
grouping $S(x,y,z) = x'y'z + x'yz' + xy'z' + xyz$

Problem 6.45

Let the Boolean function $F = A'C + A'B + AB'C + BC$.

- Express this function as a sum of min terms.
- Find the minimal sum - of - products expression.

Solution:

- $$\begin{aligned}
F &= A'C + A'B + AB'C + BC \\
&= A'C(B+B') + A'B(C+C') + AB'C + BC(A+A') \\
&= A'BC + A'B'C + A'BC + A'BC' + AB'C + ABC + A'BC \\
&= A'BC + A'B'C + A'BC' + AB'C + ABC \\
&= A'B'C + A'BC' + A'BC + AB'C + ABC \\
&= m_1 + m_2 + m_3 + m_5 + m_7
\end{aligned}$$

$$\therefore F(A,B,C) = \Sigma(1,2,3,5,7)$$

b.

		BC	
	A	00 01 11 10	
0		1 1 1 1	
1		1 1	

\therefore The minimal sum-of products expression is

$$F(A, B, C) = C + A'B$$

Problem 6.46

Simplify the Boolean function $F(w,x,y,z) = \Sigma(0,1,2,4,5,6,8,9,12,13,14)$

Solution:

		yz	
	wx	00 01 11 10	
00		1 1	1
01		1 1	
11		1 1	1
10		1 1	

$$\therefore F(w, x, y, z) = y' + w'z' + xz'$$

Problem 6.47*Simplify the Boolean function*

$$F = A'B'C' + B'CD' + A'BCD' + AB'C'$$

Solution:

Expressing the given function as a sum of minterms.

$$F = A'B'C' + B'CD' + A'BCD' + AB'C'$$

$$= A'B'C'(D+D') + B'CD'(A+A') + A'BCD' + AB'C'(D+D')$$

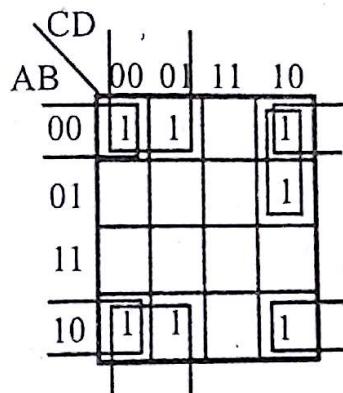
$$= A'B'C'D + A'B'C'D' + AB'CD' + A'B'CD' + A'BCD' + AB'C'D + AB'C'D'$$

$$= A'B'C'D' + A'B'C'D + A'B'CD' + A'BCD' + AB'C'D' + AB'C'D + AB'CD'$$

0000 0001 0010 0110 1000 1001 1010

$$= m_0 + m_1 + m_2 + m_6 + m_8 + m_9 + m_{10}$$

$$\therefore F(A,B,C,D) = \Sigma(0,1,2,6,8,9,10)$$



$$\therefore F(A,B,C,D) = B'D' + B'C' + A'CD'$$

Problem 6.48*Simplify the expression using K-Map, $F(A,B,C) = A'B + BC' + AC'$ [2068 Magh]***Solution:**

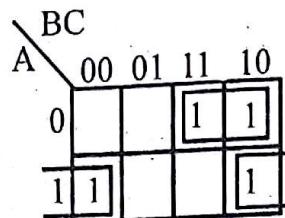
Expressing the given function as a sum of minterms.

$$F = A'B + BC' + AC'$$

$$= A'B(C+C') + BC'(A+A') + AC'(B+B')$$

$$= A'BC + A'BC' + ABC' + A'BC' + ABC' + AB'C'$$

$$\begin{aligned}
 &= A'BC + A'BC' + ABC' + AB'C' \\
 &= A'BC' + A'BC + AB'C' + ABC' \\
 &\quad 010 \quad 011 \quad 100 \quad 110 \\
 &= m_2 + m_3 + m_4 + m_6 \\
 \therefore F(A,B,C) &= \Sigma(2,3,4,6)
 \end{aligned}$$



$$\therefore F(A,B,C) = AC' + A'B$$

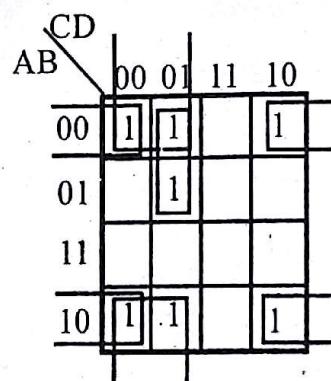
Problem 6.49

Simplify the following Boolean function into (a) sum-of-products form and (b) product-of-sums form.

$$F(A, B, C, D) = \Sigma(0, 1, 2, 5, 8, 9, 10)$$

Solution:

a.



$F(A,B,C,D) = B'C' + B'D' + A'C'D$ which is the required sum - of- products form.

- b. In the map, the squares marked with 0's represent the minterms not included in F and therefore denotes the complement of F .

	CD	00	01	11	10
AB					
00			0		
01	0		0	0	
11	0	0	0	0	
10			0		

$$F' = BD' + AB + CD$$

Applying DeMorgan's theorem, we get

$$F = (B'+D) (A'+B') (C'+D')$$

$\therefore F(A,B,C,D) = (A'+B') (C'+D') (B'+D)$ which is the required product - of - sums form.

Problem 6.50

Simplify $\pi(0, 4, 5, 8, 9, 11, 15)$ using K-map and write its SOP expression.

Solution:

	CD	00	01	11	10
AB					
00	0				
01	0	0			
11			0		
10	0	0	0		

For SOP form,

	CD	00	01	11	10
AB					
00		1	1	1	
01			1	1	
11	1	1		1	
10					1

$$\text{SOP expression is } F(A,B,C,D) = ABC' + A'B'D + A'C + CD'$$

Problem 6.51

Simplify the Boolean function $F(w,x,y,z) = \Sigma(1,3,7,11,15)$
 which has the don't-care conditions $d(w,x,y,z) = \Sigma(0,2,5)$

Solution:

The minterms of F are the variable combinations that make the function equal to 1. The minterms of d are the variable combinations that make the function either 0 or 1.

wx \ yz	00	01	11	10
00	x	1	1	x
01		x	1	
11			1	
10			1	

a. $F = yz + w'x'$

wx \ yz	00	01	11	10
00	x	1	1	x
01		x	1	
11			1	
10			1	

b. $F = yz + w'z$

Note: Either of the expressions is correct.

Problem 6.52

Simplify the Boolean function:

$$F(w, x, y, z) = \Sigma(1,3,10) + \Sigma_d(0,2,8,12)$$

Solution:

wx \ yz	00	01	11	10
00	x	1	1	x
01				
11	x			
10	x			1

$$F(w, x, y, z) = w'x' + x'z'$$

Problem 6.53

Simplify using K-map.

$$F(x, y, z) = xyz + x'y'z + xy'z' + x'y'z' + x'yz \quad [2070 Bhadra]$$

Solution:

$$F(x, y, z) = xyz + x'y'z + xy'z' + x'y'z' + x'yz = \Sigma(0, 1, 3, 4, 7)$$

	00	01	11	10
0	1	1	1	0
1	1	0	1	0

$$\therefore F = y'z' + x'y' + yz$$

Problem 6.54

$$\text{Simplify: } A\bar{B}\bar{C} + A\bar{B}\bar{C}D + A\bar{C}$$

Solution:

$$\begin{aligned}
 A\bar{B}\bar{C} + A\bar{B}\bar{C}D + A\bar{C} &= A\bar{B}\bar{C}(1+D) + A\bar{C} \\
 &= A\bar{B}\bar{C} + A\bar{C} (\because 1+X=1) \\
 &= A\bar{C}(\bar{B} + 1) \\
 &= A\bar{C} (\because \bar{X}+1=1) \\
 &= A\bar{C}
 \end{aligned}$$

Problem 6.55

$$\text{Simplify: } (A+B)(A+\bar{B})(\bar{A}+B)$$

Solution:

$$\begin{aligned}
 (A+B)(A+\bar{B})(\bar{A}+B) &= (A+B)(A\bar{A} + AB + \bar{A}\bar{B} + B\bar{B}) \\
 &= (A+B)(0+AB+\bar{A}\bar{B}+0) (\because X\bar{X}=0) \\
 &= (A+B)(AB+\bar{A}\bar{B}) \\
 &= AAB + A\bar{A}\bar{B} + ABB + \bar{A}B\bar{B} \\
 &= AB + 0 + AB + 0 (\because XX=X) \\
 &= AB (\because XY+XY=XY)
 \end{aligned}$$

Problem 6.56

$$\text{Prove: } \overline{\bar{A}\bar{B} + \bar{A} + AB} = 0$$

$$\text{Solution: L.H.S.} = \overline{\bar{A}\bar{B} + \bar{A} + AB}$$

$$= \overline{\bar{A} + \bar{B} + \bar{A} + AB} (\because \overline{XY} = \bar{X} + \bar{Y})$$

$$\begin{aligned}
 &= \overline{\overline{A} + \overline{B} + AB} \quad (\because \overline{X} + \overline{X} = \overline{X}) \\
 &= \overline{\overline{AB} + AB} \quad (\because \overline{X} + \overline{Y} = \overline{XY}) \\
 &= \overline{1} \quad (\because \overline{X} + X = 1) \\
 &= 0 \text{ proved.}
 \end{aligned}$$

Problem 6.57 Prove: $\overline{AB+BC+CA} = \overline{A}\overline{B} + \overline{B}\overline{C} + \overline{A}\overline{C}$

$$\begin{aligned}
 \text{Solution: L.H.S.} &= \overline{AB+BC+CA} \\
 &= \overline{AB+(BC+CA)} \\
 &= \overline{AB} \overline{(BC+CA)} \quad (\because \overline{X+Y} = \overline{X}\overline{Y}) \\
 &= \overline{AB} \overline{(B+A)C} \\
 &= \overline{AB} \left\{ \overline{C} + \overline{(B+A)} \right\} \quad (\because \overline{XY} = \overline{X} + \overline{Y}) \\
 &= \overline{AB} \left\{ \overline{C} + \overline{B} \overline{A} \right\} \\
 &= (\overline{A} + \overline{B})(\overline{C} + \overline{B} \overline{A}) \\
 &= \overline{A}\overline{C} + \overline{A}\overline{A}\overline{B} + \overline{B}\overline{C} + \overline{A}\overline{B}\overline{B} \\
 &= \overline{A}\overline{C} + \overline{A}\overline{B} + \overline{B}\overline{C} + \overline{A}\overline{B} \quad (\because \overline{XX} = \overline{X}) \\
 &= \overline{A}\overline{C} + \overline{A}\overline{B} + \overline{B}\overline{C} \quad (\because XY + XY = XY)
 \end{aligned}$$

proved.

Problem 6.58

Verify the following

[2069 Bhadra]

i. $AB + \overline{A}C = (A+C)(\overline{A}+B)$

Solution:

$$\begin{aligned}
 \text{R.H.S.} &= (A+C)(\overline{A}+B) \\
 &= A\overline{A} + AB + \overline{A}C + BC
 \end{aligned}$$

$$\begin{aligned}
 &= 0 + AB + \bar{A} C + BC \\
 &= AB + \bar{A} C + BC (A + \bar{A}) (\because A + \bar{A} = 1) \\
 &= AB + \bar{A} C + ABC + \bar{A} BC \\
 &\doteq AB + ABC + \bar{A} C + \bar{A} BC \\
 &= AB(1+C) + \bar{A} C(1+B) \\
 &= AB + \bar{A} C (\because 1+X=1) \\
 &= \text{L.H.S. proved.}
 \end{aligned}$$

ii. $XY + \bar{X} Z + YZ = XY + \bar{X} Z$

Solution:

$$\begin{aligned}
 \text{L.H.S.} &= XY + \bar{X} Z + YZ \\
 &= XY + \bar{X} Z + YZ (X + \bar{X}) (\because X + \bar{X} = 1) \\
 &= XY + \bar{X} Z + XYZ + \bar{X} YZ \\
 &= XY + XYZ + \bar{X} Z + \bar{X} YZ \\
 &= XY(1+Z) + \bar{X} Z(1+Y) \\
 &= XY + \bar{X} Z (\because 1+A = 1) \\
 &= \text{R.H.S. proved.}
 \end{aligned}$$

Problem 6.59

Simplify the expressions

i. $\bar{A} \bar{B} \bar{C} + \bar{A} \bar{B} C + A \bar{B} \bar{C} + A \bar{B} C$

ii. $A \bar{C} + ABC + A(C + A \bar{C})$ [2067 Mangsir]

Solution:

$$\begin{aligned}
 \text{i. } &\bar{A} \bar{B} \bar{C} + \bar{A} \bar{B} C + A \bar{B} \bar{C} + A \bar{B} C \\
 &= \bar{A} \bar{B} (\bar{C} + C) + A \bar{B} (\bar{C} + C) \\
 &= \bar{A} \bar{B} + A \bar{B} [\because X + \bar{X} = 1]
 \end{aligned}$$

$$= \bar{B} (\bar{A} + A)$$

$$= \bar{B}$$

$$\text{ii. } A\bar{C} + ABC + A(C+A\bar{C})$$

$$= A\bar{C} + ABC + AC + AA\bar{C}$$

$$= A\bar{C} + ABC + AC + A\bar{C} \quad [\because XX=X]$$

$$= A\bar{C} + ABC + AC \quad [\because XY+XY=XY]$$

$$= A\bar{C} + AC + ABC$$

$$= A(\bar{C} + C) + ABC$$

$$= A + ABC$$

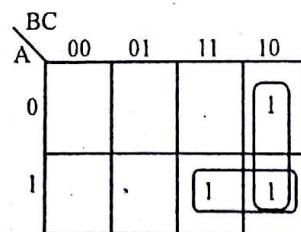
$$= A(1+BC)$$

$$= A \quad [\because 1+X=1]$$

Problem 6.60

Simplify the expression using K-map: $Y = A'BC' + ABC' + ABC$ [2071 Bhadra]

Solution:



$$Y = AB + BC'$$

Problem 6.61

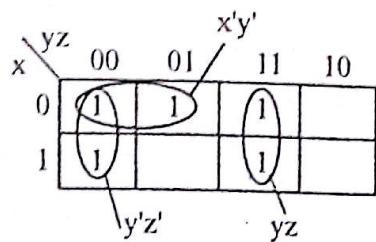
Simplify the following expression:

$$\text{i. } F(x, y, z) = xyz + x'y'z + xy'z' + x'y'z' + x'yz$$

$$\text{ii. } F(x, y, z) = \Sigma(0, 2, 5, 6) \quad [2072 Magh]$$

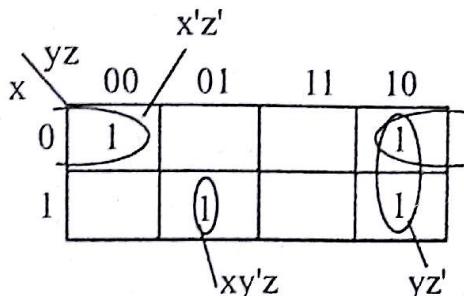
Solution:

$$\begin{aligned} \text{i. } F(x, y, z) &= xyz + x'y'z + xy'z' + x'y'z' + x'yz \\ &= 111 + 001 + 100 + 000 + 011 \\ &= \Sigma(0, 1, 3, 4, 7) \end{aligned}$$



$$F = y'z' + x'y' + yz$$

ii. $F = \Sigma (0, 2, 5, 6)$



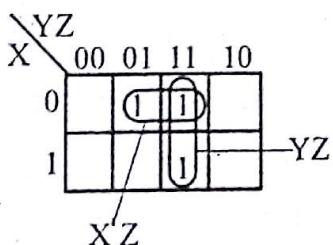
$$F = x'z' + yz' + xy'z$$

Problem 6.62

Simplify the expression using K-map:

$$F(X, Y, Z) = X'YZ + X'Y'Z + XYZ \quad [2073 Bhadra]$$

Solution:



$$F = X'Z + YZ$$

SEQUENTIAL CIRCUITS

The logic circuits whose outputs at any instant of time depend not only on the present inputs but also on past outputs are called sequential circuits.

A sequential circuit consists of a combinational circuit to which storage elements are connected to form a feedback path. The storage elements are devices capable of storing binary information.

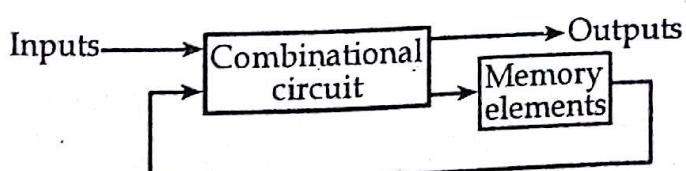


Figure 6.28 Block diagram of a sequential circuit

There are two main types of sequential circuits:

i. **Synchronous sequential circuit**

It is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time.

ii. **Asynchronous sequential circuit**

It is a system whose behavior depends upon the input signals at any instant of time and the order in which the inputs change.

FLIP-FLOP

A flip-flop is a binary storage device capable of storing one bit of information. In a stable state, the output of a flip-flop is either 0 or 1. Flip-flops are synchronous bistable devices, also known as bistable multivibrators. The term 'synchronous' means that the output changes state only at a specified point on a triggering input called the clock (CLK), which is designated as a control input, C; that is, changes in the output occur in synchronization with the clock.

The applications of flip-flop include the following:

- i. Parallel data storage
- ii. Frequency division

Some parts of digital systems operate at a slower rate than the clock (serial I/O, A/D conversion, etc.). Flip-flops can be used to divide the master clock frequency into slower clock cycles for these applications.

- iii. Counting

One of the most important applications of flip-flops is in digital counters. Digital counters not only count things, but are useful as frequency meters, parts of A/D converters, etc.

LATCHES

The latch is a type of temporary storage device that has two stable states (bistable) and is normally placed in a category separate from that of flip-flops. Latches are basically similar to flip-flops because they are bistable devices that can reside

in either of two states using a feedback arrangement, in which the outputs are connected back to the opposite inputs. The main difference between latches and flip flops is in the method used for changing their state. Storage elements that operate with signal levels (rather than signal transitions) are referred to as latches; those controlled by a clock transition are flip-flops. Latches are the basic circuits from which all flip-flops are constructed.

SOME LATCHES

i. SR Latch

The SR latch is a circuit with two cross-coupled NOR gates or two cross-coupled NAND gates, and two inputs labeled 'S' for set and 'R' for reset.

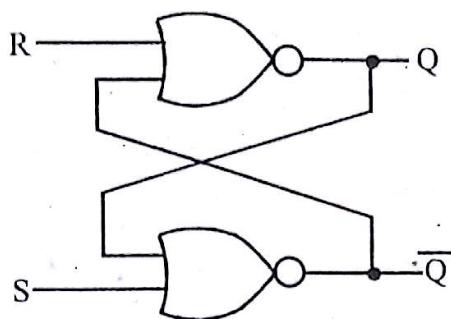


Figure 6.29 Logic diagram

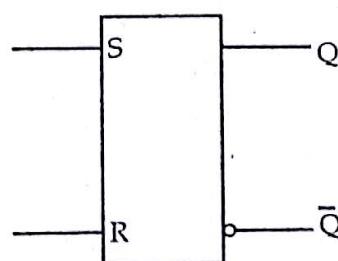


Figure 6.30 Logic symbol

S	R	Q	\bar{Q}
1	0	1	0
0	0	1	0 (after S=1, R=0)
0	1	0	1
0	0	0	1 (after S=0, R=1)
1	1	?	? (invalid)

Table 6.14 Truth table/function table

ii. SR latch with NAND gates

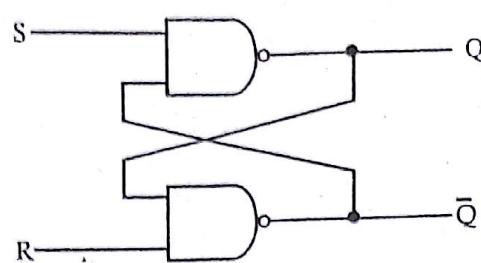


Figure 6.31 Logic diagram

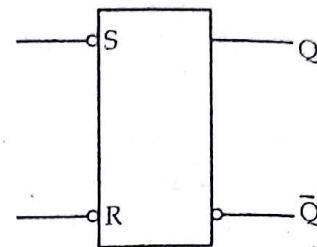


Figure 6.32 Logic symbol

S	\bar{R}	Q	\bar{Q}
1	0	0	1
1	1	0	1 (after S = 1, R = 0)
0	1	1	0
1	1	1	0 (after S = 0, R = 1))
0	0	?	? (invalid)

Table 6.15 Truth table/function table

iii. The Gated SR Latch (SR Latch with Control Input)

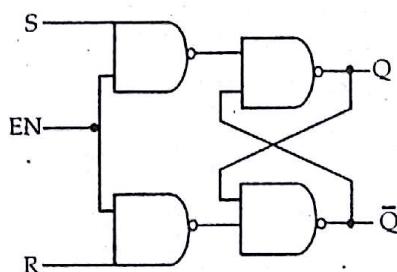


Figure 6.33 Logic diagram

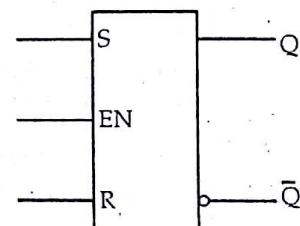


Figure 6.34 Logic symbol

EN	S	R	Q	\bar{Q}	
0	X	X	Q_0	\bar{Q}_0	
1	1	0	1	0	
1	0	0	1	0	(after S = 1, R = 0)
1	0	1	0	1	
1	0	0	0	1	(after S = 0, R = 1)
1	1	1	?	?	(Invalid)

Table 6.16 Truth table/function table

D Latch

The gated D latch

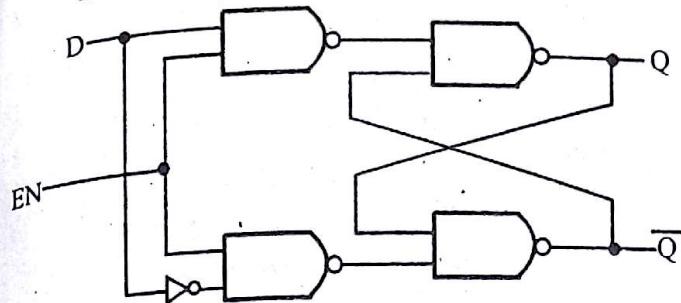


Figure 6.35 Logic diagram

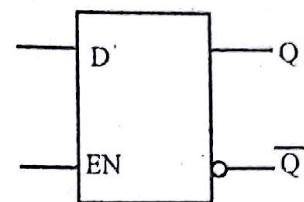


Figure 6.36 Logic symbol

EN	D	Q	\bar{Q}
0	x	Q_0	\bar{Q}_0
1	0	0	1
1	1	1	0

Table 6.17 Truth table/function table

SOME FLIP-FLOPS

i. SR Flip-Flop

SR flip-flop refers to a set-reset flip-flop. When $S=1$ and $R=0$, the output of flip-flop sets (i.e., $Q=1$, $Q'=0$). When $S = 0$ and $R = 1$, it resets (i.e., $Q = 0$, $Q' = 1$). When both inputs are low (i.e., $S = R = 0$), flip-flop will be in latch state (i.e., remains in its previous state). On occasion when both inputs are high (i.e., $S = R = 1$), it will be in indeterminant state.

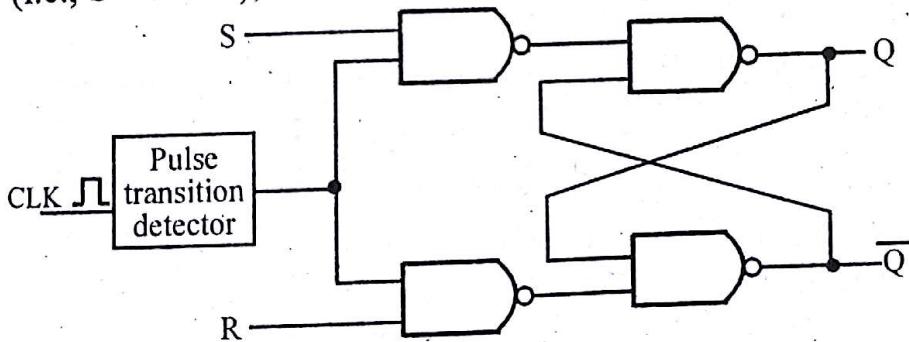


Figure 6.37 Logic diagram

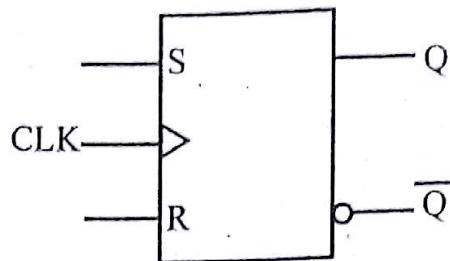


Figure 6.38 Logic symbol

INPUTS			OUTPUTS		COMMENTS
S	R	CLK	Q	\bar{Q}	
0	0	\times	Q_0	\bar{Q}_0	No change (Latch state)
0	1	\uparrow	0	1	RESET
1	0	\uparrow	1	0	SET
1	1	\uparrow	?	?	Invalid (Indeterminant)

\uparrow = Clock transition LOW to HIGH

\times = don't care

Q_0 = previous output

Table 6.18 Truth table

ii. D Flip – Flop

The D flip-flop is useful when a single data bit (1 or 0) is to be stored. It is also called delay flip-flop because it is used as delay circuits. The addition of an inverter to an SR flip-flop creates a basic D flip-flop.

The output of flip-flop sets when D=1 and resets when D=0.

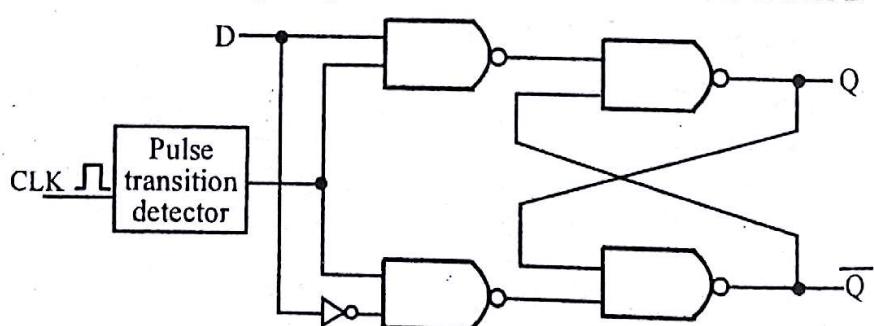


Figure 6.39 Logic diagram

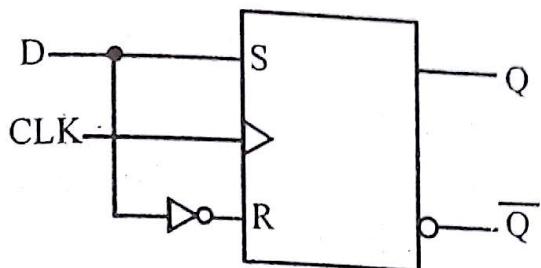


Figure 6.40 Logic symbol

INPUTS		OUTPUTS		COMMENTS
D	CLK	Q	\bar{Q}	
1	↑	1	0	SET
0	↑	0	1	RESET

Table 6.19 Truth table

iii. JK Flip-Flop

JK flip-flop has no invalid state as does the SR flip-flop.

A JK flip-flop is a refinement of the SR flip-flop in that the indeterminate state of the SR type is defined in the JK type. Inputs J and K behave like inputs S and R to set and reset the flip-flop respectively. When $J = K = 1$, the flip-flop output toggles i.e., switches to its complements state; if $Q = 0$ it switches to $Q = 1$ and vice – versa.

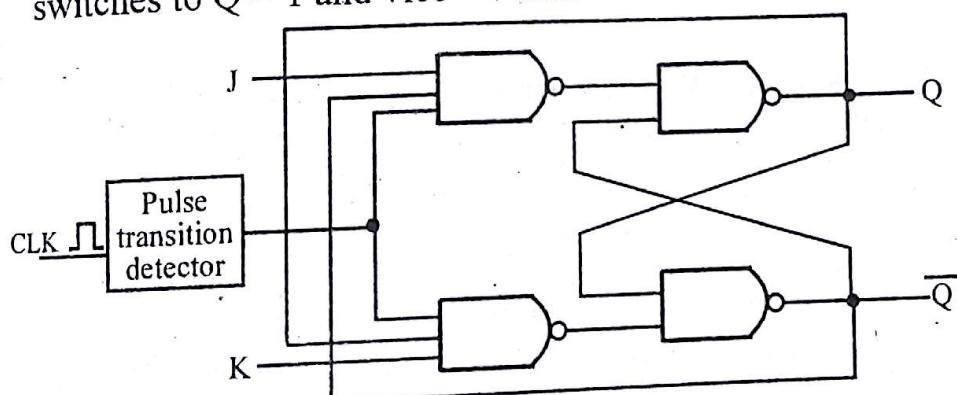


Figure 6.41 Logic diagram

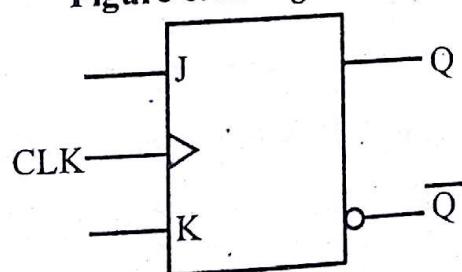


Figure 6.42 Logic symbol

INPUTS			OUTPUTS		COMMENTS
J	K	CLK	Q	\bar{Q}	
0	0	↑	Q_0	\bar{Q}_0	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	\bar{Q}_0	Q_0	Toggle

Table 6.20 Truth table

Race around

When $J = K = 1$ in a JK flip-flop, then present output is the complement of the previous output. That is, if $J = K = 1$ and output is 0, then after the clock pulse, output becomes 1. But if the propagation delay of the gates is much lesser than the clock pulse duration, then during the same pulse, at first output becomes 0 and after another propagation delay, output becomes 1, and so on. Thus, within the same pulse duration, due to very small propagation delays, output oscillates back and forth between 0 and 1. This condition is called race around condition, and at the end of pulse, the output is uncertain.

iv. Master Slave JK Flip-Flop

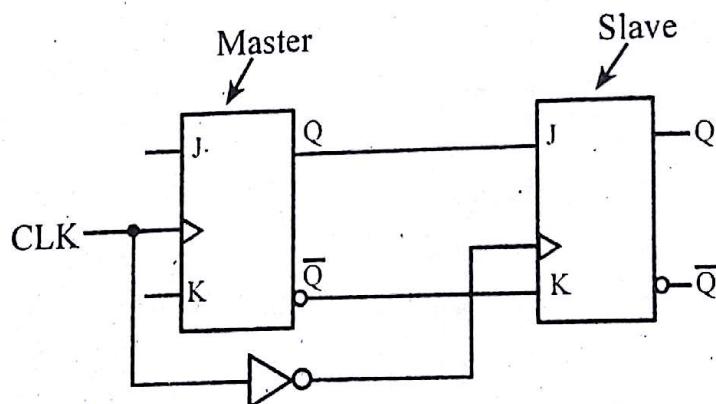


Figure 6.43 Master slave JK flip-flop

To begin with, the master is positive-edge triggered and the slave is negative-edge triggered. Therefore, the master responds to its J and K inputs before the slave. If $J=1$ and

$K=0$, the master sets. The high Q output of the master drives the J input of the slave, so on negative edge of the clock (this makes slave positive-edge triggered), the slave sets copying the action of the master. If $J = 0$, $K = 1$, the master resets when it is positive-edge triggered. The high \bar{Q} output of the master goes to the K input of the slave. So, on negative level of the clock, slave resets. Again, the slave has copied the master. If $J = 1$, $K = 1$, first master toggles its output and later slave does the same. If $J = K = 0$, the flip-flop is disabled and Q remains unchanged.

CHARACTERISTIC TABLE OF DIFFERENT FLIP-FLOPS

S	R	Q_o	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	Invalid
1	1	1	Invalid

Table 6.21 Characteristic table of SR flip-flop

J	K	Q_o	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Table 6.22 Characteristic table of JK flip-flop

D	Q_o	Q
0	0	0
0	1	0
1	0	1
1	1	1

Table 6.23 Characteristic table of D flip-flop

Q_o = previous output

Q = present output

REGISTERS

A register is a group of flip-flops, each one of which is capable of storing one bit of information. An n-bit register consists of a group of n flip-flops capable of storing n bits of binary information. In addition to the flip-flops, a register may have combinational gates that perform certain data-processing tasks.

COUNTERS

A counter is essentially a register that goes through a predetermined sequence of binary states. The gates in the counter are connected in such a way as to produce the prescribed sequence of states. The sequence of states may follow the binary number sequence is called a binary counter. An n-bit binary counter consists of n flip-flops and can count in binary from 0 to $2^n - 1$. Counters are classified into two broad categories according to the way they are clocked: asynchronous and synchronous. In asynchronous counters, commonly called ripple counters, the first flip-flop is clocked by the external clock pulse and then each successive flip-flop is clocked by the output of the preceding flip-flop. In synchronous counters, the clock input is connected to all of the flip-flops so that they are clocked simultaneously.

SHIFT REGISTERS

A register capable of shifting the binary information held in each cell to its neighbouring cell, in a selected direction, is called a shift register. The logical configuration of a shift register consists of a chain of flip-flops in cascade, with the

output of one flip-flop connected to the input of the next flip-flop. All flip-flops receive common clock pulses, which activate the shift of data from one stage to the next.

Serial In/Serial Out Shift Register

The serial in/serial out shift register accepts data serially- that is, one bit at a time on a single line. It produces the stored information on its output also in serial form.

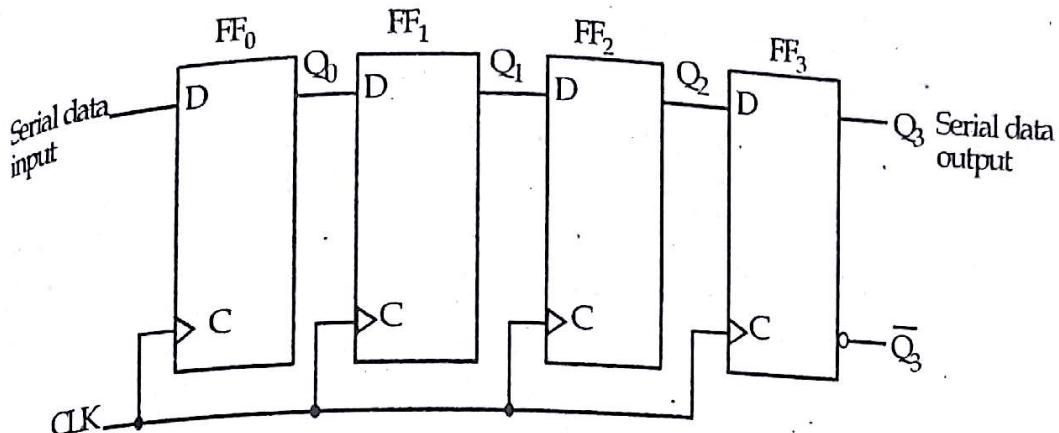


Figure 6.44 Serial in/serial out shift register

ii. Serial In/ Parallel Out Shift Register

In serial in/ parallel out shift register, data bits are entered serially (least-significant bit first). Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously, rather than on a bit-by-bit basis as with the serial output.

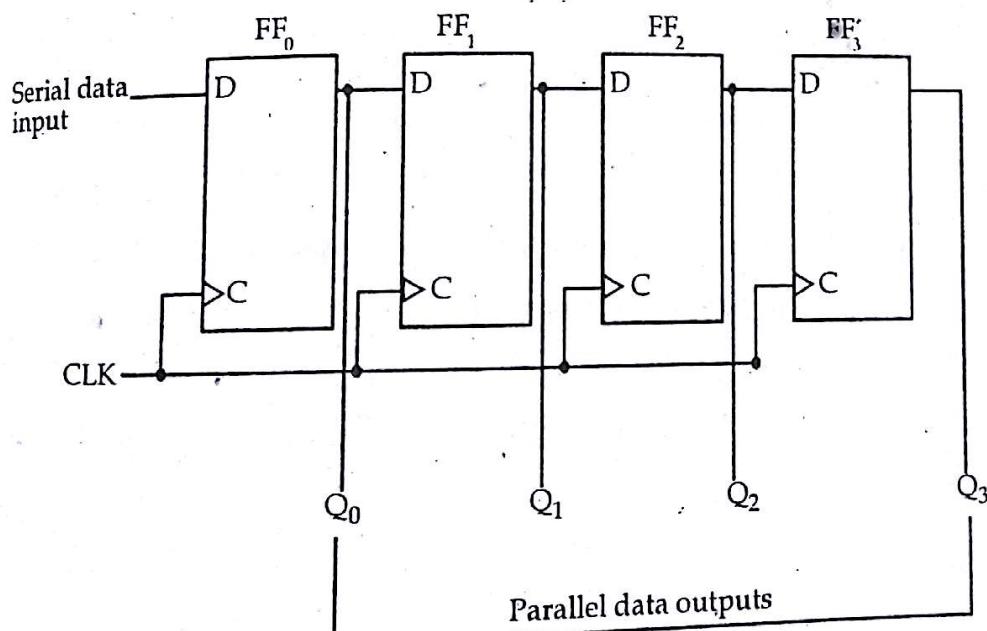


Figure 6.45 Serial in/parallel out shift register

iii. Parallel In/Serial Out Shift Register

In parallel in/serial out shift register, the bits are entered simultaneously into their respective stages on parallel lines rather than on a bit-by-bit basis on one line. Once the data are completely stored in the register, the stored information are retrieved serially (one bit at a time).

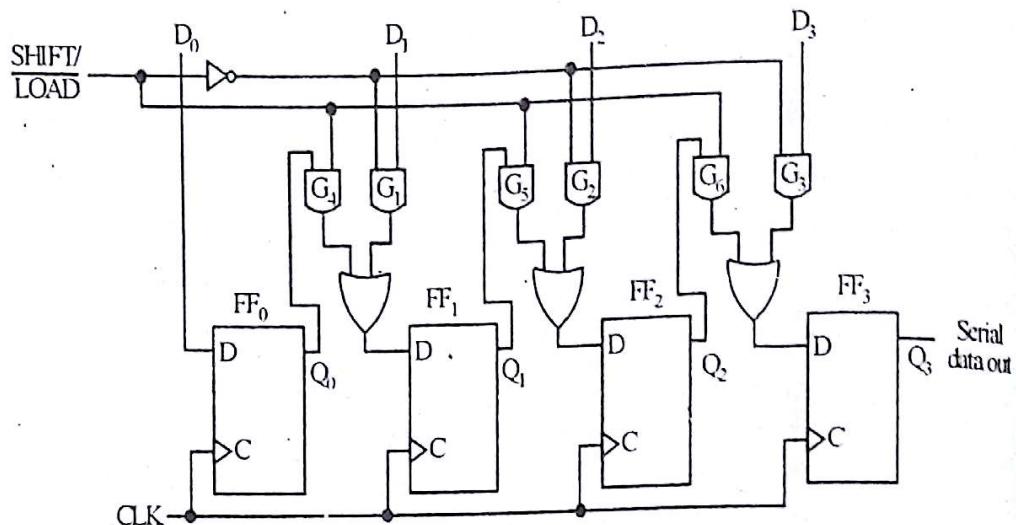


Figure 6.46 Parallel in /serial out shift register

When SHIFT/ LOAD = 0 (low), gates G_1 through G_3 are enabled, allowing each data bit to be applied to the D input of its respective flip-flop.

When SHIFT/ LOAD = 1 (HIGH), gates G_1 through G_3 are disabled and gates G_4 through G_6 are enabled, allowing the data bits to shift right from one stage to the next.

iv. Parallel In/Parallel Out Shift Register

In parallel in/parallel out shift register, the bits are entered simultaneously into their respective stages on parallel lines. Immediately following this, the bits appear on the parallel outputs.

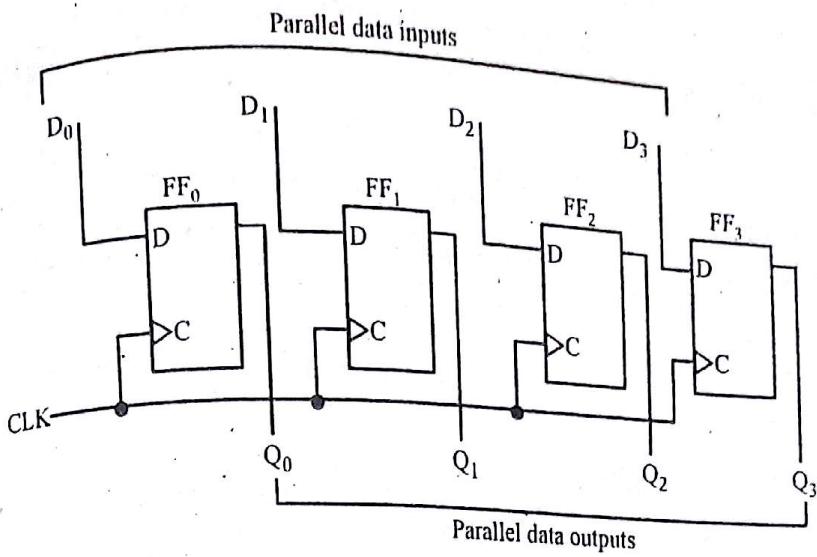


Figure 6.47 Parallel in/parallel out shift register

DUALITY PRINCIPLE

The duality principle states that a Boolean expression remains valid if operators OR and AND are interchanged and 1's and 0's in the expression are also interchanged.

In order to understand this principle, consider the Boolean theorem

$$A + 0 = A$$

According to duality principle, this Boolean expression remains valid if OR function is replaced by AND function and 0 by 1. In that case, the Boolean expression becomes:

$$A \cdot 1 = A$$

To apply duality principle to a Boolean expression, we simply interchange OR and AND operator and replace 1's by 0's and 0's by 1's.

ANSWERS TO SOME QUESTIONS

- 1.** Draw a block diagram of edge triggered, with preset and clear facilities of D flip-flop and its truth table. State one important advantage over RS flip-flop. [2067 Chaitra]

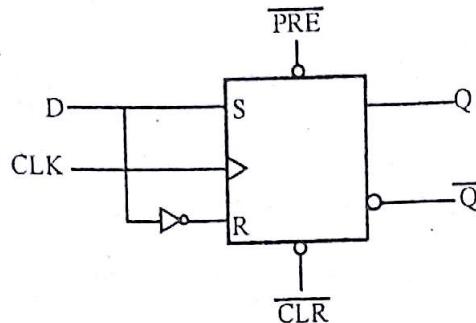


Fig.: Block diagram of a D flip-flop with preset and clear facilities.

Truth table

INPUTS		OUTPUTS		COMMENTS
D	CLK	Q	\bar{Q}	
1	↑	1	0	SET
0	↑	0	1	RESET

↑ = clock transition from low to high

Advantage of D flip-flop over RS flip-flop

Inputs to the D flip-flop are never similar, they are in complemented form. Hence, invalid output is restricted in D flip-flop.

- 2.** Draw a 3 – bit counter circuit.

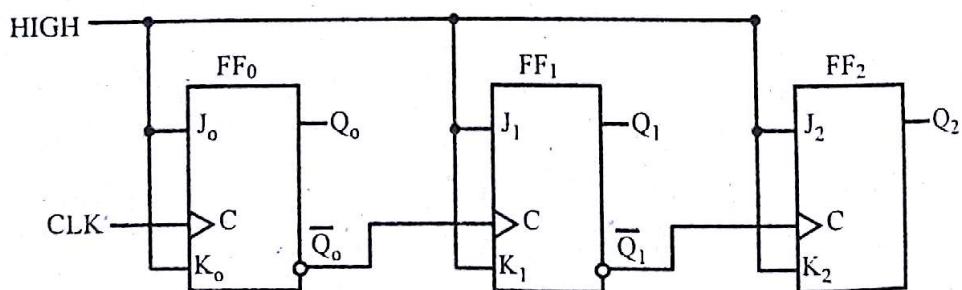


Fig.: A 3-bit asynchronous binary counter.

Clock pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

3. Express -39 as an 8 bit number in the sign magnitude, 1's complement, and 2's complement forms.

Solution:

Sign magnitude

First, $+39 = 00100111$

$-39 = 10100111$

In the **1's complement form**, -39 is produced by taking the 1's complement of $+39$ (00100111).

Therefore, $(11011000)_2$ Ans

In the **2's complement form**, -39 is produced by taking the 2's complement of $+39$.

Therefore, $(11011001)_2$ Ans

4. Design a full-adder using two half adders.

Solution:

For half-adder,

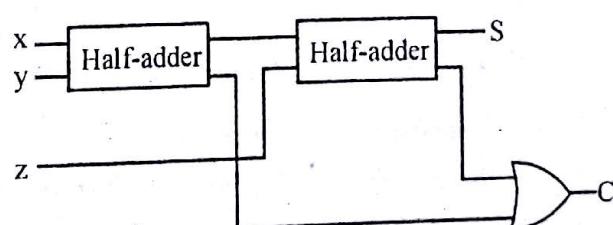
$$\text{Sum} = x \oplus y$$

$$\text{Carry} = xy$$

For full-adder,

$$\text{Sum}(S) = x \oplus y \oplus z$$

$$\text{Carry } (C) = (x \oplus y)z + xy$$



*Fig.: A full-adder using
two half-adders*

Application Of Electronic System

INTRODUCTION

An electronic system is a physical interconnection of components, or parts, that gathers various amounts of information together. It does this with the aid of input devices such as transducers and sensors, that respond in some way to this information and then uses electrical energy in the form of an output action to control a physical process or perform some type of mathematical operation on the signal. A simple electronic system consists of an input, a process, and an output with the input variable to the system and the output variable from the system both being signals. Electronic systems are generally represented schematically as a series of interconnected blocks and signals with each block having its own set of inputs and outputs; the representation commonly known to us as "block diagram representation".

TRANSDUCERS AND SENSORS

Sensors provide us with a means of generating signals that can be used as inputs to electronic circuits. The things that we might want to sense include physical parameters such as temperature, light level, and pressure. Being able to generate an electrical signal that accurately represents these quantities allows us not only to measure and record these values but also to control them. Sensors are, in fact, a subset of a larger family of devices known as transducers. So, we will consider these before we look at sensors.

Transducers

Transducers are devices that convert energy in the form of sound, light, heat, etc. into an equivalent electrical signal or vice-versa. For example, a loudspeaker is a transducer that converts low frequency electric current into audible sounds. A microphone, on the other hand, is a transducer that performs

the reverse function i.e., that of converting sound pressure variations into voltage or current.

Transducers may be used as both inputs to electronic circuits and outputs from them. In this view, a loudspeaker is an "output transducer" designed for use in conjunction with an audio system. Whereas, a microphone is an "input transducer" designed for use with a recording or sound reinforcing system.

Examples:

- i. Potentiometer device - for the measurement of pressure, displacement.
- ii. Resistance strain gauge - for the measurement of force, torque, displacement.
- iii. Photoemissive cell - for the measurement of light and radiation.
- iv. Resistance thermometer - for the measurement of temperature, radiant heat.

The transducers are of different types and the classification may be:

- i. On the basis of transduction form used.
- ii. As primary and secondary transducers.
- iii. As passive and active transducers.
- iv. As analog and digital transducers.
- v. As transducers and inverse transducers.

Sensors

A sensor is a special kind of transducer that is used to generate an input signal to a measurement, instrumentation, or control system. The signal produced by a sensor is an electrical analogy of a physical quantity such as distance, velocity, acceleration, temperature, pressure, light level, etc. The choice of sensor is governed by a number of factors including accuracy, resolution, cost, and physical size.

Sensors can be categorized on various basis as

- i. Active or passive
- ii. Digital or analogue

Examples:

- i. Photocell – for measuring light level.
- ii. Rotating vane flow sensor – for measuring flow.
- iii. Tachogenerator – for measuring angular velocity.
- iv. Float switch – for measuring liquid level.

MEASUREMENT AND INSTRUMENTATION SYSTEM

The measurement of a given quantity is essentially an act or the result of comparison between the quantity (whose magnitude is unknown) and a predefined standard.

Instrumentation system is a collection of instruments, devices, hardware or functions or their applications for the purpose of measuring, monitoring or controlling an industrial process or machine or any combination of these.

The instrumentation systems can be classified into two distinct categories:

1. Analog systems
2. Digital systems

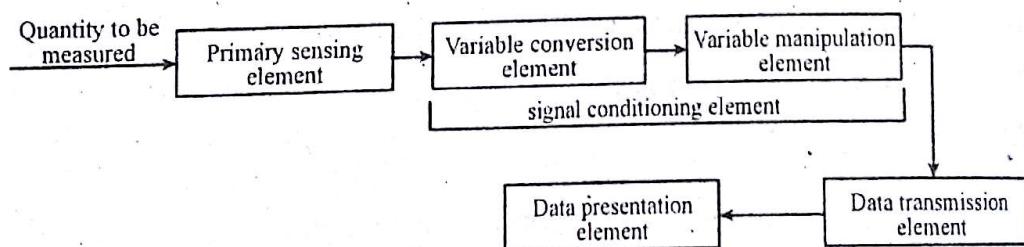


Figure 7.1 Functional elements of an instrumentation system

Figure 7.1 shows the arrangement of an instrumentation system. The physical quantity to be measured (e.g., temperature) acts upon a primary sensing element that produces an electrical output signal. This signal is an electrical analogue of the physical input but it should be noted that there may not be a linear relationship between the physical quantity and its electrical equivalent. Because of this and since the output produced by the primary sensing element may be small

or may suffer from the presence of noise i.e., unwanted signals, further signal conditioning is required to make the signal at an acceptable level. Signal conditioning involves any or all of these stages: amplifying, wave shaping, filtering, rectifying. Then, data transmission is achieved to a location of our interest and finally, displayed on LCD, LEDs, or other displaying devices.

STRAIN GAUGE

A strain gauge is a device used to measure the strain of an object. When an electrical conductor is stretched or compressed, its length, cross-sectional area, and resistivity changes and hence, the electrical resistance. This is the principle of operation of strain gauge.

The strain gauges are used for the measurement of strain and associated stress in experimental stress analysis. Secondly, many other detectors and transducers, notably the load cell, torque meters, diaphragm type pressure gauges, temperature sensors, accelerometers, and flow meters employ strain gauges as secondary transducers.

Working principle

Consider a strain gauge made of circular wire of resistivity ρ having length l , and area of cross-section A . On the application of tensile force normal to the cross-sectional area, let Δl , ΔD , $\Delta \rho$, and ΔR be the change in length, diameter, resistivity, and resistance respectively.

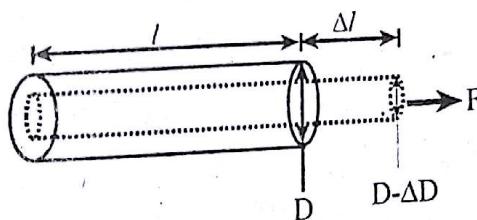


Figure 7.2 An electrical conductor being stretched on the application of force, F

$$\text{Resistance of unstrained gauge, } R = \rho l/A$$

Differentiating both sides w.r.t. S , we have

$$\frac{dR}{dS} = \frac{\rho}{A} \frac{\partial \ell}{\partial S} - \frac{\rho \ell}{A^2} \frac{\partial A}{\partial S} + \frac{\ell}{A} \frac{\partial \rho}{\partial S}; S = \text{tensile stress}$$

Dividing throughout by $R = \rho \ell / A$, we get

$$\frac{1}{R} \frac{dR}{dS} = \frac{1}{\ell} \frac{\partial \ell}{\partial S} - \frac{1}{A} \frac{\partial A}{\partial S} + \frac{1}{\rho} \frac{\partial \rho}{\partial S}$$

$$\text{Here, } \frac{1}{A} \frac{\partial A}{\partial S} = \frac{2}{D} \frac{\partial D}{\partial S} \left(\because A = \frac{\pi D^2}{4} \right)$$

$$\therefore \frac{1}{R} \frac{dR}{dS} = \frac{1}{\ell} \frac{\partial \ell}{\partial S} - \frac{2}{D} \frac{\partial D}{\partial S} + \frac{1}{\rho} \frac{\partial \rho}{\partial S} \dots \text{(i)}$$

Poisson's ratio is

$$\nu = \frac{\text{lateral strain}}{\text{longitudinal strain}} = \frac{-\frac{\partial D}{D}}{\frac{\partial \ell}{\ell}} \Rightarrow \frac{\partial D}{D} = -\nu \frac{\partial \ell}{\ell}$$

Equation (i) is then reduced to

$$\frac{1}{R} \frac{dR}{dS} = \frac{1}{\ell} \frac{\partial \ell}{\partial S} + \frac{2\nu}{\ell} \frac{\partial \ell}{\partial S} + \frac{1}{\rho} \frac{\partial \rho}{\partial S}$$

For small variations, we can write

$$\frac{\Delta R}{R} = \frac{\Delta \ell}{\ell} + 2\nu \frac{\Delta \ell}{\ell} + \frac{\Delta \rho}{\rho} \dots \text{(ii)}$$

$$\text{where gauge factor (G}_f\text{)} = \frac{\frac{\Delta R}{R}}{\frac{\Delta \ell}{\ell}}$$

$$\text{or, } \frac{\Delta R}{R} = G_f \frac{\Delta \ell}{\ell} = G_f; \varepsilon = \text{strain}$$

Equation (ii) now becomes

$$G_f \varepsilon = \varepsilon + 2\nu \varepsilon + \frac{\Delta \rho}{\rho}$$

$$\text{or, } G_f = 1 + 2\nu + \frac{\rho}{\varepsilon}$$

If $\Delta \rho$ is considered negligible, then

$$G_f = 1 + 2\nu$$

DIGITAL MULTIMETER (DMM)

A piece of test equipment used for measuring voltage, current, resistance, and possibly other electrical quantities and displaying the value in number form is called digital multimeter.

Figure 7.3 below shows the controls and display provided by a simple digital multimeter. The display fitted to a digital multimeter usually consists of a $3\frac{1}{2}$ -digit seven-segment display- the $\frac{1}{2}$ simply indicates that the first digit is either blank (zero) or 1. The mode switch and range selector allow us to select different ranges and measurement functions. These functions are:

- i. DC voltage
- ii. DC current
- iii. AC voltage
- iv. AC current
- v. Resistance
- vi. Capacitance
- viii. Continuity test (buzzer)
- ix. Transistor current gain (h_{FE})

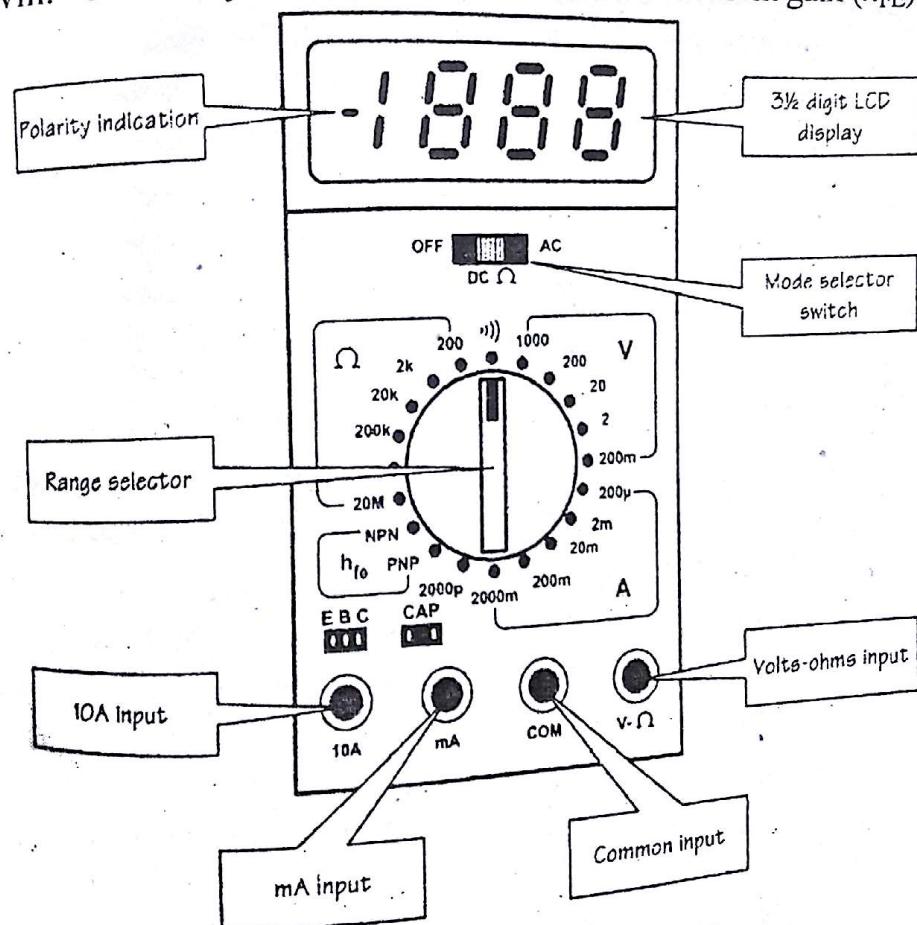


Figure 7.3 Digital multimeter display and controls

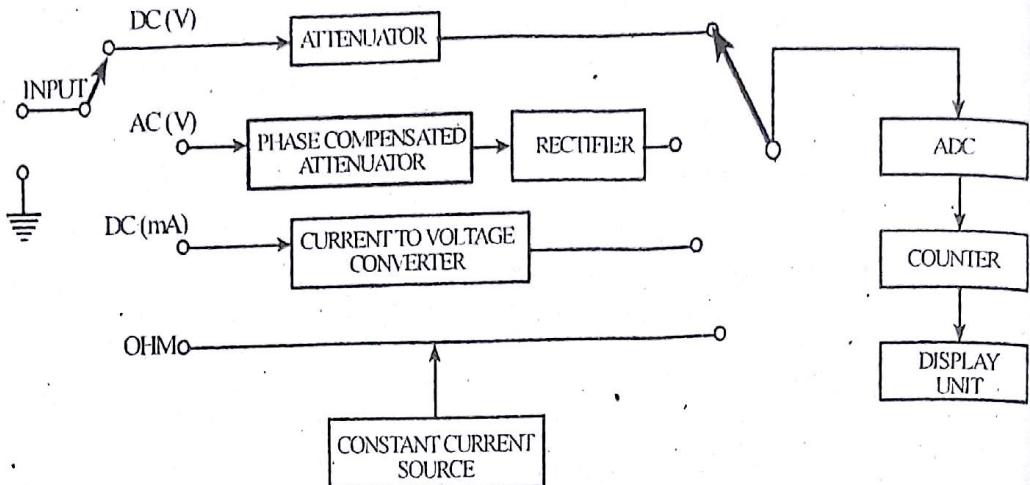


Figure 7.4 Block diagram of a digital multimeter

Explanation:

Before measuring, all quantities other than DC voltage are first converted into an equivalent DC voltage by some device.

For the measurement of DC voltage, the input DC voltage is first passed through attenuator. For the measurement of AC voltage, the input AC voltage is fed to compensated attenuator and then passed to rectifier to obtain DC voltage. If we want to measure current (DC), it is passed through "current to voltage converter" and finally, reading is observed. Measurement of resistance involves passing a constant current from constant current source through the resistance and then measuring the corresponding voltage to calculate resistance.

DO's and DON'Ts of using a digital multimeter:

- DO ensure that you have selected the correct range and measuring function before attempting to connect the meter into a circuit.
- DO select a higher range than expected and then progressively increase the sensitivity as necessary to obtain a meaningful indication.
- DO switch the meter to the 'off' position in order to conserve battery life when the instrument is not being used.
- DO check and, if necessary, replace the internal battery regularly.

- DO use properly insulated test leads and prods.
- DO check that a suitably rated fuse is used in conjunction with the current ranges (if the current ranges aren't working, it's probably the fuse that's blown!).
- DON'T attempt to measure resistance in a circuit that has the power applied to it.
- DON'T rely on voltage and current readings made on circuits where high-frequency signals may be present (as with analogue instruments, digital meters may produce readings that are wildly inaccurate or misleading in such circumstances).
- DON'T rely on measurements made when voltage/current is changing or when a significant amount of AC may be present superimposed on a DC level.

CATHODE RAY OSCILLOSCOPE (CRO)

The cathode ray oscilloscope (CRO) is a very useful and versatile laboratory instrument used for display, measurement, and analysis of waveforms and other phenomena in electrical and electronic circuits. CROs are in fact very fast X-Y plotters, displaying an input signal versus another signal or versus time. From this graph, it is possible to:

- determine the time and voltage values of a signal
- calculate the frequency of an oscillating signal
- see the 'moving parts' of a circuit represented by the signal
- tell if a malfunctioning component is distorting the signal
- find out how much of a signal is d.c. or a.c.
- tell how much of the signal is noise and whether the noise is changing with time.

Working principle:

When an oscilloscope probe is connected to a circuit, the voltage signal travels through the probe to the vertical system

of the oscilloscope. Figure 7.5 below shows a simple block diagram of a cathode ray oscilloscope.

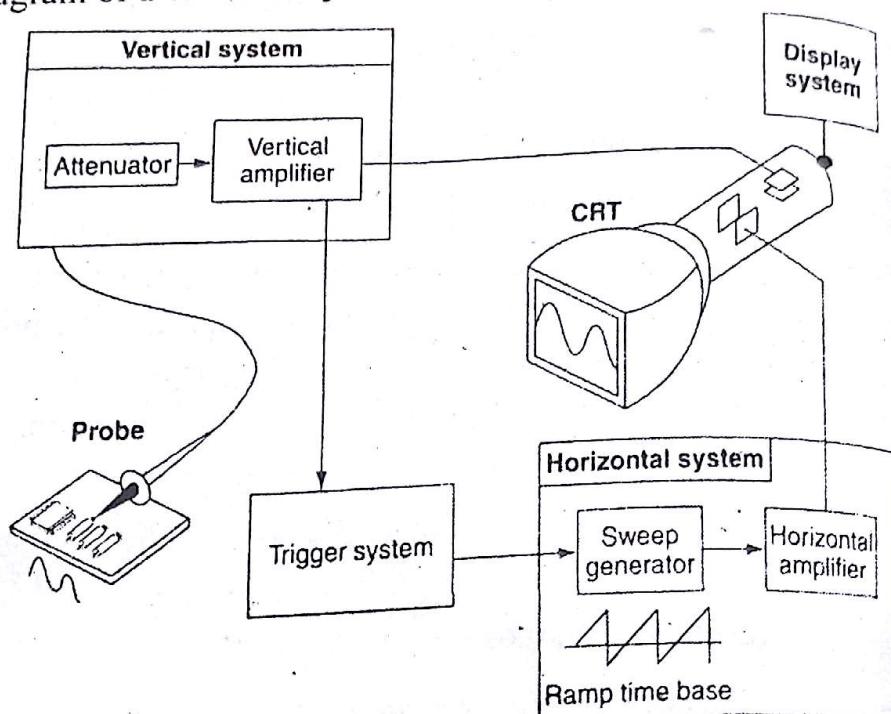


Figure 7.5 Block diagram of a general purpose CRO

Depending on how the vertical scale (volts/division control) is set, an attenuator reduces the signal voltage or an amplifier increases the signal voltage. Next, the signal travels directly to the vertical deflection plates of the cathode ray tube (CRT). Voltage applied to these deflection plates causes a glowing dot to move (An electron beam hitting phosphor inside the CRT creates the glowing dot.). A positive voltage causes the dot to move up while a negative voltage causes the dot to move down. The signal also travels to the trigger system to start or trigger a 'horizontal sweep'. Horizontal sweep is a term referring to the action of the horizontal system causing the glowing dot to move across the screen. Triggering the horizontal system causes the horizontal time base to move the glowing dot across the screen from left to right within a specific time interval. Many sweeps in rapid sequence cause the movement of the glowing dot to blend in a solid line. At higher speeds, the dot may sweep across the screen up to 500000 times each second.

Together, the horizontal sweeping action (i.e., the X direction) and the vertical deflection action (i.e., the Y direction), traces a graph of the signal on the screen. The trigger is necessary to stabilize a repeating signal. It ensures that the sweep begins at the same point of a repeating signal, resulting in a clear picture.

Uses:

Oscilloscopes are used by everyone from television repair technicians to physicists. They are indispensable for anyone designing or repairing electronic equipment. With the proper transducer, an oscilloscope can measure any kind of physical phenomena (sound, pressure, heat, light, etc.). An automobile engineer uses an oscilloscope to measure engine vibrations; a medical researcher uses an oscilloscope to measure brain waves, and so on.

REGULATED POWER SUPPLY (DC POWER SUPPLY)

The regulated power supply circuit keeps the output voltage constant inspite of change in load current or input voltage.

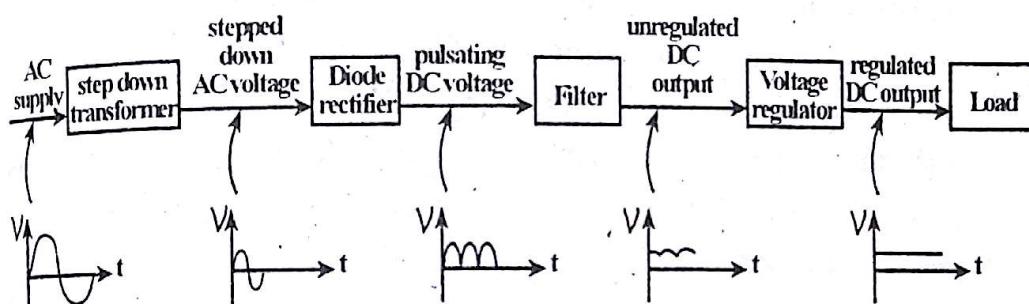


Figure 7.6 Block diagram of a regulated power supply

Explanation:

The transformer steps down the AC voltage to the level required for the desired DC output. The rectifier circuit converts this stepped down voltage into a pulsating DC voltage, which has large ripple content. The filter circuit used after a rectifier circuit reduces the ripple content in the pulsating DC voltage and tries to make it smoother. But still, the output of the filter has some ripple. This voltage is called unregulated DC voltage. To make the DC voltage almost ripple free and to make the output DC voltage stable against variations caused by changes in load current, a voltage

regulator is employed. Finally, the regulated DC voltage is fed to load.

REMOTE CONTROL

A remote control is a component of an electronic device, most commonly a television set, DVD player, home theatre systems, and dimmers, originally used for operating the television device wirelessly from a short line-of-sight distance. Remote control has continually evolved and advanced over recent years to include Bluetooth connectivity, motion sensor enabled capabilities, and voice control.

Remote controls are usually small wireless handheld objects with an array of buttons for adjusting various settings such as television channel, track number, and volume. In fact, for the majority of modern devices with this kind of control, the remote contains all the function controls while the controlled device itself only has a handful of essential primary controls.

Most remote controls for electronic appliances use a near infrared diode to emit a beam of light that reaches the device (Few remote controls operate by radio frequency waves). A 940 nm wavelength LED is typical. This infrared light is invisible to the human eye, but picked up by sensors on the receiving device.

Remote control may be classified as:

- i. Single channel (single-function, one-button) remote control.
- ii. Multi channel (normal multi-function) remote control.

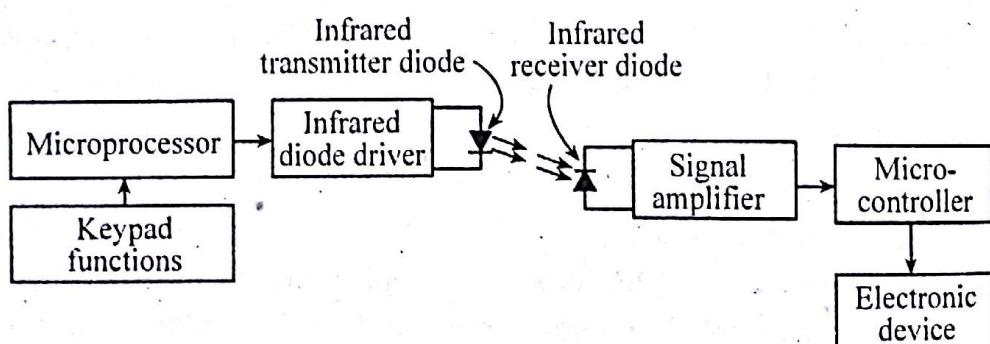


Figure 7.7 Block diagram of a microcontroller based infrared remote control

Explanation:

In all keypad, all functions are listed as buttons for switching given function. When we switch a function, the related switch is closed and microprocessor gets triggered. The control bits from the microprocessor are modulated and sent to infrared diode driver and finally, LED emits the signal in the form of infrared light waves. The infrared signal is received by photodiode or phototransistor which converts the infrared signal into electrical signal. The electrical signal is then demodulated and corresponding control bits are decoded in microcontroller to perform desired function in electronic device.

CHARACTER DISPLAY

Character display is the display of alphanumeric characters.

i. Dot matrix display

A dot matrix display is a display device that consists of a dot matrix of lights or mechanical indicators arranged in a rectangular configuration (most common) such that by switching on or off selected lights, text or graphics can be displayed. A dot matrix controller converts instructions from a processor into signals which turns on or off lights in the matrix so that the required display is produced.

Dot matrix displays are used to display information on machines, clocks, railway and plane arrival (or departure) indicators, etc.

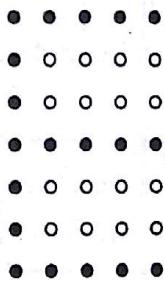


Figure 7.8 Displaying letter E using 5×7 dot matrix

ii. Seven-segment display

A seven-segment display (SSD) or seven segment indicator is a form of electronic display device for displaying decimal

numerals that is an alternative to the more complex dot matrix displays. By illuminating the proper combination of these seven segments (made up of LED or LCD), numbers from 0 to 9 can be displayed.

Seven-segment displays are widely used in digital clocks, electronic meters, and other electronic devices for displaying numerical information.



Figure 7.9 Seven segment display number 3

CLOCK COUNTER MEASUREMENT

Clock counter measurement is common for many physical parameters. There are many clock counter measurements—ramp counter, integration op-amp counter, count up measurements, successive counting measurements.

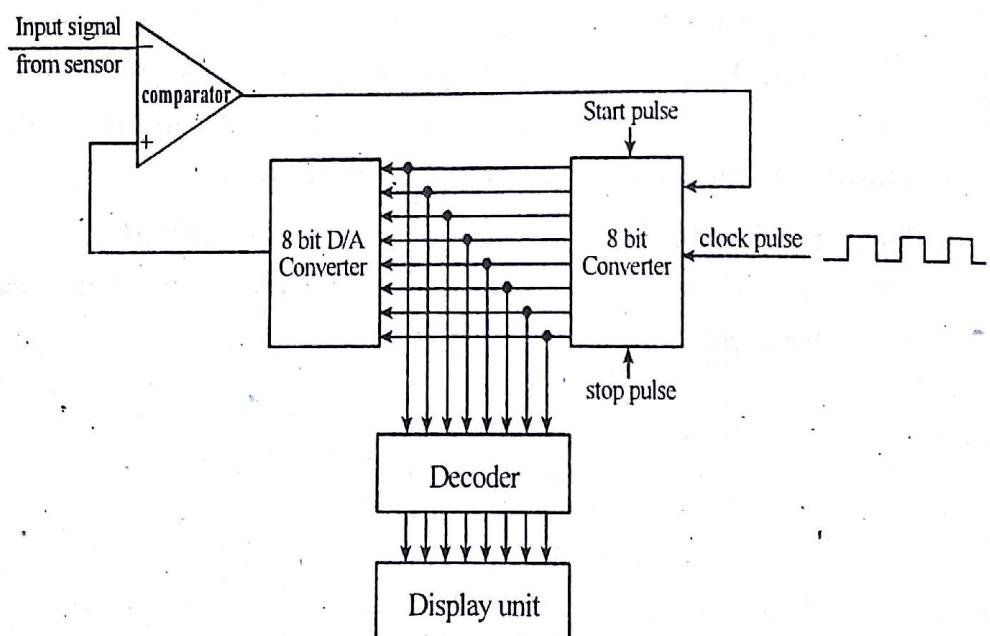


Figure 7.10 Block diagram of a clock counter measurement (count up type)

Explanation:

The DC voltage to be measured from the sensor is fed to a comparator. The negative high output, initially from the

comparator is then passed to counter and with input of clock pulse, the MSB of counter is set high and all other bits low. These bits are the input to D/A converter whose output is corresponding analog voltage of binary pattern in counter and is fed to the non-inverting terminal of the comparator. If the output of the comparator is still negative, then the bit one significant less than MSB is set retaining MSB high. If the output is greater than zero, MSB is reset and the bit one significant less than MSB is set. In this way, the process continues until the output from comparator is zero or nearly zero. The binary value in counter when the output of comparator is zero or nearly zero is the final digital value of the input analog voltage from the sensor.

DATA LOGGER

A data logger (or data recorder) is an electronic device that records data over time or in relation to location of instrument at different parts of the plant effortlessly as quickly as often and as accurately as desired. Increasingly, but not entirely, they are based on a digital processor (or computer). They generally are small, battery powered, portable, and equipped with a microprocessor, internal memory for data storage, and sensors.

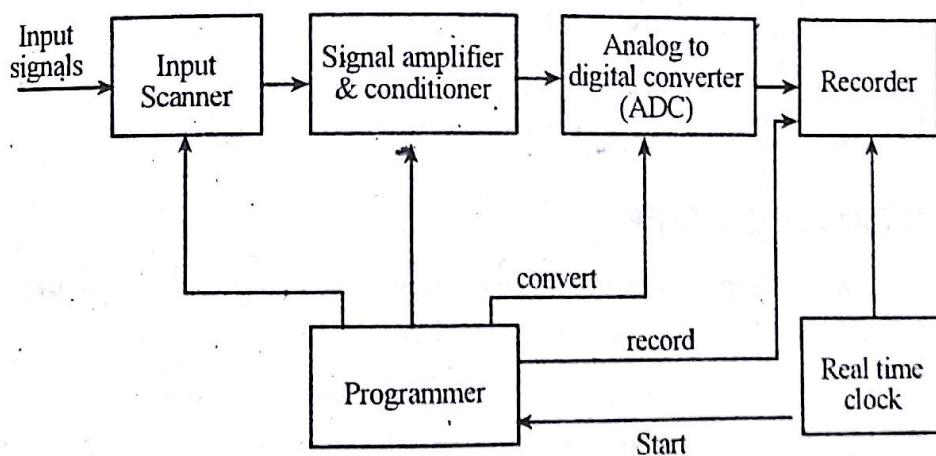


Figure 7.11 Block diagram of a data logger

- Input signals:** It may be high level signals from pressure transducer, low level signals from thermocouple, AC, ON, OFF signals from switch and relays, etc.

- ii. **Input scanner:** It is an automatic sequence switch which selects each signal in turn.
- iii. **Signal amplifier:** It amplifies low level signal up to 5V output.
- iv. **Signal conditioner:** It changes signal to more linear and suitable form for digital analysis.
- v. **Analog to digital converter:** It converts the analog signals to digital signals suitable for driving the recording equipment.
- vi. **Recorder:** A recorder records electrical and non-electrical quantities as a function of time. The record may be written or printed.
- vii. **Programmer:** The programmer is used to control the sequence of operation of various items of data logger.
- viii. **Real time clock:** It commands programmer to sequence one set of measurement at the intervals selected by user.

Application areas:

1. Weather station recording (wind, speed, temperature, humidity, etc.)
2. Hydrographic recording (water level, depth, flow, etc.)
3. Wildlife research
4. Vehicle testing
5. Environmental monitoring.

AUDIO VIDEO SYSTEM

A system in which information exchange takes place in audio-visual environment i.e. message/ information consists of audio-video signals is called audio video system. For example, television, telemedicine services, teleconferencing services, etc.

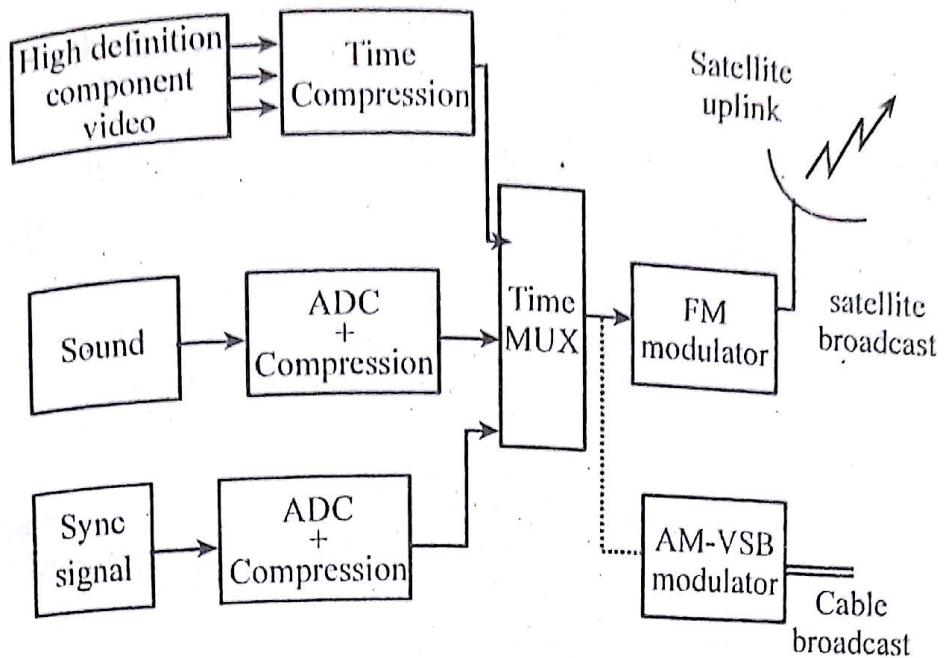


Figure 7.12 Typical audio video transmission

- High definition Video from HD camera is taken and time compression is applied.
- Sound and sync signals are digitized using ADC and compressed to reduce bit rate.
- Time compressed HD - Video, digitally compressed sound and sync signals are time multiplexed according to standards.
- The standard signal are then modulated and transmitted FM modulation is done if satellite broadcasting is there and AM-VSB modulation is done if cable broadcasting is to be done.

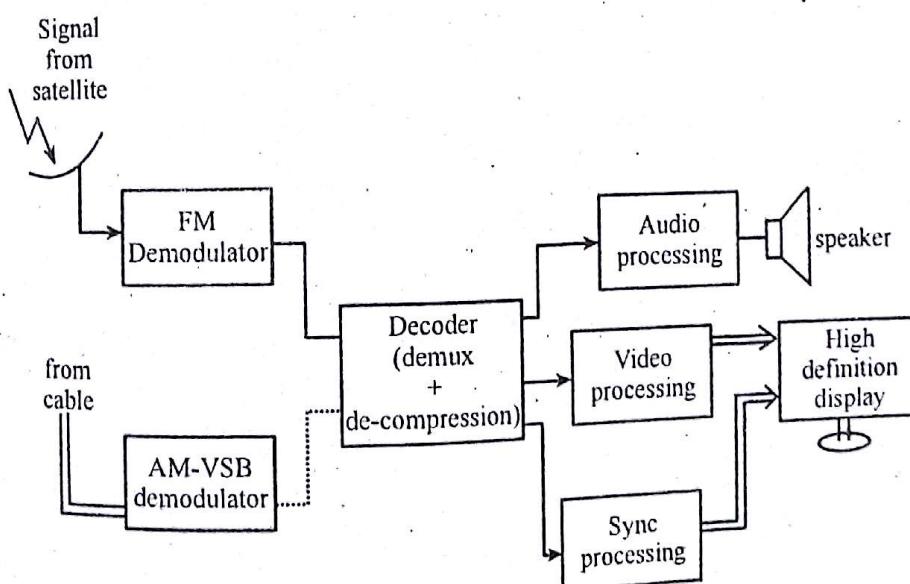


Figure 7.13 Typical audio video reception

- Incoming signal is selected and signal demodulation takes place.
- Demodulated signal output gives compressed video bit stream, compressed sync bit stream and uncompressed audio bit stream.
- Thus, video bit stream is processed by video processing stage where decompression and D to A conversion takes place.
- Audio stream is processed by audio processing stage where DAC is used to convert digitized audio into analog audio signal and then it is pre-amplified and power amplified.
- Finally, video is displayed on high definition display and sound through speaker.

ANSWERS TO SOME QUESTIONS

1. How do you define analog and digital systems? Write down the advantages of digital system over analog system.

An "analog system" contains devices that manipulate the physical quantities represented in analog form. In an analog system, the quantities can vary continuously over a range of values. For example, the amplitude of output signal of the speaker in a radio receiver can have any value between zero and its maximum limit. A "digital system" is a combination of devices designed for manipulating physical quantities or information represented in digital form, that is, they can take only discrete values. Some of the familiar digital systems are calculators, digital watches, digital computers, etc.

Advantages of digital system over analog system:

- i. Greater accuracy and precision.
- ii. Storage of information is easier.
- iii. Digital systems are less affected by noise.

2. Comparison of Digital and Analog Instruments

[2068 Magh]

Digital and analog instruments can be compared under the following headings:

- i. **Accuracy:** Digital instruments can be made to much greater accuracies than the best analog instruments.
- ii. **Reaction to environment:** Analog meter movements are relatively simple and will operate under a wide range of environments. Digital instruments are relatively complex and consist of large number of parts which individually will react to change in temperature and humidity.
- iii. **Resolution:** This is the readability below which differences can no longer be differentiated. In analog instruments, the limit is one part in several hundreds. Digital instruments can be made with a resolution of one part in several thousands.

- iv. **Power requirements:** Digital instruments draw only negligible power whereas the analog instruments draw a large amount of power.
- v. **Cost and portability:** Analog instruments are low in cost and extremely portable whereas digital instruments are not portable. However, modern developments have made digital instruments low in cost and extremely portable.
- vi. **Range and polarity:** Many digital instruments incorporate automatic polarity and range indication. These features are not available in analog instruments.
- vii. **Freedom from observational errors:** The digital instruments are free from observational errors while analog instruments have considerable observational errors.

3. Application circuit of strain gauge [2068 Magh]

Wheatstone bridge can be employed for the measurement of small resistance change that occurs in strain gauge.

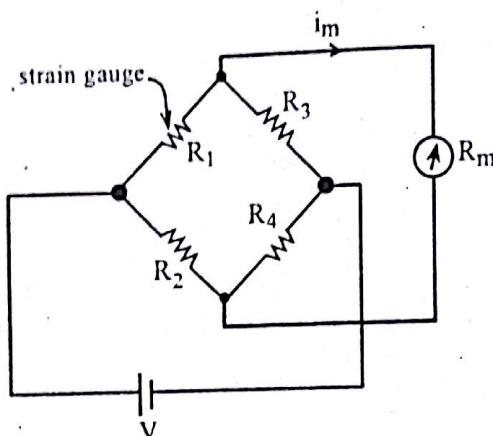


Fig.: Application circuit of strain gauge

The resistive arm R₁ is a strain gauge whose resistance changes as per the strain produced in it. With no strain applied on arm R₁, the bridge is in balanced condition with

$$\frac{R_1}{R_2} = \frac{R_3}{R_4}$$

When the strain is applied across the arm R₁, the bridge becomes unbalanced. This leads to the flow of current through the meter,

R_m . This current, i_m is proportional to change in resistance caused by application of strain on R_1 . The readout value of current by the meter is calibrated with the value of strain being measured to obtain the value of strain.

4. Describe active and passive transducers. [2072 Ashwin]

Active transducers

These transducers do not need any external source of power for their operation. Therefore, they are also called "self generating type" transducers. Active transducers generate electric current or voltage directly in response to environmental stimulation. Examples of active transducers are thermocouples and piezoelectric accelerometers.

Passive transducers

These transducers need external source of power for their operation. Passive transducers produce a change in capacitance, resistance, or inductance in response to environmental stimulation. Examples of passive transducers are strain gauges, resistance temperature detectors, and thermistors.

APPENDIX

Parameter	Common emitter	Common collector	Common base
Voltage gain	medium/high (40)	unity (1)	high (200)
Current gain	high (200)	high (200)	unity (1)
Power gain	very high (8000)	high (200)	high (200)
Input resistance	medium ($2.5\text{K}\Omega$)	high ($100\text{K}\Omega$)	low (200Ω)
Output resistance	medium/high ($20\text{K}\Omega$)	low (100Ω)	high ($100\text{K}\Omega$)
Phase shift	180°	0°	0°
Typical applications	General purpose, AF and RF amplifiers	Impedance matching, input and output stages	RF and VHF amplifiers

Table 1 Characteristics of BJT amplifiers

Particulars	Half-wave rectifiers	Full-wave rectifiers	
		Centre-tap	Bridge
Number of diodes required	1	2	4
Average value of current, I_{dc}	I_{op}/π	$2I_{op}/\pi$	$2I_{op}/\pi$
RMS value of current, I_{rms}	$I_{op}/2$	$I_{op}/\sqrt{2}$	$I_{op}/\sqrt{2}$
DC output voltage, V_{dc}	$\frac{I_{op}}{\pi} R_L$	$\frac{2I_{op}}{\pi} R_L$	$\frac{2I_{op}}{\pi} R_L$
Rectification efficiency (max.)	40.6%	81.2%	81.2%
Ripple factor	1.21	0.482	0.482
Voltage regulation	good	better	good
Form factor	1.57	1.11	1.11
Peak factor	2	$\sqrt{2}$	$\sqrt{2}$

Table 2 Comparison between half-wave, centre-tap and bridge rectifiers

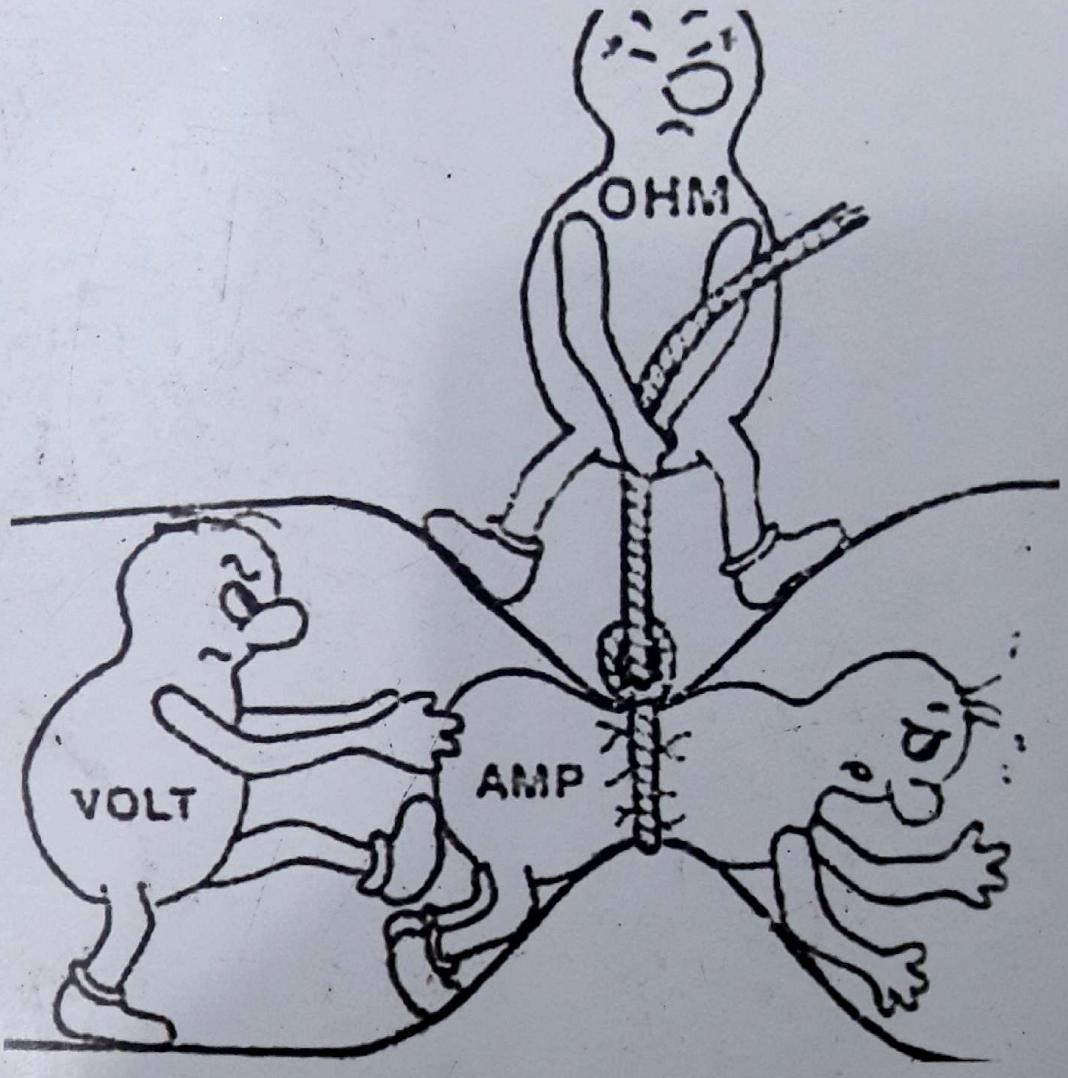
Parameter	Ideal	Real
Voltage gain	Infinite	100,000
Input resistance	Infinite	100 MΩ
Output resistance	Zero	20 Ω
Bandwidth	Infinite	2 MHz
Slew rate	Infinite	10 V/μs
Input offset voltage	Zero	Less than 5 mV

Table 3 Comparison of operational amplifier parameters for ideal and real devices

	Designation	Frequency range
ELF	Extremely low frequency	30 – 300 Hz
VF	Voice frequency	300 – 3000 Hz
VLF	Very low frequency	3 – 30 KHz
LF	Low frequency	30 – 300 KHz
MF	Medium frequency	300 – 3000 KHz
HF	High frequency	3 – 30 MHz
VHF	Very high frequency	30 – 300 MHz
UHF	Ultra-high frequency	300 – 3000 MHz
SHF	Super-high frequency	3 – 30 GHz
EHF	Extremely high frequency	30 – 300 GHz

Table 4 ITU frequency bands

Insights



SYSTEM INCEPTION

290/-

9 789937 282529

Price Rs 350/-