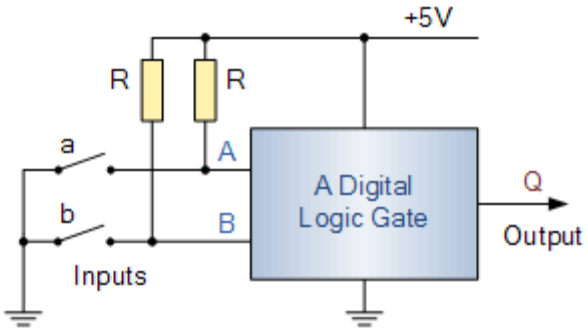
PULL UP AND PULL DOWN RESISTORS

What do they do?

Let's say you have an MCU with one pin configured as an input. If there is nothing connected to the pin and your program reads the state of the pin, will it be high (pulled to VCC) or low (pulled to ground)? It is difficult to tell. This phenomenon is referred to as *floating*. To prevent this unknown state, a pull-up or pull-down resistor will ensure that the pin is in either a high or low state, while also using a low amount of current.

Pull-up Resistors Application

Pull-up resistors are very common when using microcontrollers (MCUs) or any digital logic device



By using these two pull-up resistors, one for each input, when switch "A" or "B" is open (off), the input is effectively connected to the +5V supply rail via the pull-up resistor. The result is that as there is very little input current into the input of the logic gate, very little voltage is dropped across the pull-up resistor so nearly all the +5V supply voltage is applied to the input pin creating a HIGH, logic "1" condition.

When switches "A", or "B" are closed, (off) the input is shorted to ground (low) creating a logic "0" condition as before at the input. However, this time we are not shorting out the supply rail as the pull-up resistor only passes a small current (as determined by Ohms law) through the closed switch to ground.

By using a *pull-up resistor* in this way, the input always has a default logic state, either "1" or "0", high or low, depending on the position of the switch, thus achieving the proper output function of the gate at "Q" and therefore preventing the input from floating about or self-biasing giving us exactly the switching condition we require.

Calculating Pull-up Resistor Value

All digital logic gates, circuits and micro-controllers are limited not only by their operating voltage, but in the current sinking and sourcing ability of each input pin. Digital logic circuits operate using two binary states which are normally represented by two distinct voltages: a high voltage V_H for logic "1" and low voltage V_L for logic "0". But within each of these two voltage states, there is a range of voltages which define the upper and lower voltages of these two binary states.

So for example, for the TTL 74LSxxx series of digital logic gates, the voltage ranges representing a logic level "1" and a logic level "0" are shown.

Where: $V_{IH(min)}$ = 2.0V is the minimum input voltage guaranteed to be recognized as a logic "1" (high) input and $V_{IL(max)}$ = 0.8V is the maximum input voltage guaranteed to be recognized as a logic "0" (low) input.

When the input of the logic gate is HIGH, current flows into the TTL input as the input acts basically as a path connected directly to ground. This input current, $I_{IH(max)}$ is positive in value as it flows "into" the gate and for most TTL 74LSxxx inputs have a value of 20µA.

Likewise, when the input of the logic gate is LOW, the current flows out of the TTL input as the input acts basically as a path connected directly to Vcc. This input current, $I_{IL(max)}$ is negative in value as it flows "out-of" the gate and for most TTL 74LSxxx inputs, has a value of -400uA, (-0.4mA).

Note that the values of HIGH and LOW voltages and currents differ between TTL logic families and are also much, much lower for CMOS logic families. Also the input voltage and current requirements for micro-controllers, PIC, Arduino, Raspberry Pie, etc will also be different so please consult their data sheets first.

Pull-up Resistor Example

Two TTL 74LS00 NAND Gates along with a single-pole double-throw switch are to be used to make a simple Set-Rest bistable flip-flop. Calculate: 1). The maximum pull-up resistor values if the voltage representing a logic HIGH input is to be held at 4.5 volts when the switch is open, and 2). The current flowing through the resistor when the switch is closed (assume zero contact resistance). Also draw the circuit.

Data given: Vcc = 5V, V_{IH} = 4.5V, and $I_{IH(max)}$ = 20uA

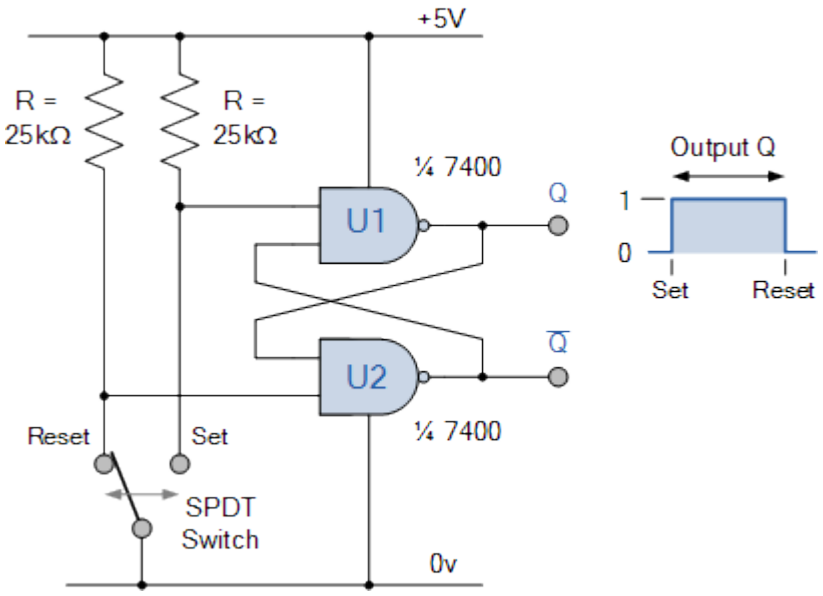
1). Pull-up Resistor value, R_{MAX}

$$R_{MAX} = \frac{V_{CC} - V_{IH}}{I_{IH}} = \frac{5 - 4.5}{20 \times 10^{-6}} = 25K\Omega$$

2). Resistor Current, I_R

$$I_R = \frac{V_{CC}}{R} = \frac{5V}{25k\Omega} = 200\mu A \text{ or } 0.2mA$$

Set-Reset Bistable Circuit



Pull-down Resistors

A *Pull-down resistor* works in the same way as the previous pull-up resistor, except this time the logic gates input is tied to ground, logic level "0" (low) or it may go HIGH by the operation of a mechanical switch. This pull-down resistor configuration is particularly useful for digital circuits like latches, counters and flip-flops that require a positive one-shot trigger when a switch is momentarily closed to cause a state change.

While they may seem to operate in the same way as the pull-up resistor, the resistive value of a passive pull-down resistor is more critical with TTL logic gates than with similar CMOS gates. This is because a TTL input sources much more current out of its input in its LOW state.

From above we saw that the maximum voltage level that represents a logic "0" (low) for a TTL 74LSxxx series logic gate is between 0 and 0.8 volts, ($V_{IL(MAX)}$ = 0.8V). Also when LOW, the gate sources current to the value of 400uA, (I_{IL} = 400uA). The maximum pull-down resistor value for a single TTL logic gate is therefore calculated as:

Single Gate Pull-down Resistor Value

$$R_{MAX} = \frac{V_{IL(MAX)} - 0}{I_{IL}} = \frac{0.8 - 0}{400 \times 10^{-6}} = 2K\Omega$$

Then the maximum pull-down resistor value is calculated as 2kΩ's. Again, as with the pull-up resistor calculations, this 2kΩ's resistor value leaves no room for error as the voltage drop is at maximum. So if

the resistance is too large, the voltage drop across the pull-down resistor may result in a gate input voltage beyond the normal LOW voltage range, so to ensure correct switching it is better to have an input voltage of 0.5 volts or less.

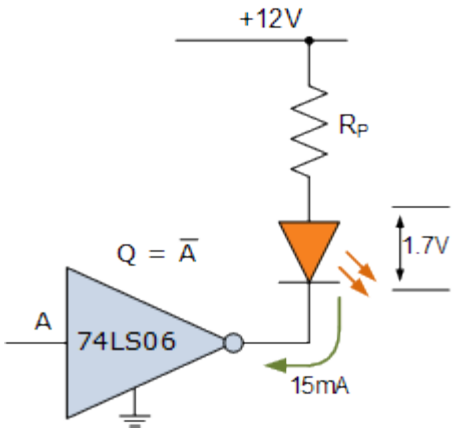
Therefore if we assume a voltage drop of only 0.4 volts across the resistor, a quick calculation would give us a single pull-down resistor value of 1kΩ's. Reducing the resistive value further, will produce a smaller voltage drop tying the input further to ground (low). This datasheet value of 400uA or 0.4mA (I_{IL}) is the minimum LOW current value but it may be higher.

Also, connecting inputs together will result in a larger current through the resistor. For example, a fan-in of 10 will result in 10 x 400uA = 4.0mA requiring a pull-down resistance of 100Ω's.

But why use a pull-down resistor at all when a direct connection to ground (0V) would produce the required LOW?. A direct connection to ground without the pull-down resistor would certainly work in most cases, but as the gates input is permanently tied to ground, the use of a resistor limits the current flowing out of the input thereby reducing power loss while still maintaining a logic "0" condition.

Pull-up Resistor Example No2

A 74LS06 Hex Inverter Driver is required to control a single red LED indicator from a 12 volt supply. If the LED requires 15mA at 1.7V voltage drop and the V_{OL} of the HEX Inverter when fully ON is 0.1 volts, calculate the value of the current limiting resistor required to drive the LED.



$$R_P = \frac{V}{I} = \frac{V_{CC} - V_{LED} - V_{OL}}{I_{LED}}$$

$$R_P = \frac{12 - 1.7 - 0.1}{15 \times 10^{-3}} = 680\Omega$$

We can use open-collector drivers in a similar way to drive small electromechanical relays, lamps or dc motors as these devices typically require 5V or 12V or more, at a current of about 10 to 20 mA's to operate correctly.

Two or more open-collector outputs of TTL gates can be directly connected together and tied through a single external pull-up resistor. The result is that the outputs are effectively AND'ed together as the combination behaves as if the gates were connected to an AND gate. This type of configuration is called wired AND logic.