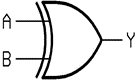
**LAB#2**

**Objective:**

Introduction to Flip-Flops & Latching.

**Task1:**

To design XOR gate in verilog by using Gate Level Modeling.

**Circuit diagram:**

**CODING:**

//Design Module

module gate(c,a,b);

input a,b;

output c;

xor x1(c,a,b);

endmodule

//Stimulux Module

module aazib;

reg a,b;

wire c;

gate xs1(c,a,b);

initial

begin

a=1'b0; b=1'b0;

#20

a=1'b0; b=1'b1;

#20

a=1'b1; b=1'b0;

#20

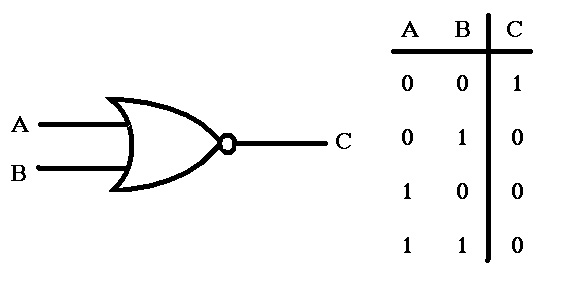
a=1'b1; b=1'b1;

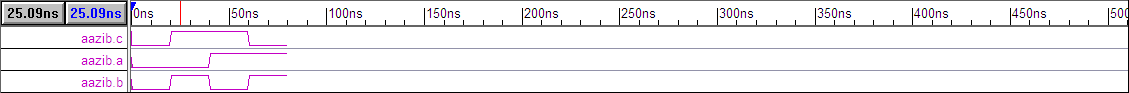
#20

$finish;

end

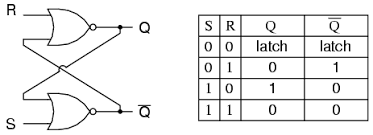
endmodule

**Truth Table:**

**Results (Timing diagram) :**

**TASK2:**

To design RS latch using NOR gate by using Gate Level Modeling.

**Circuit diagram:**

**CODING:**

//Design Module

module rs(q,qb,r,s);

input r,s;

output q,qb;

nor n1(q,r,qb);

nor n2(qb,s,q);

endmodule

//Stimulux Module

module aazib;

reg r,s;

wire q,qb;

rs rs1(q,qb,r,s);

initial

begin

r=1'b1; s=1'b1;

#30

r=1'b0; s=1'b1;

#30

r=1'b1; s=1'b0;

#30

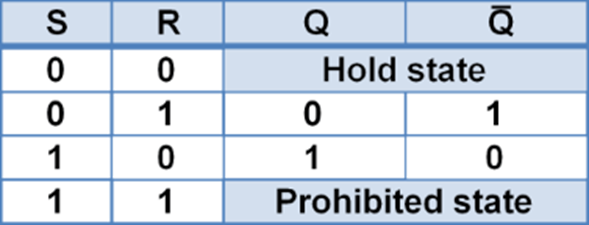
r=1'b0; s=1'b0;

#30

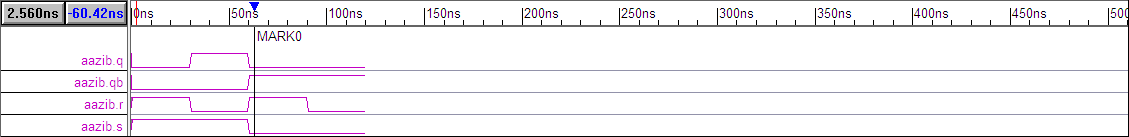
$finish;

end

endmodule

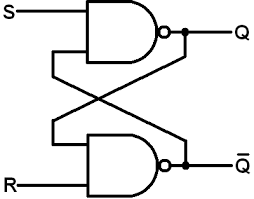
**Truth Table:**

**Results (Timing diagram) :**



**TASK3:**

To design SR latch using NAND gate by using Gate Level Modeling.

**Circuit diagram:**

**CODING:**

//Design Module

module rs(q,qb,s,r);

input s,r;

output q,qb;

nand n1(q,s,qb);

nand n2(qb,r,q);

endmodule

//Stimulux Module

module aazib;

reg s,r;

wire q,qb;

rs rs1(q,qb,s,r);

initial

begin

r=1'b0; s=1'b0;

#30

r=1'b0; s=1'b1;

#30

r=1'b1; s=1'b0;

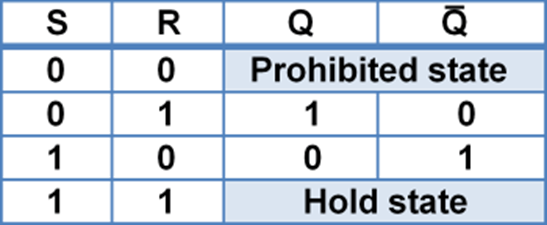
#30

$finish;

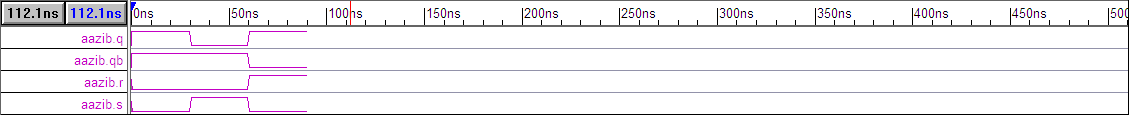
end

endmodule

**Truth Table:**

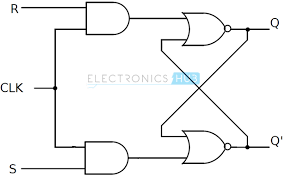
****

**Results (Timing diagram) :**



**TASK4:**

To design RS FlipFlop using AND & NOR gate by using Gate Level Modeling.

**Circuit diagram:**

**CODING:**

//Design Module

module rsff(q,qb,r,s,clk);

input r,s,clk;

output q,qb;

wire a,b;

and a1(a,r,clk);

and a2(b,s,clk);

nor n1(q,a,qb);

nor n2(qb,b,q);

endmodule

//Stimulux Module

module aazib;

reg r,s,clk;

wire q,qb;

rsff rs1(q,qb,r,s,clk);

initial

clk=1'b1;

always

#5clk=~clk;

initial

begin

r=1'b0; s=1'b1;

#30

r=1'b1; s=1'b0;

#30

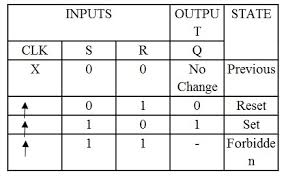
r=1'b0; s=1'b0;

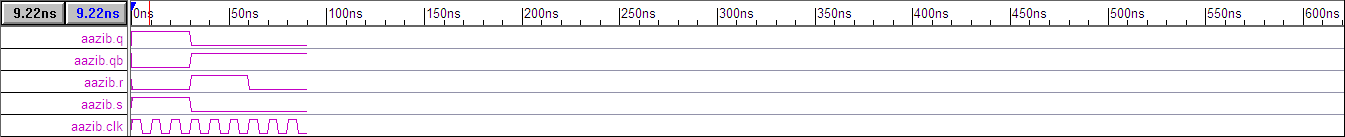
#30

$finish;

end

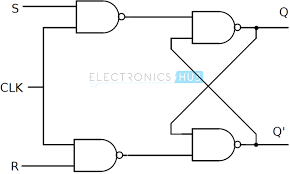
endmodule

**Truth Table:**

**Results (Timing diagram):**

**TASK5:**

To design SR flipflop using NAND gate by using Gate Level Modeling.

**Circuit diagram:**

**CODING:**

//Design Module

module rsff(q,qb,s,r,clk);

input s,r,clk;

output q,qb;

wire a,b;

nand a1(a,s,clk);

nand a2(b,r,clk);

nand n1(q,a,qb);

nand n2(qb,b,q);

endmodule

//Stimulux Module

module aazib;

reg s,r,clk;

wire q,qb;

rsff rs1(q,qb,s,r,clk);

initial

clk=1'b1;

always

#5clk=~clk;

initial

begin

s=1'b0; r=1'b1;

#30

s=1'b1; r=1'b0;

#30

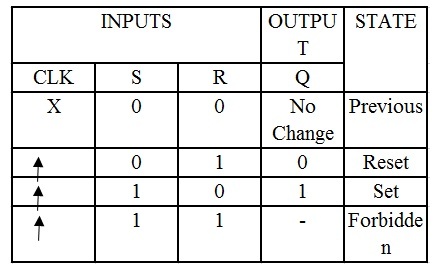
s=1'b0; r=1'b0;

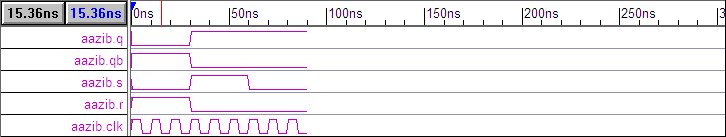
#30

$finish;

end

endmodule

**Truth Table:**

**Results (Timing diagram):**