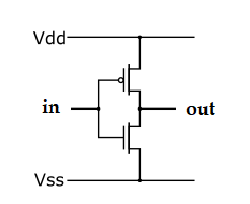
**LAB # 08**

**Objective:** INTRODUCTION TO SWITCH LEVEL MODELING.

**Task1:** TO design NOT, NAND, AND, OR gate in verilog by using Switch Level Modeling.

**For NOT Gate**

**CMOS Circuit:**

**Coding:**

//Design Module

module notgate(out,in);

input in;

output out;

supply1 vdd;

supply0 gnd;

pmos p1(out,vdd,in);

nmos n1(out,gnd,in);

endmodule

//Stimullux Module

module aazib;

reg in;

wire out;

notgate g1(out,in);

initial

begin

in=1'b0;

#20

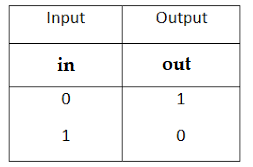
in=1'b1;

#20

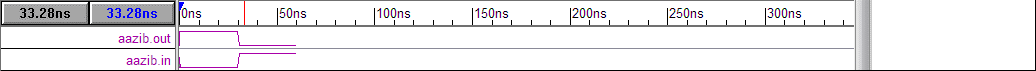
$finish;

end

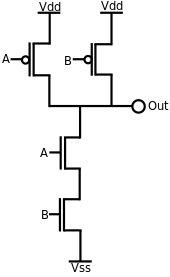
endmodule

**Truth Table:**

**Results (Timing diagram) :**



**For NAND Gate**

**CMOS Circuit:**

**Coding:**

//Design Module

module nandgate(out,a,b);

input a,b;

output out;

wire x;

supply1 vdd;

supply0 gnd;

pmos p1(out,vdd,a);

pmos p2(out,vdd,b);

nmos n1(out,x,b);

nmos n1(x,gnd,a);

endmodule

//Stimullux Module

module aazib;

reg a,b;

wire out;

nandgate g1(out,a,b);

initial

begin

a=1'b0; b=1'b0;

#20

a=1'b1; b=1'b0;

#20

a=1'b0; b=1'b1;

#20

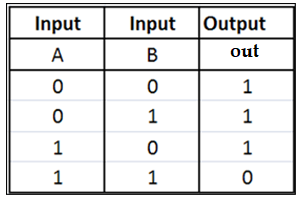
a=1'b1; b=1'b1;

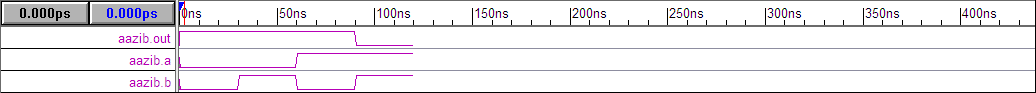
#20

$finish;

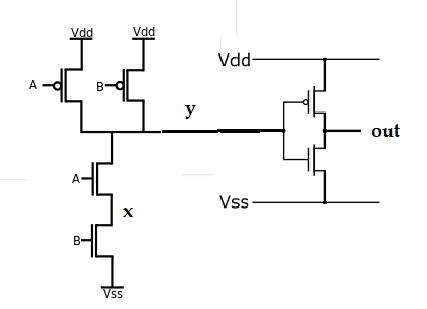
end

endmodule

**Truth Table:**

**Results (Timing diagram) :**

**For AND Gate**

**CMOS Circuit:**

**Coding:**

//Design Module

module andgate(out,a,b);

input a,b;

output out;

wire x,y;

supply1 vdd;

supply0 gnd;

pmos p1(y,vdd,a);

pmos p2(y,vdd,b);

pmos p3(out,vdd,y);

nmos n1(y,x,b);

nmos n2(x,gnd,a);

nmos n3(out,gnd,y);

endmodule

//Stimullux Module

module aazib;

reg a,b;

wire out;

andgate g1(out,a,b);

initial

begin

a=1'b0; b=1'b0;

#20

a=1'b1; b=1'b0;

#20

a=1'b0; b=1'b1;

#20

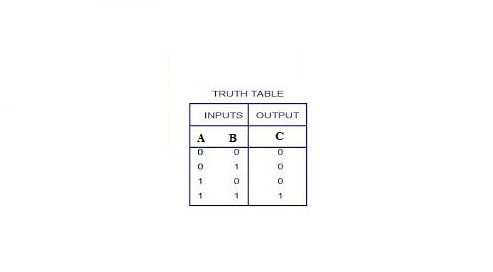
a=1'b1; b=1'b1;

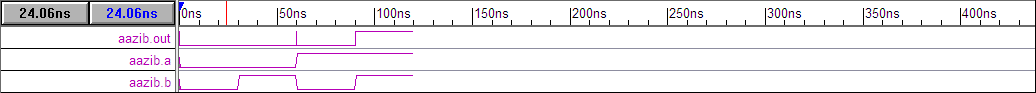
#20

$finish;

end

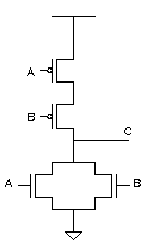
endmodule

**Truth Table:**

**Results (Timing diagram) :**

**For NOR Gate**

**CMOS Circuit:**

****

**Coding:**

//Design Module

module norgate(out,a,b);

input a,b;

output out;

wire x;

supply1 vdd;

supply0 gnd;

pmos p1(x,vdd,a);

pmos p2(out,x,b);

nmos n1(out,gnd,a);

nmos n2(out,gnd,b);

endmodule

//Stimullux Module

module aazib;

reg a,b;

wire out;

norgate g1(out,a,b);

initial

begin

a=1'b0; b=1'b0;

#20

a=1'b1; b=1'b0;

#20

a=1'b0; b=1'b1;

#20

a=1'b1; b=1'b1;

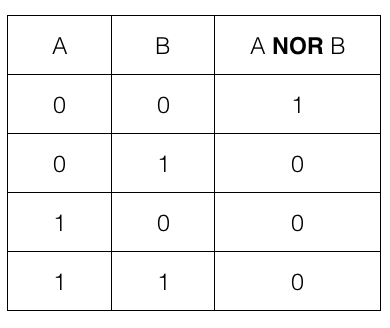
#20

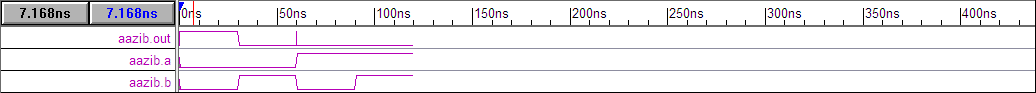
$finish;

end

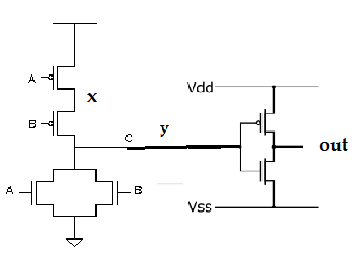
endmodule

**Truth Table:**



**Results (Timing diagram) :**

**For OR Gate**

** CMOS Circuit:**

**Coding:**

//Design Module

module orgate(out,a,b);

input a,b;

output out;

wire x,y;

supply1 vdd;

supply0 gnd;

pmos p1(x,vdd,a);

pmos p2(y,x,b);

pmos p3(out,vdd,y);

nmos n1(y,gnd,a);

nmos n2(y,gnd,b);

nmos n3(out,gnd,y);

endmodule

//Stimullux Module

module aazib;

reg a,b;

wire out;

orgate g1(out,a,b);

initial

begin

a=1'b0; b=1'b0;

#20

a=1'b1; b=1'b0;

#20

a=1'b0; b=1'b1;

#20

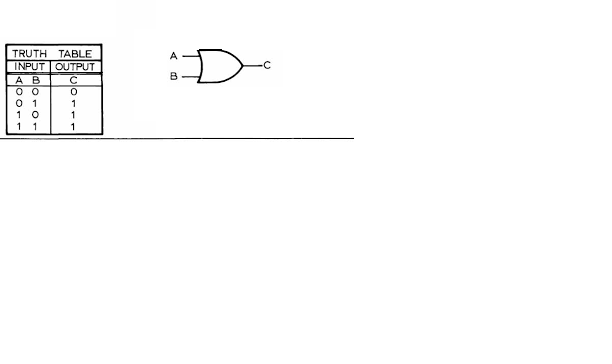
a=1'b1; b=1'b1;

#20

$finish;

end

endmodule

**Truth Table:**

**Results (Timing diagram) :**

