**LAB # 09**

**Objective:** Designing ckt diagrams of experessions & observe result by using Switch Level Modeling.

1. **Out =**

**Coding:**

//Design Module

module exp1(out,a,b,c);

input a,b,c;

output out;

wire x,y;

supply1 vdd;

supply0 gnd;

pmos p1(x,vdd,a);

pmos p2(out,x,b);

pmos p3(out,vdd,c);

nmos n1(out,y,a);

nmos n2(out,y,b);

nmos n3(y,gnd,c);

endmodule

//Stimullux Module

module aazib;

reg a,b,c;

wire out;

exp1 g1(out,a,b,c);

initial

begin

a=1'b0; b=1'b0; c=1'b0;

#20

a=1'b1; b=1'b0; c=1'b0;

#20

a=1'b0; b=1'b1; c=1'b0;

#20

a=1'b1; b=1'b1; c=1'b1;

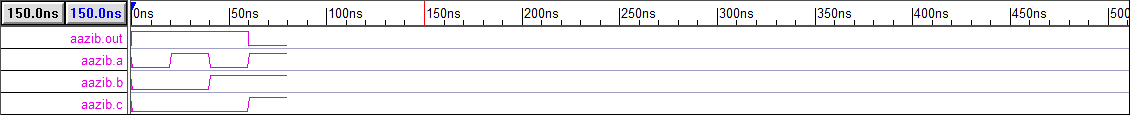
#20

$finish;

end

endmodule

**Results (Timing diagram) :**



**Coding:**

//Design Module

module exp2(out,a,b,c);

input a,b,c;

output out;

wire x,y;

supply1 vdd;

supply0 gnd;

pmos p1(x,vdd,c);

pmos p2(out,x,a);

pmos p3(out,x,b);

nmos n1(out,y,a);

nmos n2(y,gnd,b);

nmos n3(out,gnd,c);

endmodule

//Stimullux Module

module aazib;

reg a,b,c;

wire out;

exp2 g1(out,a,b,c);

initial

begin

a=1'b0; b=1'b0; c=1'b0;

#20

a=1'b1; b=1'b0; c=1'b0;

#20

a=1'b0; b=1'b1; c=1'b0;

#20

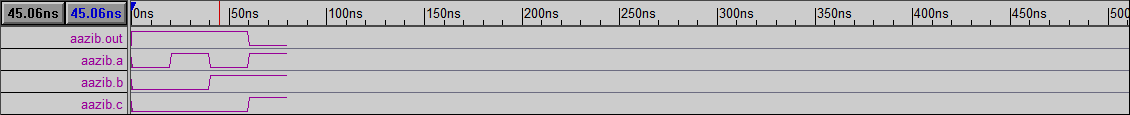
a=1'b1; b=1'b1; c=1'b1;

#20

$finish;

end

endmodule

**Results (Timing diagram):** 

**c)**

**Coding:**

//Design Module

module exp3(out,a,b,c,d);

input a,b,c,d;

output out;

wire x,y,z;

supply1 vdd;

supply0 gnd;

pmos p1(x,vdd,a);

pmos p2(out,x,b);

pmos p3(y,vdd,c);

pmos p4(out,y,d);

nmos n1(out,z,a);

nmos n2(out,z,b);

nmos n3(z,gnd,c);

nmos n4(z,gnd,d);

endmodule

//Stimullux Module

module aazib;

reg a,b,c,d;

wire out;

exp3 g1(out,a,b,c,d);

initial

begin

a=1'b0; b=1'b0; c=1'b0; d=1'b0;

#20

a=1'b1; b=1'b0; c=1'b0; d=1'b1;

#20

a=1'b0; b=1'b1; c=1'b0; d=1'b1;

#20

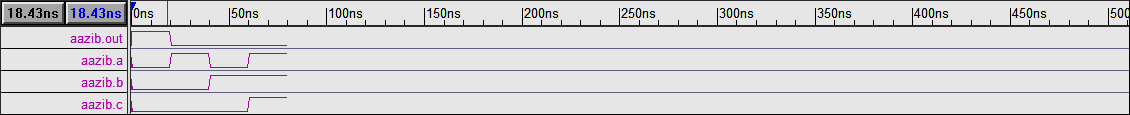
a=1'b1; b=1'b1; c=1'b1; d=1'b1;

#20

$finish;

end

endmodule

**Results (Timing diagram):**

**Coding:**

//Design Module

module exp4(out,a,b);

input a,b;

output out;

wire x,y,z,w;

supply1 vdd;

supply0 gnd;

pmos p1(x,vdd,a);

pmos p2(out,x,b);

pmos p3(y,vdd,a);

pmos p4(out,y,b);

nmos n1(out,z,a);

nmos n2(z,gnd,b);

nmos n3(out,w,a);

nmos n4(w,gnd,b);

endmodule

//Stimullux Module

module aazib;

reg a,b;

wire out;

exp4 g1(out,a,b);

initial

begin

a=1'b0; b=1'b0;

#20

a=1'b1; b=1'b0;

#20

a=1'b0; b=1'b1;

#20

a=1'b1; b=1'b1;

#20

$finish;

end

endmodule

**Results (Timing diagram):**

