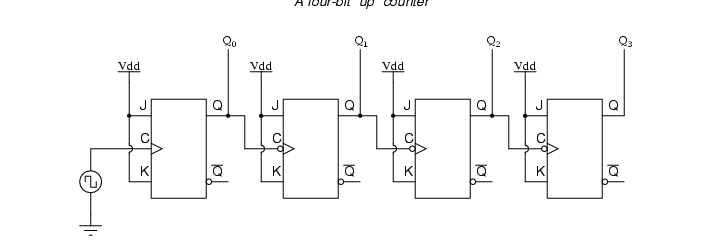
**LAB#14 Open-Ended LAB**

**Title: Design Asynchronous counter in verilog by using Xilinx ISE.**

1. **Objective:** Introduction to xilinx.

**Task1:** To Asynchronous counterin verilog by using Xilinx ISE.

1. **Hardware/Software required:** Xilinx and MS word
2. **Block Diagram:**

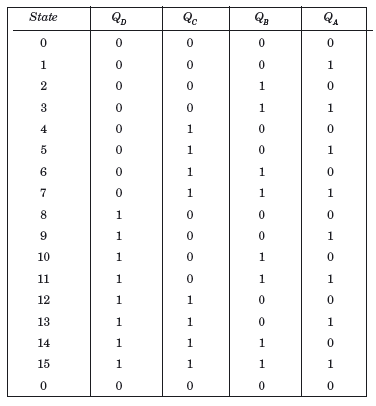
****

1. **Methodology:**

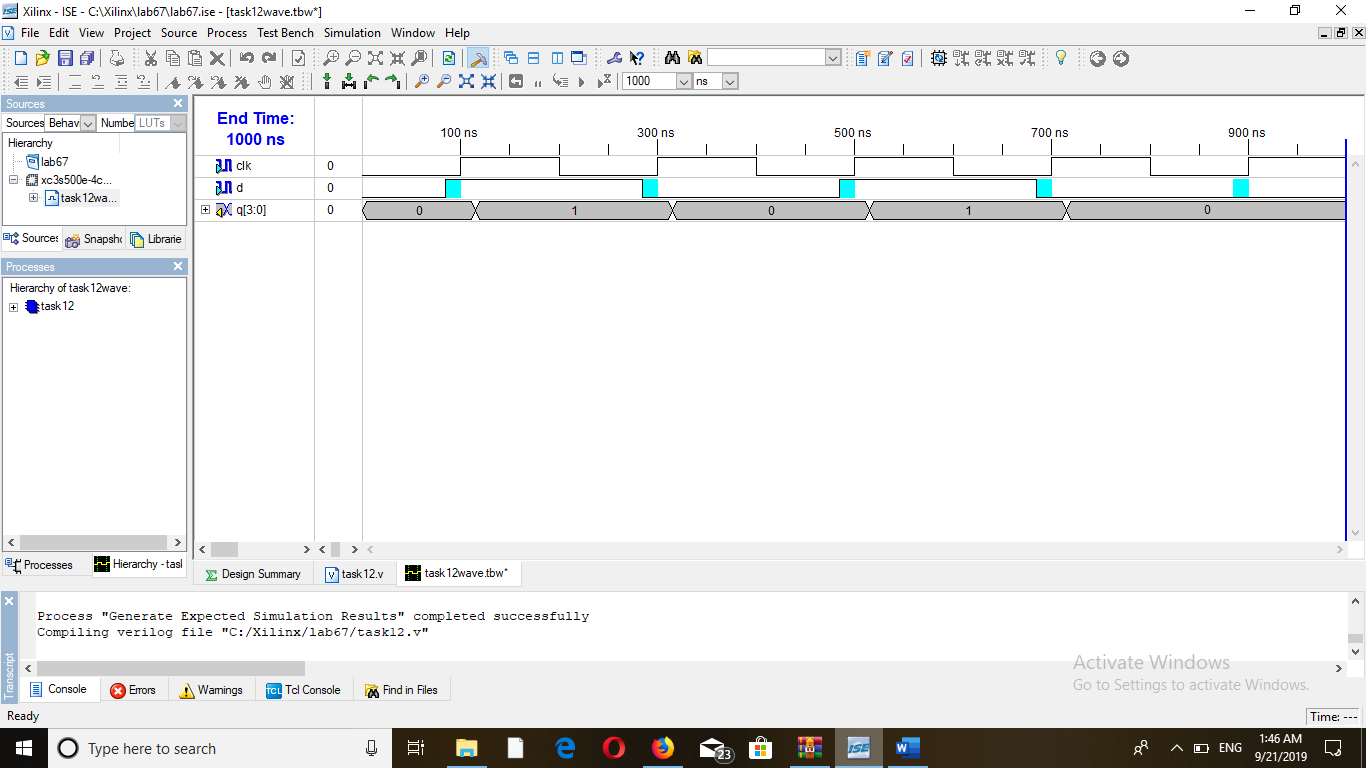
//Design Module

module dff(d,clk,q);  
input d;  
input clk;  
wire d;  
wire clk;  
output q;  
reg q;  
initial  
q = 1'b0;  
always @(posedge clk)begin  
q <= d;  
end  
endmodule  
//stimulux module  
module FOURbit\_up\_B();  
reg clk;  
reg d;  
wire [3:0]q;  
initial  
clk = 0;  
always   
#1 clk = !clk;  
dff a1(!q[0],clk,q[0]);  
dff a2(!q[1],q[0],q[1]);  
dff a3(!q[2],q[1],q[2]);  
dff a4(!q[3],q[2],q[3]);  
endmodule

1. **Observation:**

** Truth Table:**

1. **Results and Discussions:**

**Timming Diagram:**

1. **Conclusion:**

In this task I have made an Asynchronous counter by using Xilinx software through verlog code. The following timming diagram is obtained through this code which verifies the working of Asynchronous counter.