

## **Milestone 1 Journal:**

Sunday, Jan 12th:

This meeting we sat and brainstormed the basic format of our instructions and registers. We talked about how to deal with the single working register and work around it using some essential registers we would need. By the end of this meeting we had the basic instructions and registers down.

Monday, Jan 14th:

This meeting was centered around memory. With only one register to work out of, we sat and talked about how to optimise our instructions to meet this new memory model we were working out of.

Tuesday, Jan 15:

This meeting was dedicated to the assembly implementation. We redesigned some of the instructions to meet our assembly language specs and proceeded to convert it to machine code.

## **Milestone 2 Journal:**

Friday, Jan 17th:

Fixed some issues with the milestone 1 document. Added a memory map, cover page and so on.

Sunday, Jan 19th:

Worked on the RTL.

Monday, Jan 20th:

Finished the rest of M2. Added a shopping list of required hardware and a summary of RTL symbols.

Wednesday, Jan 22nd:

Finished the design document and polished it for submission. Also submitted.

### **Milestone 3 Journal:**

Sunday, Jan 26th:

On this meeting the goal was to fix the errors from Milestone 2. We updated the control signals and made changes to the RTL as specified in the design document. Once this was finished, we made a picture of the datapath to the specifications of the RTL.

Monday, Jan 27th:

On this meeting we looked at each unit of the datapath and worked on a comprehensive description for each component. We finalised the control bits and worked defining a method to test the units. We came to the conclusion that an exhaustive method would be too long and a few edge test cases would suffice.

Tuesday, Jan 28th:

Here we designed most of the test branches for our unit modules. After completing this we moved on to working on the labs in order to get some working parts.

Wednesday, Jan 29th:

In this meeting we finalised everything and mashed it all into one project. This meeting was focused on compiling all our work together and submission.

### **Milestone 4 Journal:**

Sunday, Feb 2nd:

In this meeting we reviewed our datapath and fixed some of the issues we had with clocking using control bits. We removed the Wailing wall and started taking a closer look at the controller

Monday, Feb 3rd:

In this meeting we looked at each instruction and made the state diagram. We also finished the assembler and test cases or integration plans.

Tuesday, Feb 4th:

This meeting we finished up the document and added some descriptions. All files were uploaded to the git.

### **Milestone 5 Journal:**

*Monday, Feb 10th: [4 hrs]:*

In this meeting we finished the controller, controller testing and took a look at the integration phases. We then set about to finish implementing phase 1 and phase 2 on our integration plan, making sure to fit the test cases as we completed them.

*Tuesday, Feb 11th: [4 hrs]:*

By the start of this meeting we had integration phase 1 and controller fully done and tested. This meeting was about finishing phase 2 and redefining the integration plan for phase 3 and 4 (As detailed in the design process journal). We then set tasks to finish up phase 3 and finalise the design journals.

*Wednesday, Feb 12th: [30 mins]:*

This meeting was dedicated to finalising and finishing up our respective test cases and individual journal.

### **Milestone 6 Journal:**

This milestone was geared towards finishing the processor and getting the relprime code to work. Therefore, it was a more individually done milestone. I spent most of the time on Monday and Tuesday debugging the relprime code and making sure it output the right answer.