Joshua Giambattista, WORK LOG

Milestone 1 Work:

Sunday, January 12, 2020 [3 hours]

Started design on the instruction set and listed out our eight registers. Listed out all of the instructions that we felt would be useful for the relprime program and just for general use. Started talking about how the syntax for each instruction and how they would work with memory and each register. Finished the instruction set for the R-type and IJ types.

Monday, January 13,2020 [2.5 hours]

We decided how our call convention would want to work and continued modifying the instructions to work more smoothly. Spent a lot of time figuring out how to best access memory with our design and we decided that the memory address register will hold the address of a place in memory that we want to access. But if we choose to do an instruction with the memory address register, it will first get the value out of memory. Except for the command addm so that we can still access arrays and such.

Tuesday, January 14, 2020 [3.5 hours]

Wrote the relprime code and fragments. Finalized the instruction syntax to be able to fit everything that was required. We also wrote out the binary for the relprime and the code fragments. We cleaned up all of the documentation and made sure everything was up to date.

Assigned Tasks for Milestone 2

My task for milestone 2 is to work with Abi and work on the RTL for each instruction and communicate with Michelle and Darren who will be working on the control bits so that we know what the names of all of our bits will be.

Milestone 2 Work:

Friday, January 17, 2020 [1 hour]

As a group, we went through the items that Dr. Williamson gave us to fix from M1 and made the necessary changes in our design document. Specifically, we added a memory map, reordered the description of instructions, and added in 2 more examples of our code.

Sunday, January 19, 2020 [2.5 hours]

We finished up the items for M1 and started on RTL. To do this, we drew a crude datapath for our machine as we looked at each instruction to make sure that our RTL made sense. Then, since we are doing a multi-cycle/pipelined machine, we tried to turn all of the RTL into a big table.

Monday, January 20, 2020 [2 hours]

We finalized all of our RTL and made a list of the required parts that we need for the processor. Then, we made a list of all of our input, output, control, and RTL symbols with how many bits each signal is.

Milestone 3 Work:

Sunday, January 26, 2020 [3 hours]

On Sunday we fixed the items on milestone 2 that we were told to change, including updated versions of the control signals and RTL symbols. Then, we spent the rest of the time drawing out the datapath to fit our instruction set and RTL. We also spent time double checking our datapath with the RTL to make sure everything made sense.

Monday, January 27, 2020 [2 hours]

We worked on the descriptions for each component in the datapath and defined each control signal and how it works. Then we started figuring out how we wanted to test our components. We decided that doing exhaustive testing with a few edge cases would most likely be the best way to go.

Tuesday, January 28, 2020 [2.5 hours]

We designed most of the testbenches for our components in Verilog. We designed all of the mux, ALU, adder, Memory, and Register File testbenches. Then, we tried to finish some of the labs so that we could get started on implementing our design as soon as possible.

Milestone 4 Work:

Sunday, February 2, 2020 [2 hours]

On Sunday we looked over our datapath to try and figure out the issues that we had with clocking. We got rid of our wall of registers and added some more control bits to the datapath so that the clock would work correctly. Then we started trying to specify how to control would work. Since we are doing multi-cycle, we created the layout for our finite state machine.

Monday, February 3, 2020 [3 hours]

We spent most of this time going through every instruction and figuring out what control signals would be active during each clock cycle. We also got the assembler finished and specified all of the tests that are required for implementing sections of our datapath.

Tuesday, Febrary 4, 2020 [45 minutes]

Added some last minute descriptions that we needed for this milestone and made sure to upload all of our Verilog files to git.

Milestone 5 Work:

Monday, February 9, 2020 [4 hours]

On Monday we spent the whole time trying to test control and starting our integration plan. We decided to change the plan a little bit after we got phase 1 to work. Our old plan was to have a phase 3 that would test that phase 1 and 2 worked together, but we decided that was redundant. So, our new plan has four phases, one for each third of the processor with the last one being adding everything together.

Tuesday, February 10, 2020 [3 hours]

On Tuesday we finished phase 1, 2, and 3 of our integration testing with much success. The only files we had to fix were the registers and register file because it wasn't holding values for multiple clock cycles correctly. Otherwise, everything went smoothly.

Milestone 6 Work:

This Milestone was a lot more individual for us than the previous ones. I was on a bus for roughly 10 hours, so I finished the hardware of the processor over the weekend while the other three looked up stuff for the FPGA and modified our relprime program. Then on Monday and Tuesday we worked on debugging the software and hardware together with total success on Tuesday.