Darren Zhu, WORK LOG

MILESTONE 1 WORK:

Sunday, January 12, 2020

Met with the entire team [2 hr 50 mins]

- We spent the first two hours to brainstorm all the registers and instructions we need, also the instruction format types. The last 50 minutes was spent on typing up all the results of discussion into the design document.
- We have a one bit result location select for R-type instructions which indicates the location to save the data.
- My task for tonight is to write some Assembly language fragments for common operations [est. 20 mins]

Monday, January 13, 2020

Met with the entire team [2 hrs]

- We added more instructions and adjust some instructions today so that it would become easier to use. We have new instructions which can load the result into the memory address register or the working register directly.
- We used the three dead bits on the R-type instructions to indicate the target register to save or get the data.
- We finished the explanation of call conventions and the table of instruction sets today.

Tuesday, January 14, 2020

Met with the entire team [3 hrs]

- Abi guided us through the code for relPrime.
- We updated the shamt bits on the R-type instructions to a delta value. It will represent the number of register for some instructions like move. With this change, only one instruction is needed to move data from one register to another.
- We finished translating the small programs and relPrime into binary codes.
- We removed andi instruction since we need one more IJ-type instruction seqi.
- My task for milestone 2 is:
    - the list of signals with the number of bits for each.

MILESTONE 2 WORK:

Friday, January 17, 2020

Met with the entire team [50 mins]

- We managed to fix some issues identified in the Milestone 1 meeting like adding a memory map, showing a recursive small program, and adding a cover page. For the remaining tasks, we divided it.
- My task for tonight is to:
    - Cooperate with Joshua to add mathematical descriptions for instructions. [est. 30 mins]

Sunday, January 19, 2020

Met with the entire team [2 hr 30 mins]

- Working on M2:
    - Making the RTL Specification for individual instructions.

Monday, January 20, 2020

Met with the entire team [2 hrs]

- We updated and checked everything for M1 is properly fixed.
- We was working on the rest of M2:
    - Grouping individual RTL instructions into a summary table.
    - Listing all the components required for RTL implementation.

Wednesday, January 22, 2020

Fix errors in the RTL individually, update the summary table for RTL [1 hr]

> The last step in the RTL for some instructions should be Reg[IR[5:7]] = ALUOut. We mistakenly set them as A = ALUOut which is totally wrong since we need those values to go back into the registers.

MILESTONE 3 WORK:

Sunday, January 26, 2020

Met with the entire team [3 hrs]

- We managed to fix some issues identified in the Milestone 2 meeting.
    - We updated the memory map so that the top address is 0xFFFF.
    - We divided the R-type instructions into R-type and D-type. Since the focus of R-type instructions is how to operate data from two selected registers while the D-type involves a delta value as immediate.
    - We updated the rest of file (instruction descriptions, opcode table, etc) since we changed the instruction types.
    - We updated the RTL specification since the first two cycles in each instruction should be the same. There are 5 cycles instead of 4 since the push and pop need an extra cycle to store the data.
- Joshua plotted out the Datapath diagram and guided us through the diagram with different instructions.
- I started to work on lab07 so that I will be able to learn how to test / control the memory.
- My task for tonight is to:
    - Continue work on lab 07 [est. 1 hr].

Monday, January 27, 2020

Met with the entire team [2 hrs]

- Working on M3:
    - We updated the list of components required for RTL implementation based on the new Datapath diagram.
    - We updated the list of Input signals, Output signals, and Control signals.
    - I was working on the descriptions of all control signal we have.

Tuesday, January 29, 2020

Met with the entire team [2 hrs]

- I was working on lab07 and managed to finish it.
- I identified one issue in the RTL table and fixed it. The last cycle for pop and push is misplaced.
- I was writing test code for memory.

MILESTONE 4 WORK:

Sunday, February 2, 2020

Met with the entire team [2 hrs]

- I updated opcode/funct table for D-type and R-type instructions. Now the R-type only use opcode 0 and the D-type only use opcode 1 to keep the control simple.
- I fixed the components needed for RTL implementation based on the revised design.
- Assigned tasks:
    - I will make the sign-extender and zero-extender, then test them individually. [est. 30 mins]
    - I will make the memory and test it as a component. [est. 45 mins].
    - I will make the diagram for control signals [est. 1 hr].

Monday, February 3, 2020

Met with the entire team [2 hr 30 mins]

- We have a new register IR which is only writable if the IRWrite is on. It preserves the instruction throughout all cycles for each instruction.
- I fixed the description for addi and subi instruction.
- I updated the RTL table since the wailing wall of registers is gone.
- I fixed the implementation of memory and tested it.
- I was updating the diagram for control signals.
- Task for me is to finish the diagram [est. 30 mins].

Tuesday, February 4, 2020

Met with the entire team [50 mins]

- I made the left shifter and tested it.
- I corrected the memory map, half of 0xFFFF should be 0x7FFF.
- Checking out everything for M4.

MILESTONE 5 WORK:

Monday, February 10, 2020

Met with the entire team [2.5 hrs]

- We first fixed some milestone 4 works, like the plan to implement the hardware and plan for unit test.
- I was working on integration test phase 2. I was testing the memory together with the extenders.

Continue working on Phase 2 integration test individually. [2.5 hrs]

- It took me a while to setup the data memory since we assume some data are already in the memory for the tests.
- Then I finished writing test cases for today.

Tuesday, February 11, 2020

Met with the entire team [2.5 hrs]

- I added more components (the register file, more muxes) to the phase 2 integration test. We identified a bug in the register file which was not identified before. Hence, we fixed the bug first.
- After connecting all the components for phase 2, I started to write some test cases.

Continue working on integration phase two individually. [1.5 hrs]

- I continued working on the test cases and finished them.
- I wrote test cases which can test:
    - From register file to memory
    - From memory to register file
    - From Instruction register to the MUX
    - Write memory with the data from register file
    - Write register file with the data from memory
    - Test sign-extend and zero-extend
    - Pass the immediate from the instruction register to sign and zero extenders

MILESTONE 6 WORK:

Thursday, February 13, 2020

I glue everything together in schematic. I managed to assemble the CPU but I cannot test it or run it due to some file path issues. [1.5 hrs]

Friday, February 14, 2020

I was debugging the file path issues, trying to replace all the parts with error messages. However, since we did not know how to change the file path for the memories on Friday, and some parts are done in schematic while the rests are done in Verilog, I cannot solve the file path issues. Then I met with Josh and sent all the parts to him. [1 hr]

Monday, February 17, 2020

Update the design document.

Met with Abi. [1.5 hrs]

Trying to get RelPrime to work on the CPU.

Wednesday, February 19, 2020

Finish the design document for M6. [30 mins]