



Design Process Journal

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Integration:

1. The first task is to combine 2 adders, a PC register, Shift Left, a PC Select MUX (4 inputs to one output) and an Instruction memory.
2. The next addition is to add the register file and Data memory. We connect these with a call MUX, three pop/push MUXs, location select MUX and the data write MUX.
3. The third step is to add the sign and zero extenders (connected with an Ext MUX) and a wall of 10 registers that will store each register, the immediate selected by the extenders and the data memory (The Wailing Wall).
4. The last edition is the main ALU which is attached to its two inputs using the ALUInput1 and ALUInput2 MUXs. Additionally, the second input to the ALU is also selected between the Zero Extended delta and the registers using a Delta MUX.

Affect That Architecture Had On Datapath:

1. Since our architecture was a multicycle implementation of the Accumulator, our datapath is built to be optimised towards the \$ma register we had.
2. One of the bigger design decisions was The Wailing Wall. As the controller doesn't finish until the third cycle, we forward all the registers to the next cycle. This doesn't impact efficiency as there are only eight registers and choosing between them doesn't take too long.

Changes to the Integration Plan (M4)

We do not have any update on the Integration Plan for M4.

Changes to the Integration Plan (M5)

- Phase 3 was changed to be the ALU and its various input parts.
- Phase 4 was changed to be the integration the phases 1, 2 and 3 with the control unit