Logic Design 2DI4
Lab #1
28th-September-2023

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Mustafa Shahid, shahim45, 400440384]**

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Milestone 1:

Q. Using the automatic measuring functions of the digital oscilloscope, state at what input voltage level the output of the NAND changes? Specifically, does the automatic measuring function match the HIGH-SPEED CMOS levels for LO and HI?

Answer:

According to the CMOS levels for LO and HI, the output must change at a voltage between 0.9V and 3.15V. The output of the NAND changes at 1.6 V Input from the wave generator. Yes the automatic measuring function does match the CMOS levels.

74HC00
74HC04
74HC10
74HC08

1.4.2 Building Circuits, Expressions, and Truth Tables

Milestone 2:

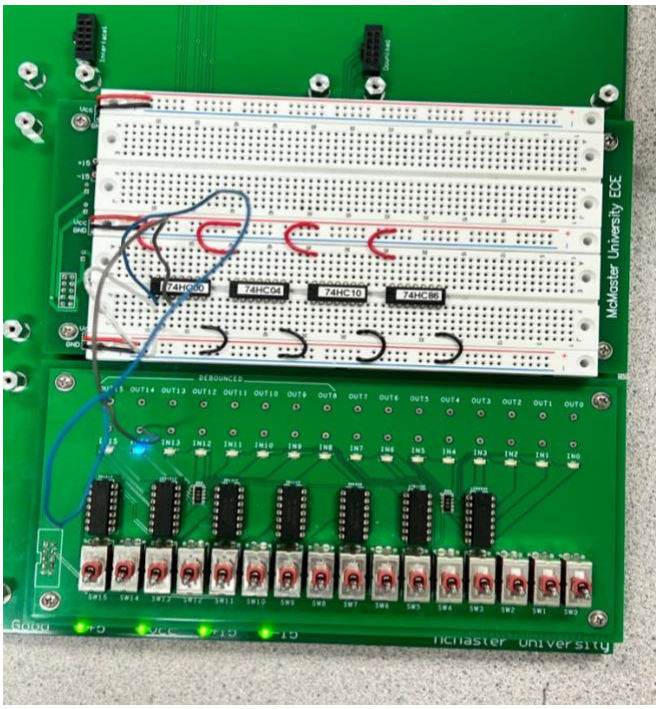
(a)

Figure 1.2: Logic Circuit 1

(i) Logic Function: F1 = (X.X)'

(ii) Truth Table (Circuit 1):

x	F_1
0	1
1	0



(b)

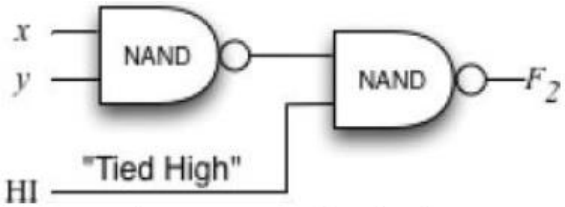
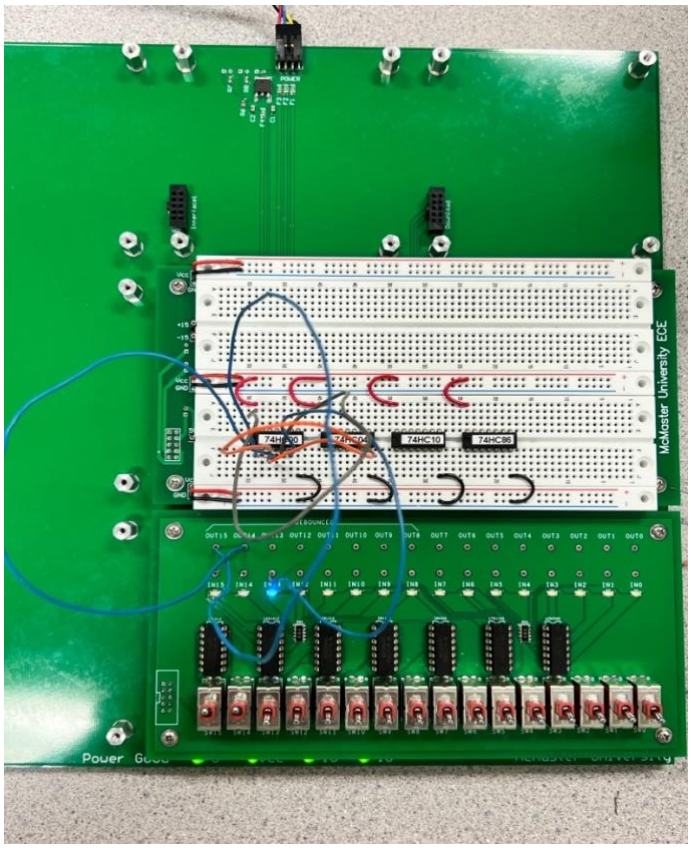


Figure 1.3: Logic Circuit 2

(i) Logical Function: ((XY)' 1)'

(ii) Truth Table (Circuit 2):

x	y	F_2
0	0	0
0	1	0
1	0	0
1	1	1



(c)

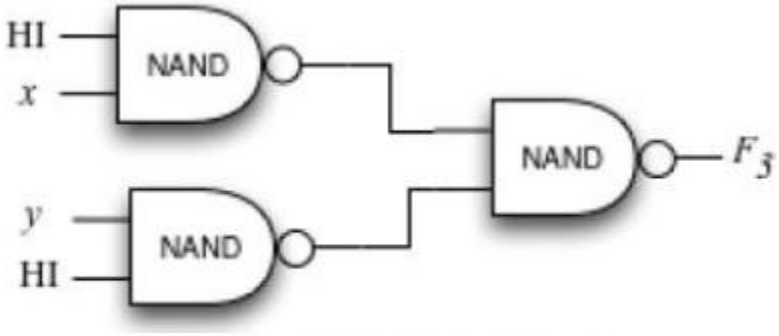
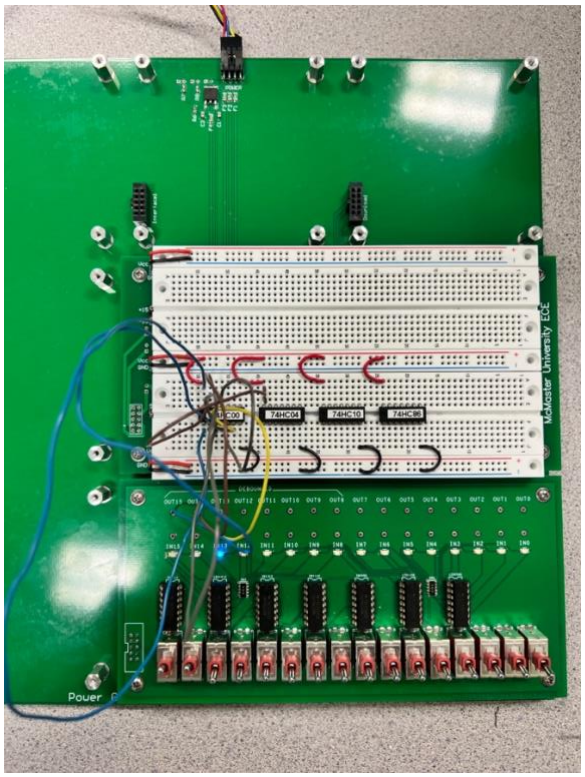


Figure 1.4: Logic Circuit 3

(i) Logical Function: ((X.1)'(Y.1)')'

(ii) Truth Table (Circuit 3):

x	y	F_3
0	0	0
0	1	1
1	0	1
1	1	1



(d)

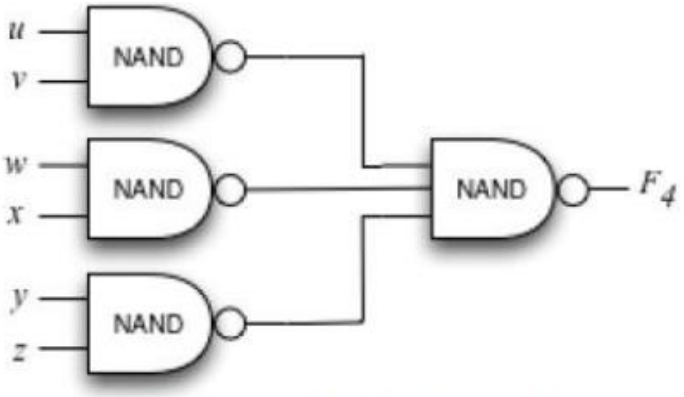


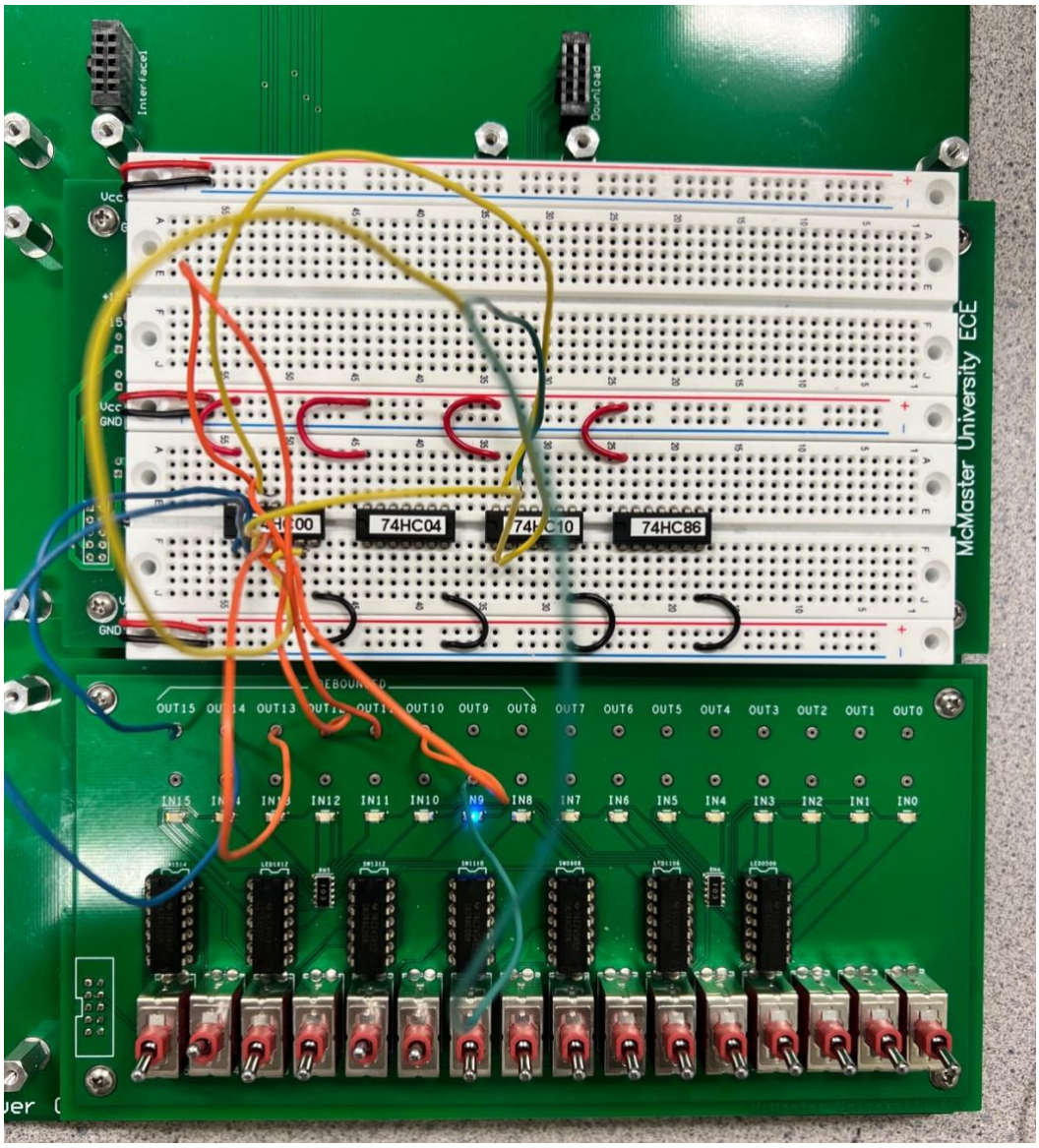
Figure 1.5: Logic Circuit 4

(i) Logic Function: ((UV)'(WX)'(YZ)')'

(ii) Truth Table (Circuit 4):

#	u	v	W	X	Y	Z	F_4
0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0
2	0	0	0	0	1	0	0
3	0	0	0	0	1	1	1
4	0	0	0	1	0	0	0
5	0	0	0	1	0	1	0
6	0	0	0	1	1	0	0
7	0	0	0	1	1	1	1
8	0	0	1	0	0	0	0
9	0	0	1	0	0	1	0
10	0	0	1	0	1	0	0
11	0	0	1	0	1	1	1
12	0	0	1	1	0	0	1
13	0	0	1	1	0	1	1
14	0	0	1	1	1	0	1
15	0	0	1	1	1	1	1
16	0	1	0	0	0	0	0
17	0	1	0	0	0	1	0
18	0	1	0	0	1	0	0
19	0	1	0	0	1	1	1
20	0	1	0	1	0	0	0
21	0	1	0	1	0	1	0
22	0	1	0	1	1	0	0
23	0	1	0	1	1	1	1
24	0	1	1	0	0	0	0
25	0	1	1	0	0	1	0
26	0	1	1	0	1	0	0
27	0	1	1	0	1	1	1

28	0	1	1	1	0	0	1
29	0	1	1	1	0	1	1
30	0	1	1	1	1	0	1
31	0	1	1	1	1	1	1
32	1	0	0	0	0	0	0
33	1	0	0	0	0	1	0
34	1	0	0	0	1	0	0
35	1	0	0	0	1	1	1
36	1	0	0	1	0	0	0
37	1	0	0	1	0	1	0
38	1	0	0	1	1	0	0
39	1	0	0	1	1	1	1
40	1	0	1	0	0	0	0
41	1	0	1	0	0	1	0
42	1	0	1	0	1	0	0
43	1	0	1	0	1	1	1
44	1	0	1	1	0	0	1
45	1	0	1	1	0	1	1
46	1	0	1	1	1	0	1
47	1	0	1	1	1	1	1
48	1	1	0	0	0	0	1
49	1	1	0	0	0	1	1
50	1	1	0	0	1	0	1
51	1	1	0	0	1	1	1
52	1	1	0	1	0	0	1
53	1	1	0	1	0	1	1
54	1	1	0	1	1	0	1
55	1	1	0	1	1	1	1
56	1	1	1	0	0	0	1
57	1	1	1	0	0	1	1
58	1	1	1	0	1	0	1
59	1	1	1	0	1	1	1
60	1	1	1	1	0	0	1
61	1	1	1	1	0	1	1
62	1	1	1	1	1	0	1
63	1	1	1	1	1	1	1


Interface
Download
Vcc
GND
74HC04
74HC86
McMaster University ECE
OUT15
OUT0
IN15
IN0

(e)

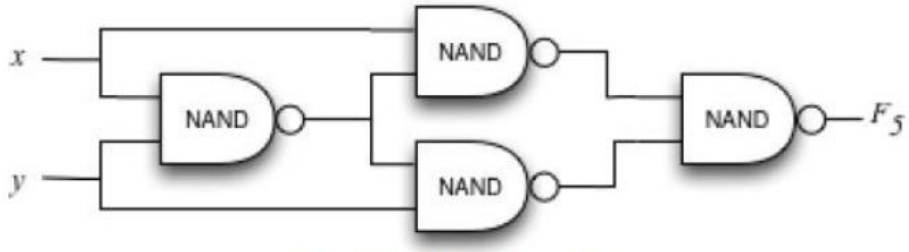
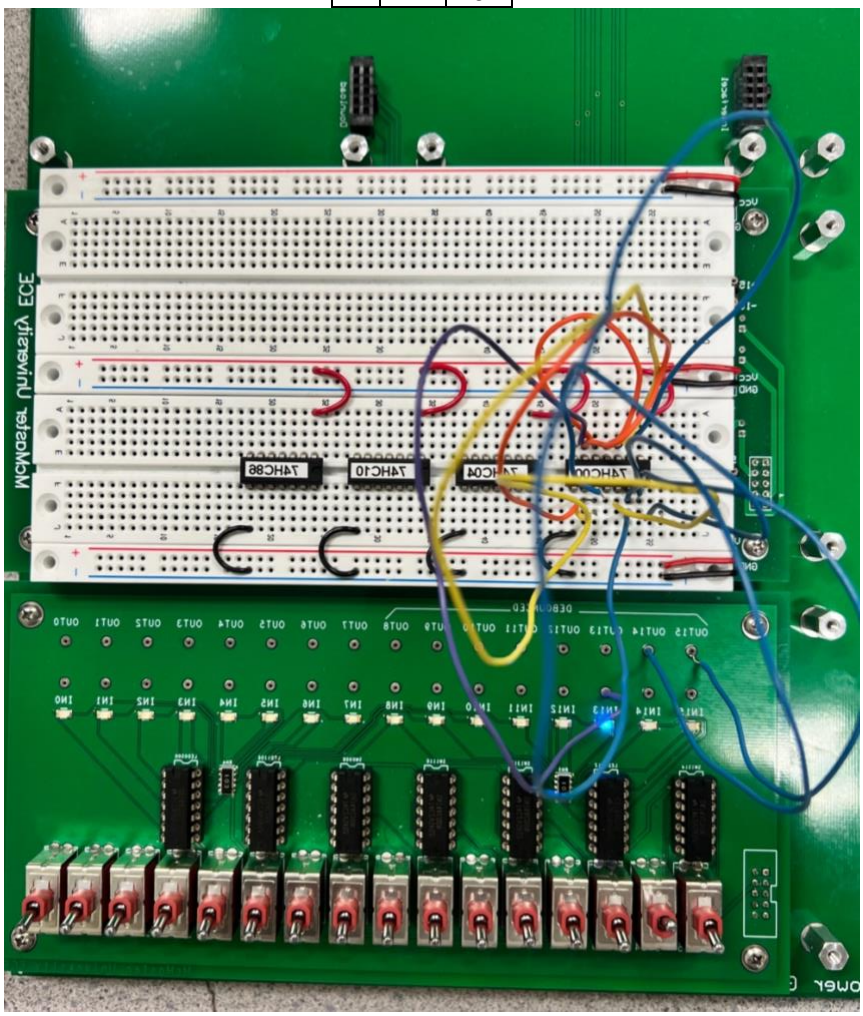


Figure 1.6: Logic Circuit 5

(i) Logic Function: (((XY)'X)'((XY)'Y)')'

(ii) Truth Table (Circuit 5)

x	y	F_5
0	0	0
0	1	1
1	0	1
1	1	0



1.4.3 Logical Equivalence

Milestone 3:

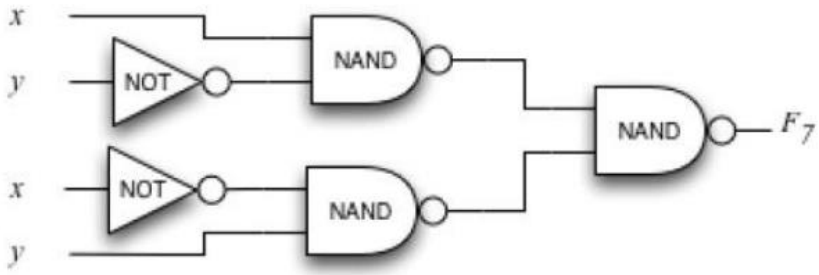
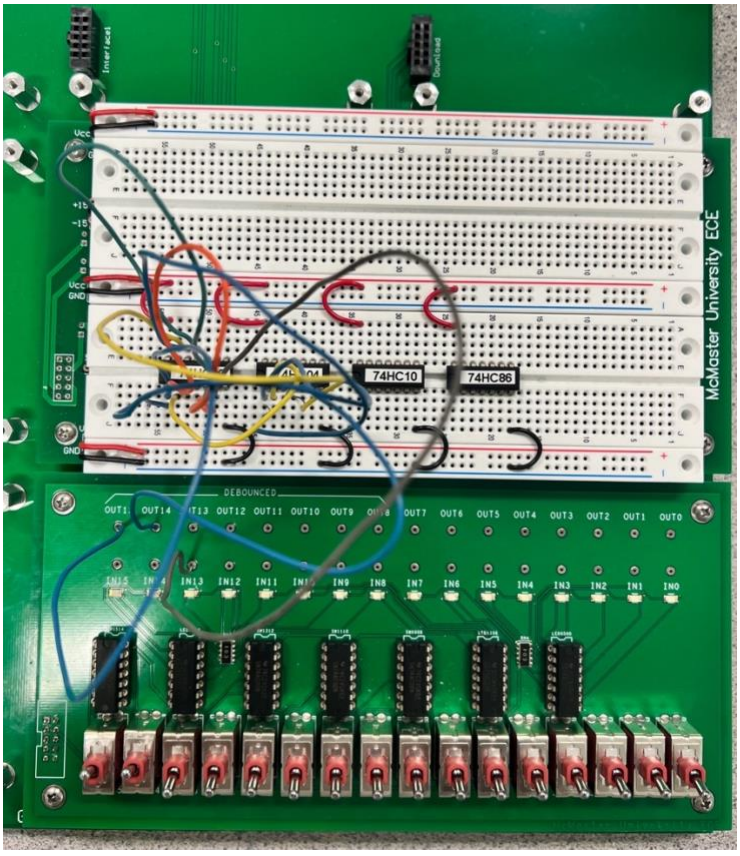


Figure 1.7: Logic Circuit 6

(i) Logic Function: ((xy')'(x'y)')'

(ii) Truth Table (Circuit 5)

x	y	F_7
0	0	0
0	1	1
1	0	1
1	1	0



Q. Build the following circuit and experimentally verify the truth table. Is this logically equivalent to a logical operator that you have seen before? If so, which one?

Answer: Yes, it is logically equivalent to XOR gate.

1.4.4 Enable/Disable Inverter

Q. The output of the 2-input XOR gate is HI when its inputs are different and LO otherwise. Verify the truth table for the XOR gate and explain how it could also be considered to be a "controllable inverter".

Answer: The XOR gate can be considered a controllable inverter because it controls the output by using one input only . For example if we look at the truth table of the XOR gate we see that only one of the inputs needs to be true for output to be true(‘ only one input switch should be on to get the output LED as on) and if both inputs are true or both are false it returns a false output.

S. No	Input#1-X	Input#2-Y	Output - XOR
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	0

1.4.5 Parity Generator

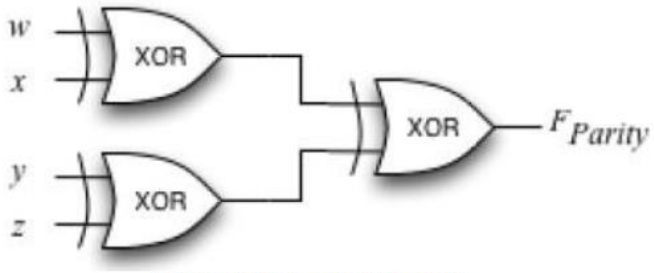
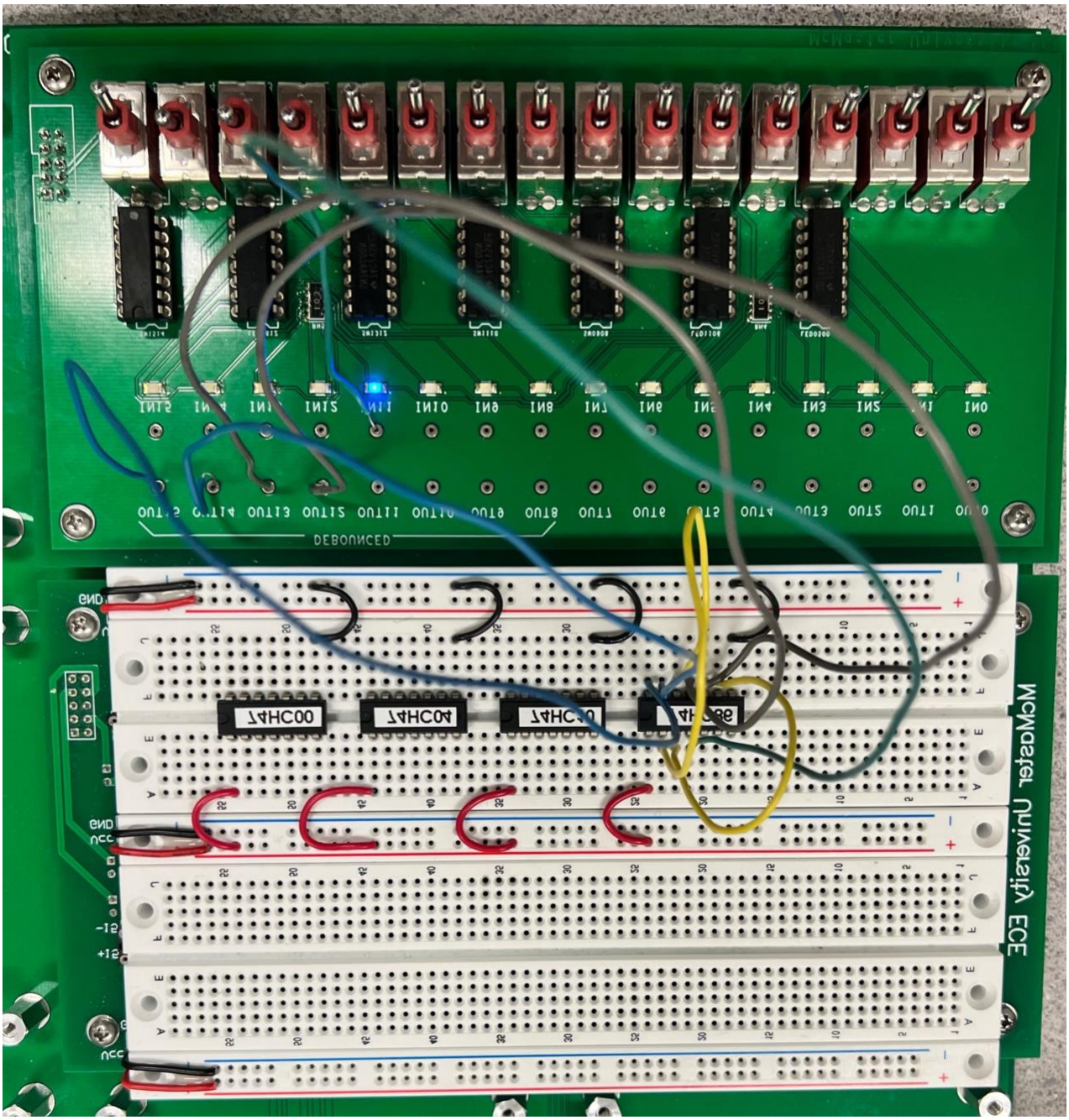


Figure 1.9: Logic Circuit 8

(i) Truth Table (Circuit 8)

S.No	w	x	y	z	F_{parity}
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	0

We verified that the output is 1 when there is an odd number of ones in the inputs and the output is 0 when we have an even number of 1 in the input as shown in the truth table as well.


DEBOUNCED
74HC00
74HC04
McMaster University ECE

1.4.6 Equality Detection

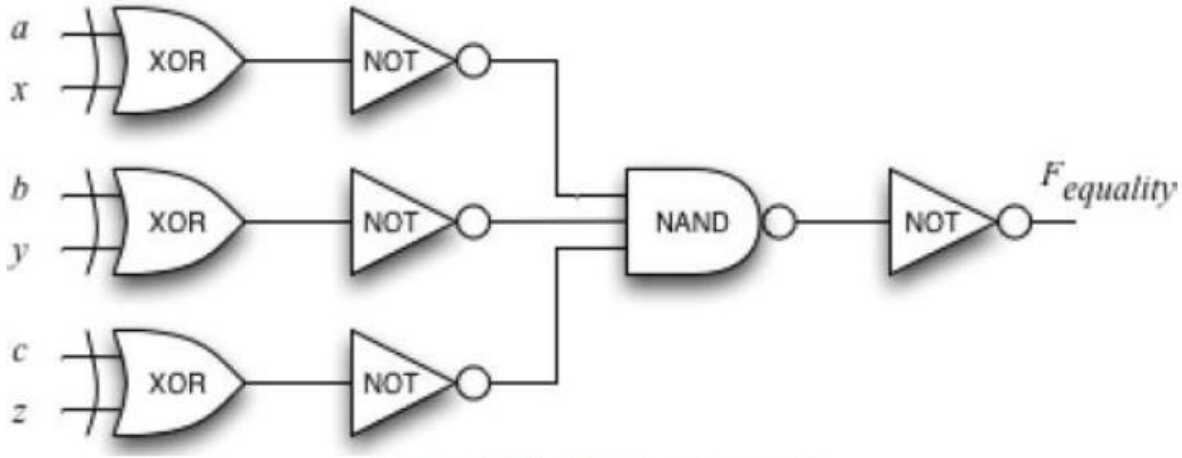
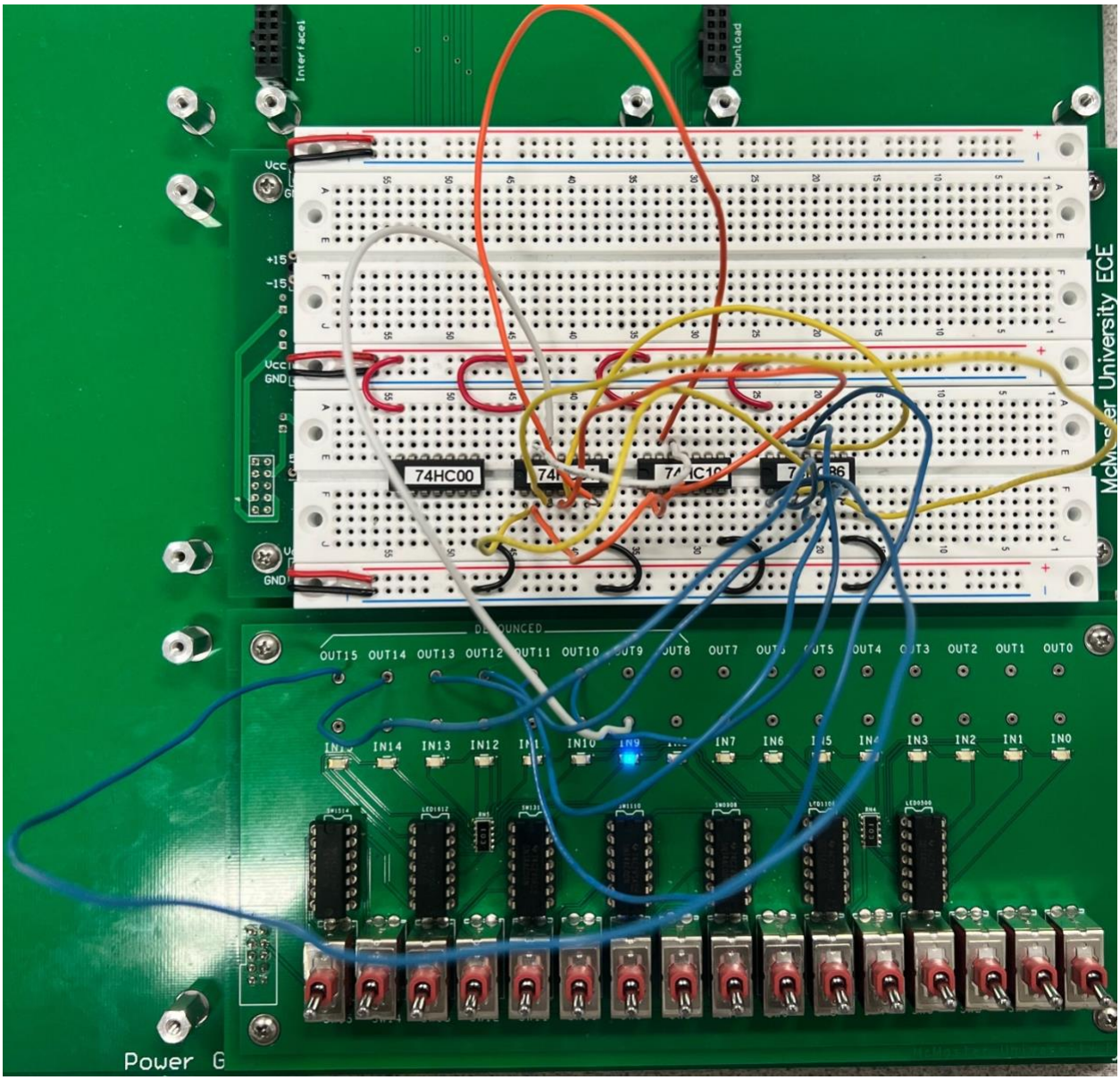


Figure 1.10: Logic Circuit 9

S. No	a	x	b	y	c	z	$F_{equality}$
0	0	0	0	0	0	0	1
1	0	0	0	0	0	1	0
2	0	0	0	0	1	0	0
3	0	0	0	0	1	1	1
4	0	0	0	1	0	0	0
5	0	0	0	1	0	1	0
6	0	0	0	1	1	0	0
7	0	0	0	1	1	1	0
8	0	0	1	0	0	0	0
9	0	0	1	0	0	1	0
10	0	0	1	0	1	0	0
11	0	0	1	0	1	1	0
12	0	0	1	1	0	0	1
13	0	0	1	1	0	1	0
14	0	0	1	1	1	0	0
15	0	0	1	1	1	1	1
16	0	1	0	0	0	0	0
17	0	1	0	0	0	1	0
18	0	1	0	0	1	0	0
19	0	1	0	0	1	1	0
20	0	1	0	1	0	0	0
21	0	1	0	1	0	1	0
22	0	1	0	1	1	0	0
23	0	1	0	1	1	1	0
24	0	1	1	0	0	0	0
25	0	1	1	0	0	1	0
26	0	1	1	0	1	0	0

27	0	1	1	0	1	1	0
28	0	1	1	1	0	0	0
29	0	1	1	1	0	1	0
30	0	1	1	1	1	0	0
31	0	1	1	1	1	1	0
32	1	0	0	0	0	0	0
33	1	0	0	0	0	1	0
34	1	0	0	0	1	0	0
35	1	0	0	0	1	1	0
36	1	0	0	1	0	0	0
37	1	0	0	1	0	1	0
38	1	0	0	1	1	0	0
39	1	0	0	1	1	1	0
40	1	0	1	0	0	0	0
41	1	0	1	0	0	1	0
42	1	0	1	0	1	0	0
43	1	0	1	0	1	1	0
44	1	0	1	1	0	0	0
45	1	0	1	1	0	1	0
46	1	0	1	1	1	0	0
47	1	0	1	1	1	1	0
48	1	1	0	0	0	0	1
49	1	1	0	0	0	1	0
50	1	1	0	0	1	0	0
51	1	1	0	0	1	1	1
52	1	1	0	1	0	0	0
53	1	1	0	1	0	1	0
54	1	1	0	1	1	0	0
55	1	1	0	1	1	1	0
56	1	1	1	0	0	0	0
57	1	1	1	0	0	1	0
58	1	1	1	0	1	0	0
59	1	1	1	0	1	1	0
60	1	1	1	1	0	0	0
61	1	1	1	1	0	1	0
62	1	1	1	1	1	0	0
63	1	1	1	1	1	1	1

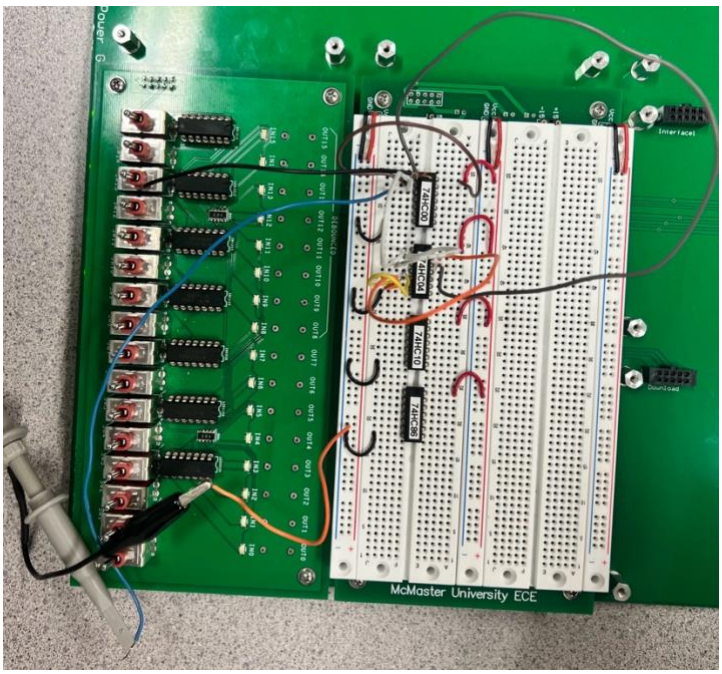

Interface1
Download
74HC00
DEBOUNCED
OUT15 OUT14 OUT13 OUT12 OUT11 OUT10 OUT9 OUT8 OUT7 OUT5 OUT4 OUT3 OUT2 OUT1 OUT0
IN14 IN13 IN12 IN10 IN7 IN6 IN3 IN2 IN1 IN0
Power G

Oscillator

Milestone 5:

Measure and clearly state the time for 1/2 of one cycle of this circuit using the automatic measurement functions of the oscilloscope.
How does this measured time compare to parameters t_{PLH} and t_{PHL} from the sn74HC00 data sheet? State t_{PLH} and t_{PHL}.

ANSWER: The total Period value from the oscilloscope is 67.5ns , thus the value of time for ½ of one cycle of this circuit is 33.75ns . This is the value for 5 gates that we have in this circuit thus for one gate the value should be 6.75ns. According to sn74hc00 the value of tplh= tphl= tpd should be between 9 and 45 as our Vcc(voltage) value is 3.3V (which is between 2V and 4.5V as stated in sn74hc00). Thus, our value of 6.75ns is not in between 9 and 45 , the possible reason for this could be that we assume the delay for the NAND gate in the circuit to be same as the delay for the NOT gates.



1.5 Discussion

Q. Referring back to the Gate Delay Measurement using the pulse F_{delay} (see Section 1.4.7), sketch and explain the output you would expect to see if the NAND in the original circuit were replaced with a NOR gate (you are not required to actually modify the circuit).

Answer: If the NAND gate is replaced with a NOR gate, then the NOR gate will always give an output of 0 (LO) as shown in the graph below. This is because our input for the NOR gate will always be HI.