Logic Design 2DI4
Lab 2

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As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Mustafa Shahid, shahim45, 400440384]**

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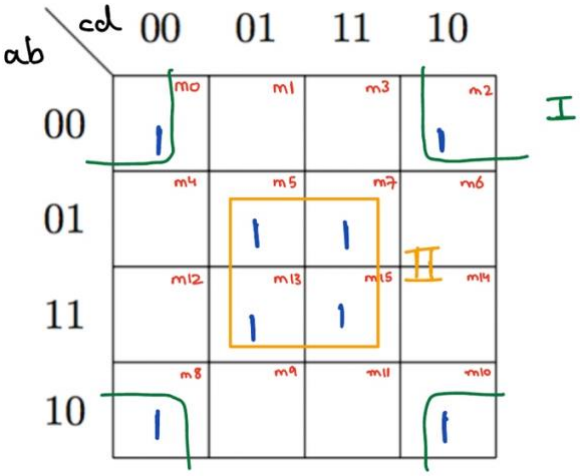
2.4.1 The Karnaugh-Map for Boolean Minimization

Milestone 1

1. Minimize and implement the following function using only NAND gates (note if you design calls for inverter(s) you may use inverter IC to simplify your implementation if you can explain how a NAND can become an inverter):

$$F(a,b,c,d) = \Sigma(0,2,5,7,8,10,13,15)$$

Answer:



F(a,b,c,d) = I + II

= b'd' + bd

= ((b'd' + bd)')'

= **((b'd')'(bd)')'**

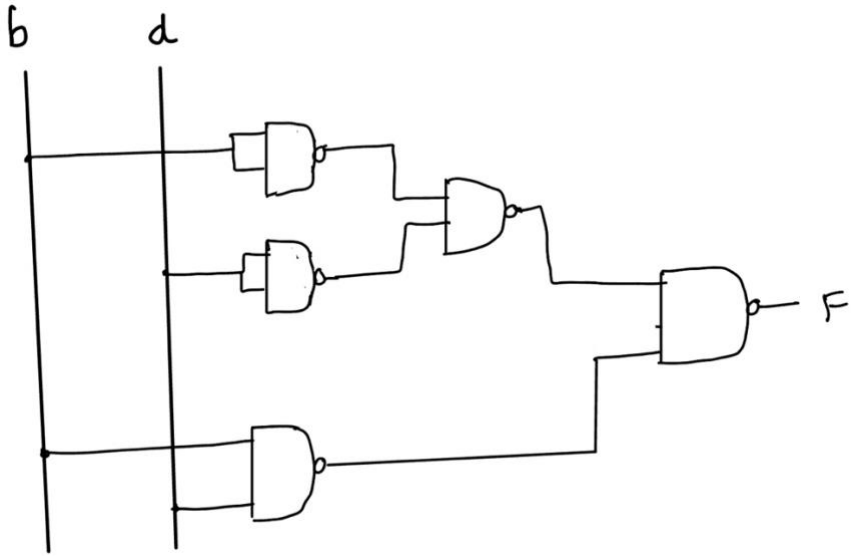
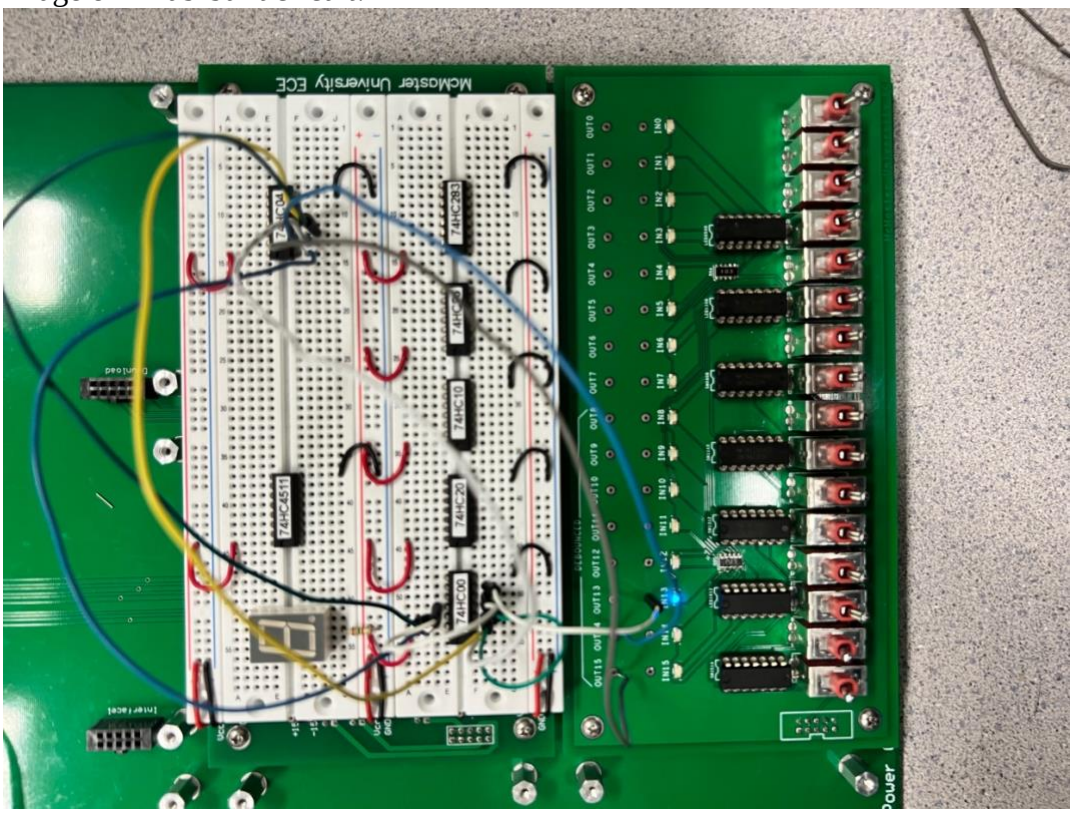


Image of in lab-built circuit:



2.4.2 The Multiplexer (MUX)

Milestone 2:

2. A MUX is a combination circuit that selects binary information from one of several inputs and logically directs that input to the output channel(s). Complete the following circuit to implement a 4:1 MUX. The input are data lines D0 to D3. The select lines are S0 and S1 (hint: given two select variables, how many items can you uniquely select?). Output is Y. Build the circuit and verify the function table.

Table 1: MUX Function Table

S_1	S_2	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

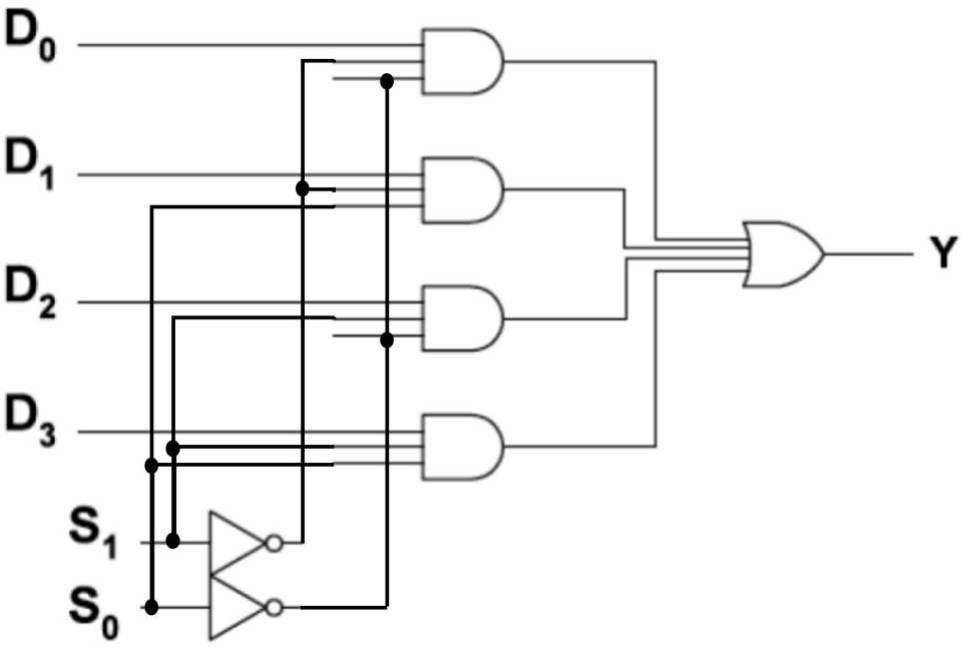
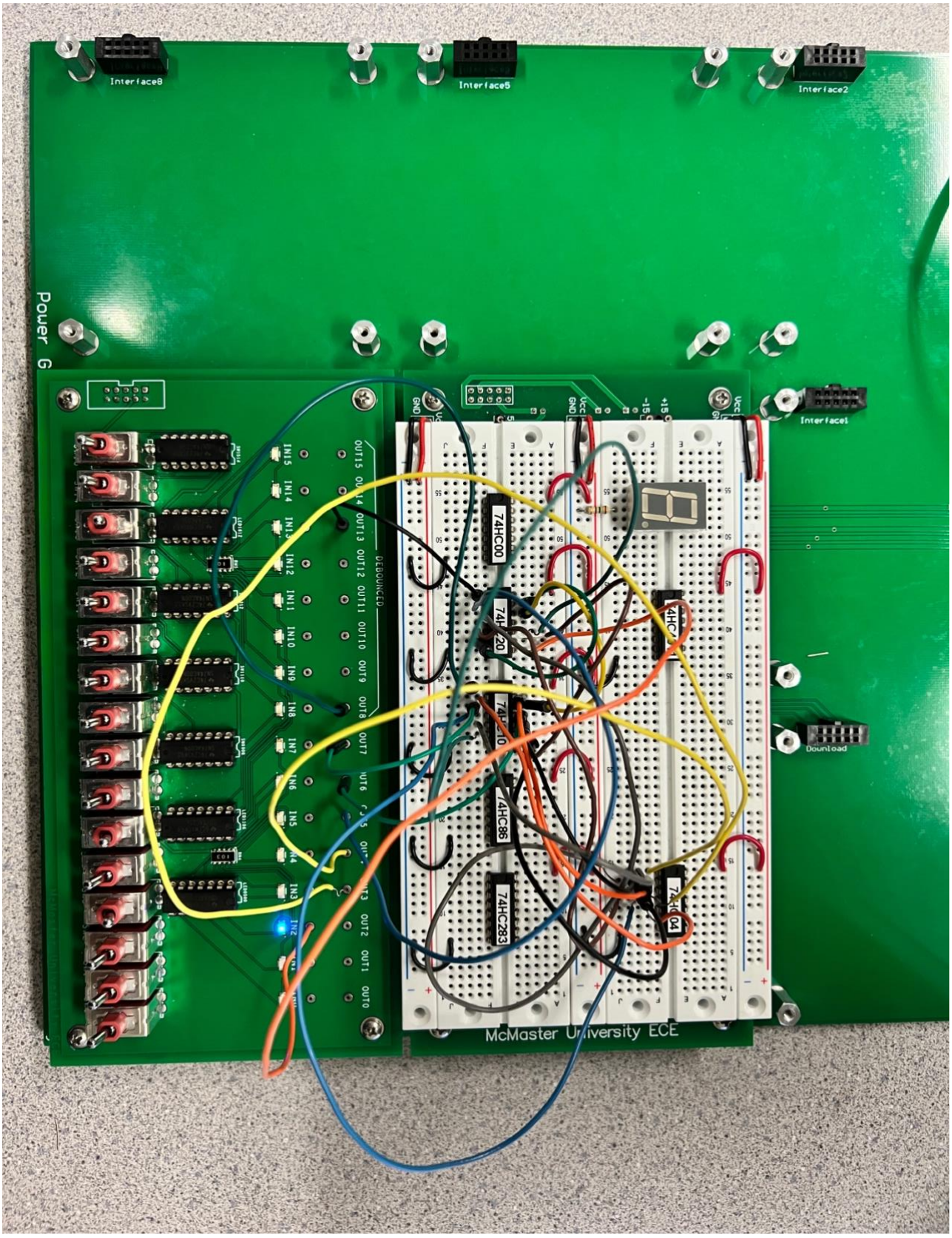


Figure 1: Completed 4:1 MUX circuit

Image of in lab-built circuit:



The above circuit we built verified the results in the truth table.

2.4.3 Half Adder

3. The fundamental circuit for computation is the half adder. Figure 2.2 illustrates the half-adder combinational logic circuit. The output S is the sum of inputs A and B, where Cout represents a carry out. Build this circuit and verify the truth table. Use switches for inputs and LEDs for output(s).

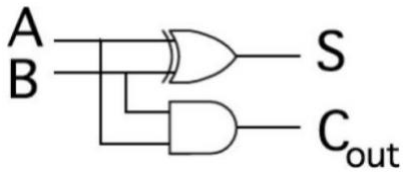
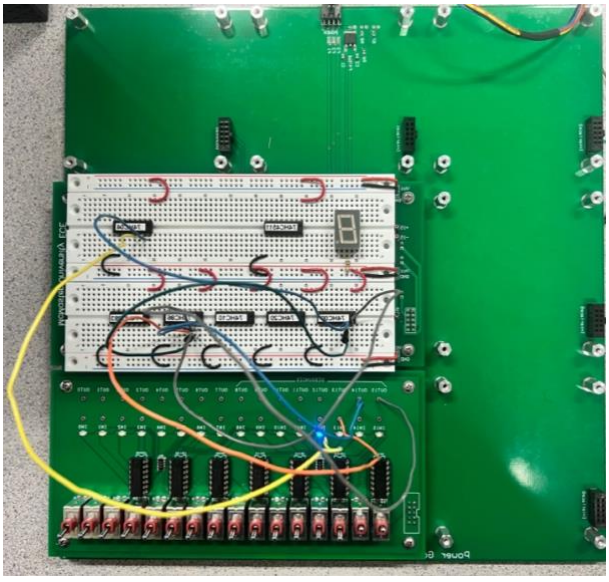


Figure 2: Half-adder circuit

Half-Adder Truth Table			
Input		Output	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Image of in-lab built circuit:



The above circuit we built verified the results in the truth table.

2.4.4 Full Adder

4. The full adder is a combination of two half-adders to produce a combinational logic circuit with a sum output (S), and a carry output (Cout) from inputs A, B, and Cin. Figure 2.3 illustrates the full-adder combinational logic circuit. This arrangement permits fast parallel organization for the addition of n-bit numbers. This circuit is the basis for many arithmetic functions, such as, subtraction, multiplication, and division. Build this circuit and verify the truth table. Use switches for inputs and LEDs for output(s)

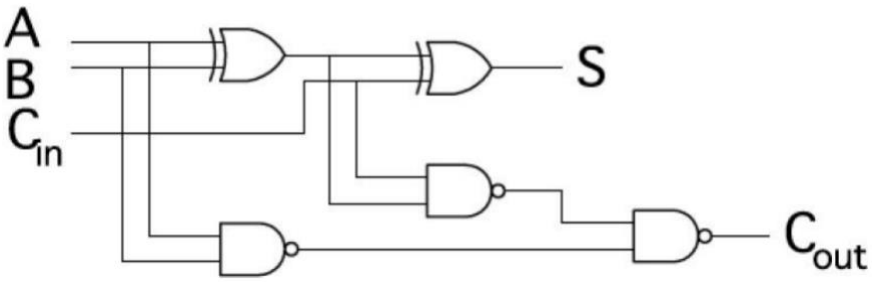
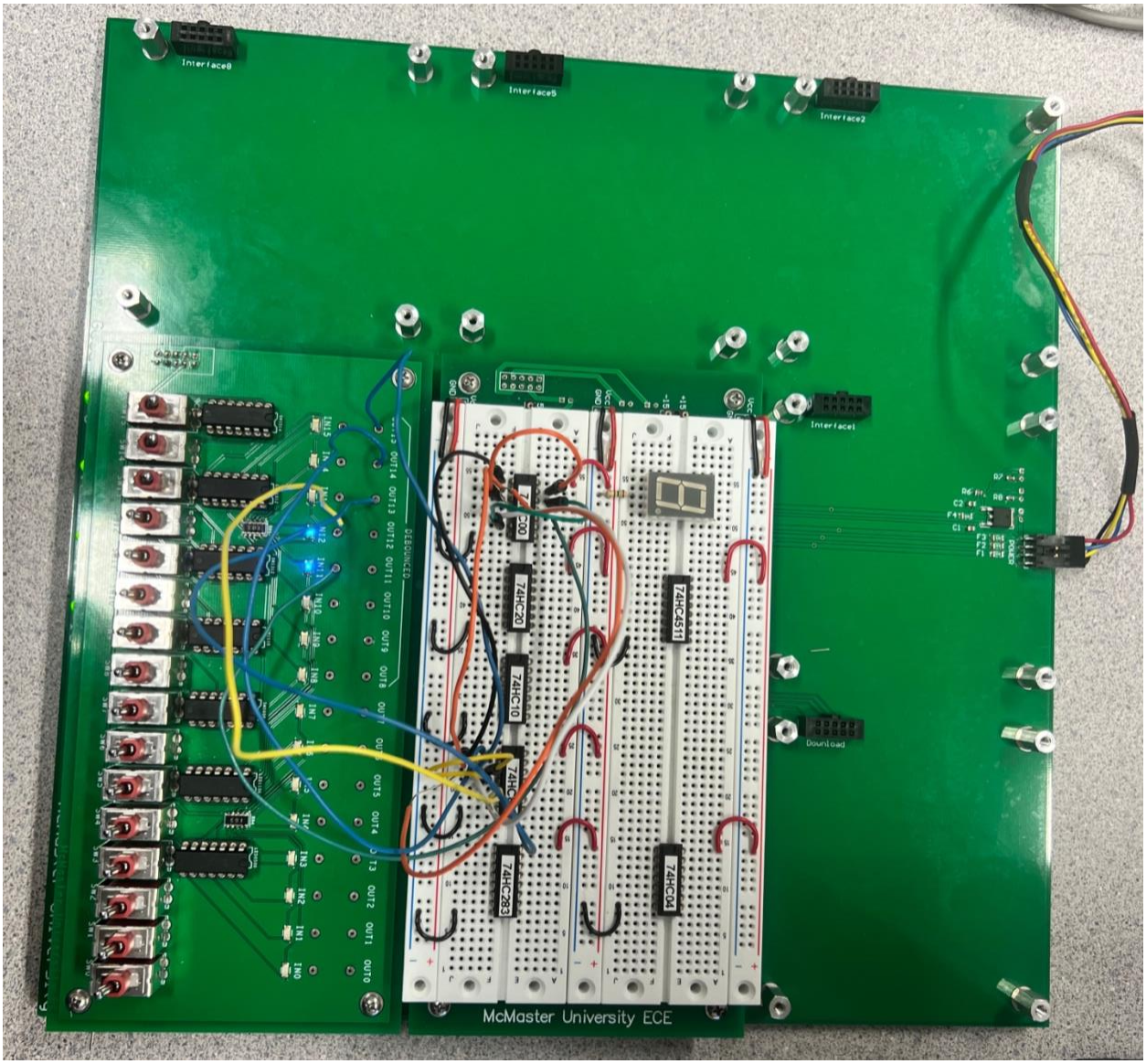


Figure 3: Full Adder circuit

Full-Adder Truth Table				
Input			Output	
A	B	C	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Image of in-lab built circuit:



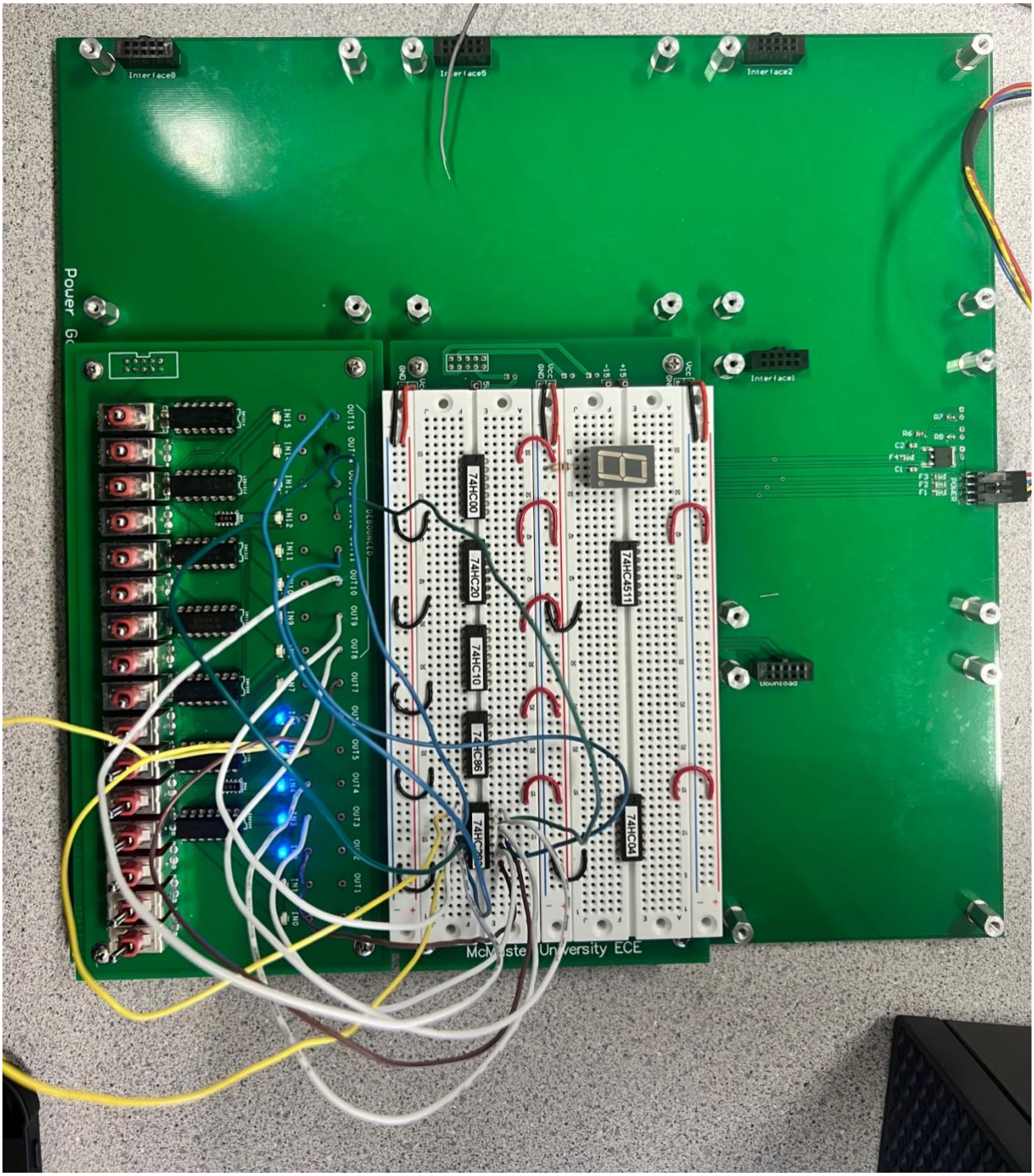
The above circuit we built verifies all the values presented in the truth table.

2.4.5 n-bit Adder using cd74HC283

5. An n-bit adder can be constructed by connecting the carry-out n full adders. The input carry to the first full address in the serial chain is C0 and the output from the final full adder is Cn. Because of the serial carry configuration, this arrangement is often referred to as a ripple carry adder and as a result it has the undesirable characteristic that add time is proportional to n. A better approach is to form the sum and carry out in a parallel arrangement, such as the arrangement of the cd74HC283. The cd74HC283 is a 4- bit parallel adder with internal carry look-ahead. Review the data sheet for this IC and note the internal configuration of gates. Verify the operation of the cd74HC283 by wiring the IC and completing the table below. Use switches for inputs and LEDs for output(s). Clearly record the output as unsigned and as signed 2's complement.

4-bit Adder Truth Table						
Input			Ouput			
C	A	B	Sum	Decimal Equivalent if Sum is unsigned	Decimal Equivalent if Sum is 2's Complement	C
0	0000	0000	0000	0	0	0
0	0000	0011	0011	3	3	0
0	0011	0000	0011	3	3	0
1	0011	0000	1011	11	11	0
0	0111	1000	1111	15	15	0
1	0111	1000	0000	16	-0	1
0	1000	1000	0100	4	4	0
0	0011	1111	0101	21	-5	1
0	0111	1111	0011	19	-3	1
0	1001	1111	0001	17	-1	1
0	1111	1111	0111	23	-7	1
1	1111	1111	1111	31	-15	1

Image of the in-lab built circuit:



The above circuit we built verified the results in the truth table.

2.4.6 Addition and Subtraction using cd74HC283

Milestone 3

6. A parallel adder may be used to add or subtract 4-bit numbers. Given the following arrangement, when S=0 the output is A+B. When S=1, the output is A-B. Construct and verify this circuit. Explain the operation (hint: what are S and the XORs doing?).

Note that this adder/subtractor may be used to take the 2's complement of an input B by setting A=0000 and S=1. Verify this for several test cases. This feature will be used in the following circuit so do not disconnect this circuit.

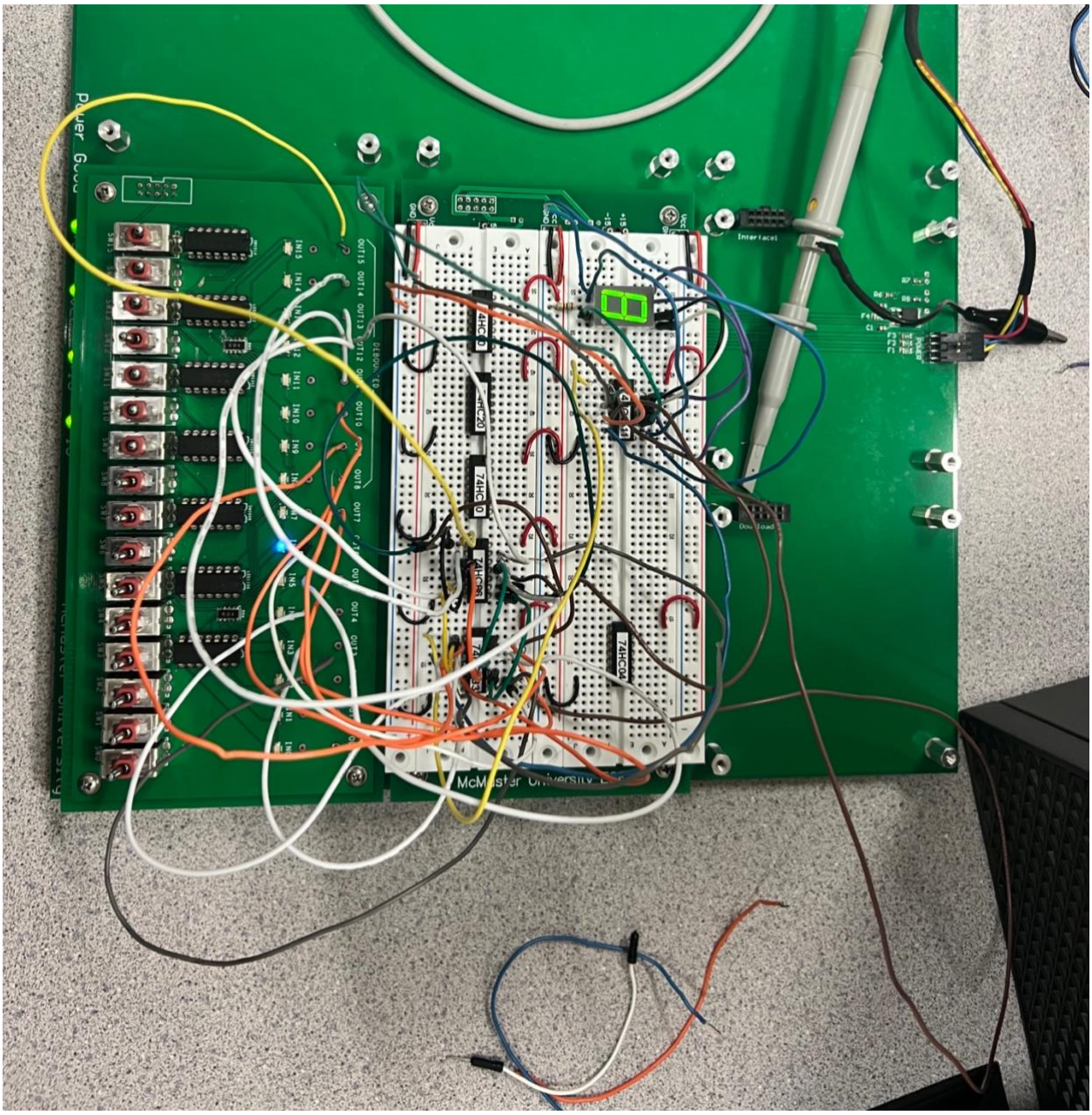
ANS-6)

When S is 0 we are in addition and B will not change as XOR doesn't change anything with 0. When S is 1 each bit of B is inverted due to XORs giving us the one's complement of B which is used to conduct operations.

2.4.7 Binary Code Decimal and the 7-Segment Display Encoder 7.

The seven-segment display is an easy and very common way to display decimal from binary codes. Each segment of the display is lit by pulling the input to the display LO. The cd74HC4511 BCD to 7-segment encoder will drive the display (part number: 157142V12703) with the correct current-limiting requirements. NEVER CONNECT THE DISPLAY INPUTS TO GROUND OR +5V – YOU WILL DESTROY THE DEVICE. Connect the circuit as shown below and leave this circuit connected for use in a following circuit. However, before proceeding you should connect the 4 BCD inputs to 4 sequential toggle switches and verify you understand the device operation.

Image of the in-lab built circuit:

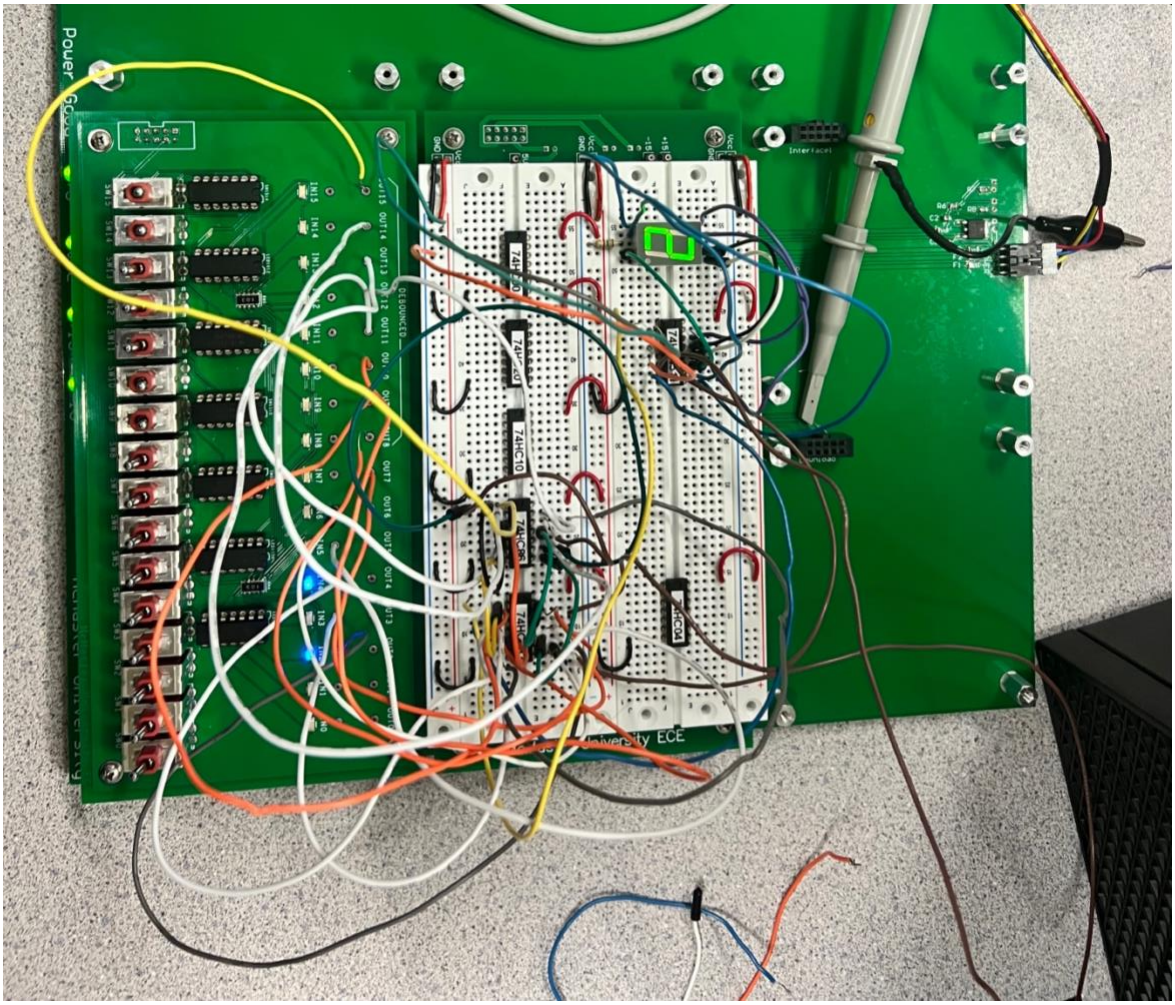


The above circuit we built verified the results in the truth table.

2.4.8 BCD, 7-Segment Display, and the 2's Complement

8. Connect the output of the adder/subtractor circuit from Section 2.4.6 to the input of the cd74HC4511 BCD to 7-segment encoder circuit from Section 2.4.7.

Image of the in-lab built circuit:



(Bonus) Display the Correct Negative BCD

Bonus Milestone

After completing Milestones 1 to 4, design a combinational logic circuit to correctly display a negative BCD number after cd74HC283 subtraction. To denote a negative, turn on a decimal point on the seven-segment display. You will have to explain your design.