Logic Design 2DI4
Lab 3

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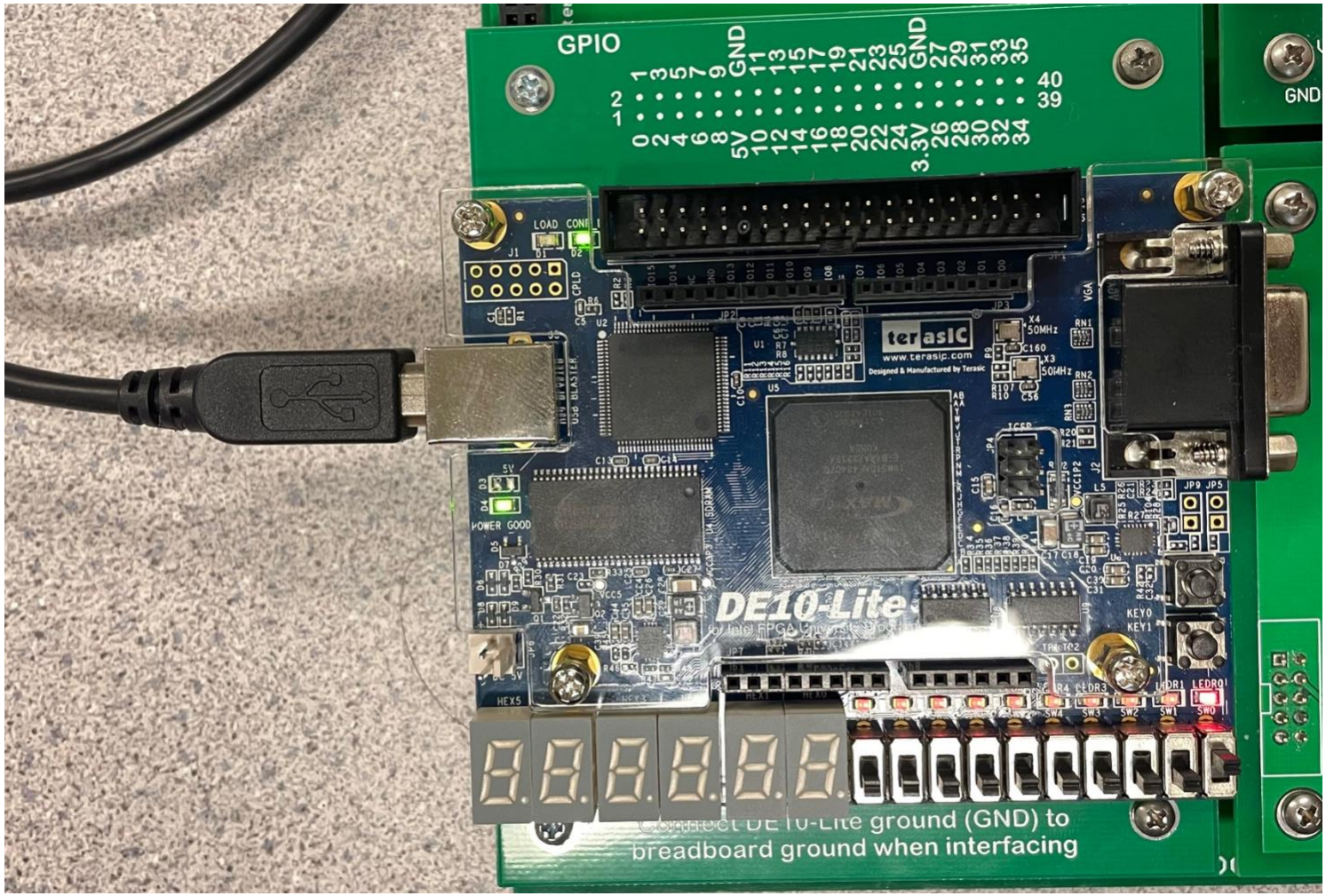
As a future member of the engineering profession, the student is responsible for performing the required work in an honest manner, without plagiarism and cheating. Submitting this work with my name and student number is a statement and understanding that this work is my own and adheres to the Academic Integrity Policy of McMaster University and the Code of Conduct of the Professional Engineers of Ontario. Submitted by **[Abaan Khan, khana454, 400428399]**


GPIO
DE10-Lite
terasIC
www.terasic.com
Designed & Manufactured by Terasic
Connect DE10-Lite ground (GND) to
breadboard ground when interfacing

3.5.2 "Programming" 3-to-8 Line Decoder in physical ICs.

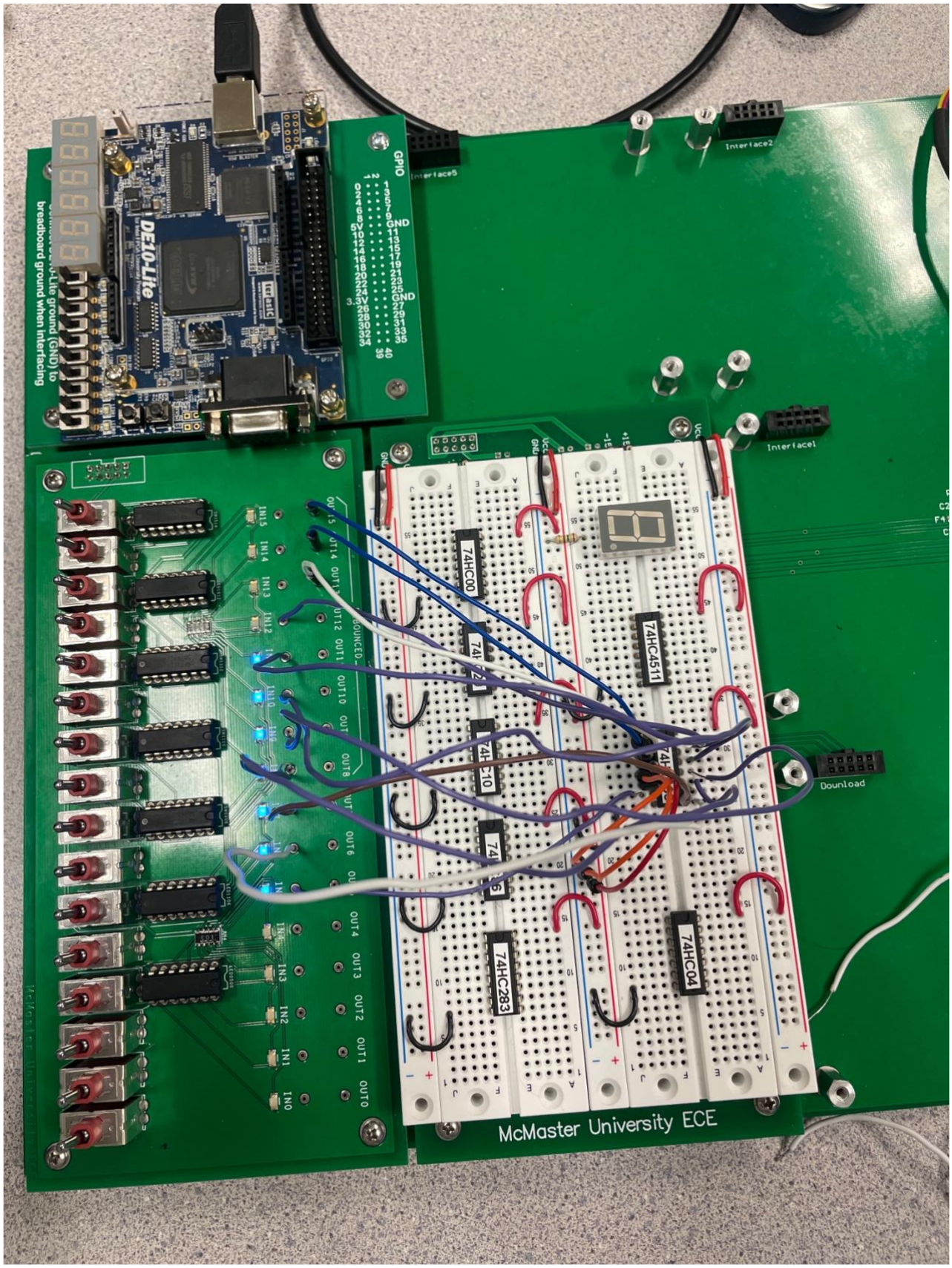
1. Verify the function table for the sn74HC138 is a 3-to-8 line decoder from Table 4.6 of your textbook (Truth Table of a Three-to-Eight-Line Decoder). Use switches for X, Y, Z selects and LEDs for the outputs. Refer to the data sheet for handling the enable pins.

Table 4.6
Truth Table of a Three-to-Eight-Line Decoder

Inputs			Outputs							
x	*y*	*z*	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Figure 1: Truth Table of a 3-8 decoder.

Image of our circuit we built in lab :



The above circuit verifies the results in the truth table taken from the textbook.

2. Referring to your textbook, find the truth table and logic expression for a full adder. "Program" this full-adder circuit such that F1 represents the sum (S) and F2 represents the carry (C). Mark every connected row-column intersection with an X. Build the circuit and verify operation.

Milestone 2

Answer:

Table 4.4
Full Adder

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Figure 2: Truth table for a full adder.

We have:

S = Sum(m1, m2, m4, m7)

C = Sum(m3, m5, m6, m7)

Therefore, the final circuit using 3:8 decoder:

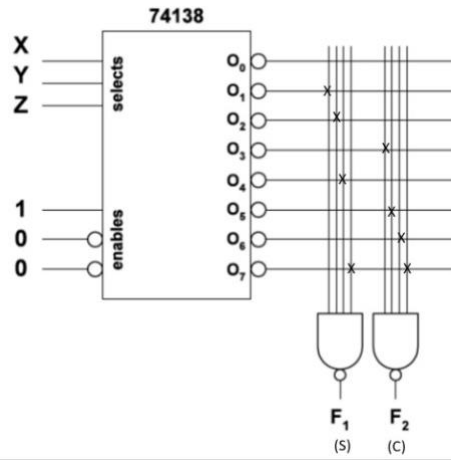
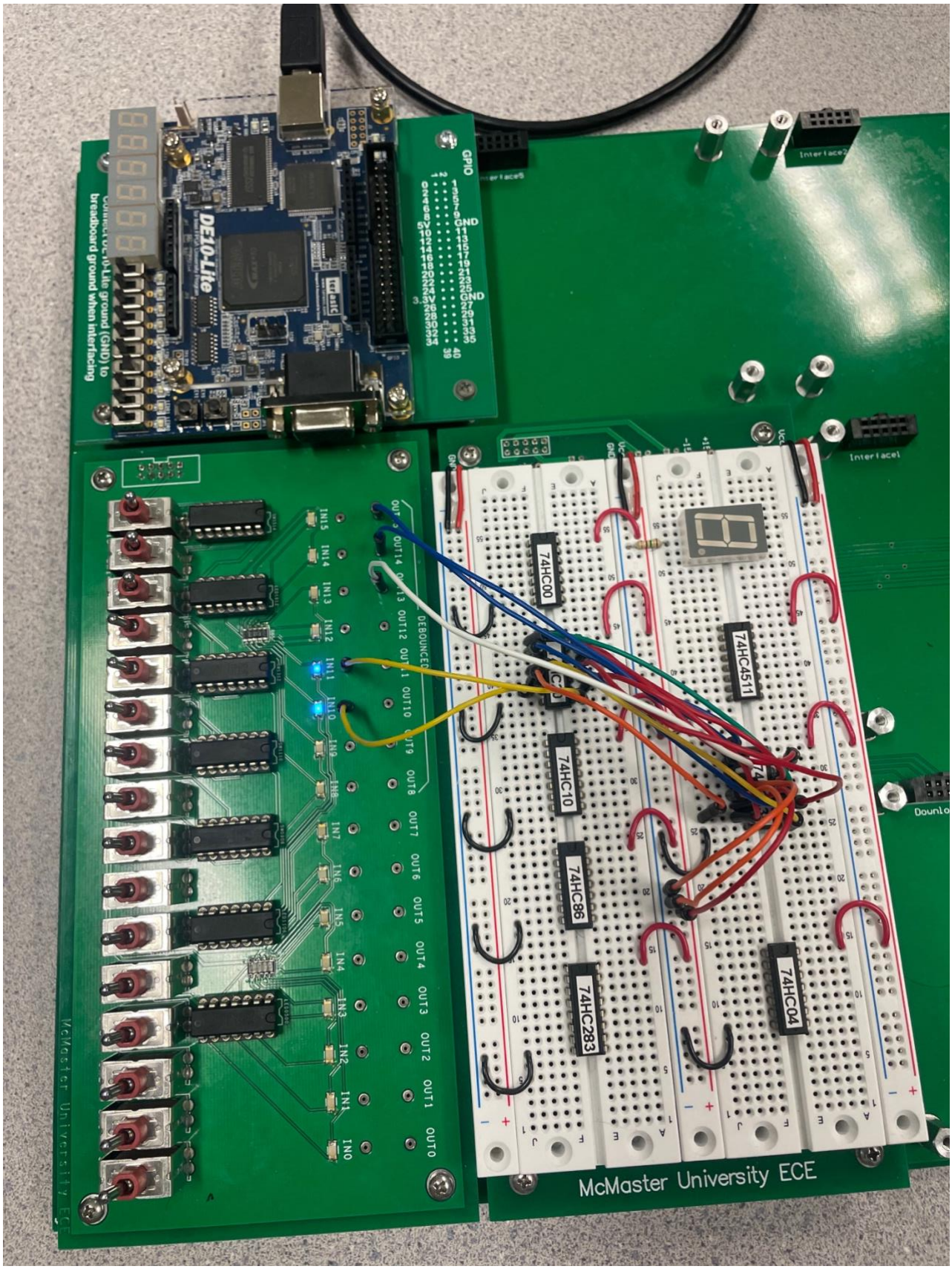


Figure 3: Full Adder circuit using 3:8 decoder.

Image of our circuit we built in lab:



The above circuit verifies the results of the truth table taken from the textbook.

3.5.3 3-to-8 Line Decoder in HDL

Milestone 3

Refer to your textbook for the design of a 3-to-8 Line Decoder (input: 3-bits binary code. output: 1 of 8 bits). For reference, a 3-to-8 line decoder schematic can be found in Mano Figure 4.18 (Figure 4.19 is a 2-to-4 line decoder with enable). HDL Example 4.1 is also a good starting point. Using Quartus II define a 3-to-8 Line Decoder, compile your model and load it on to the CPLD. For inputs connect wires from toggle switches to CPLD inputs. For outputs connect CPLD outputs to LEDs. For your report, include a screen capture of your modelling – ensure all team member names and student numbers appear in the comments of the Verilog model text.

Answer:

The Verilog model needs to be made based on the circuit shown below:

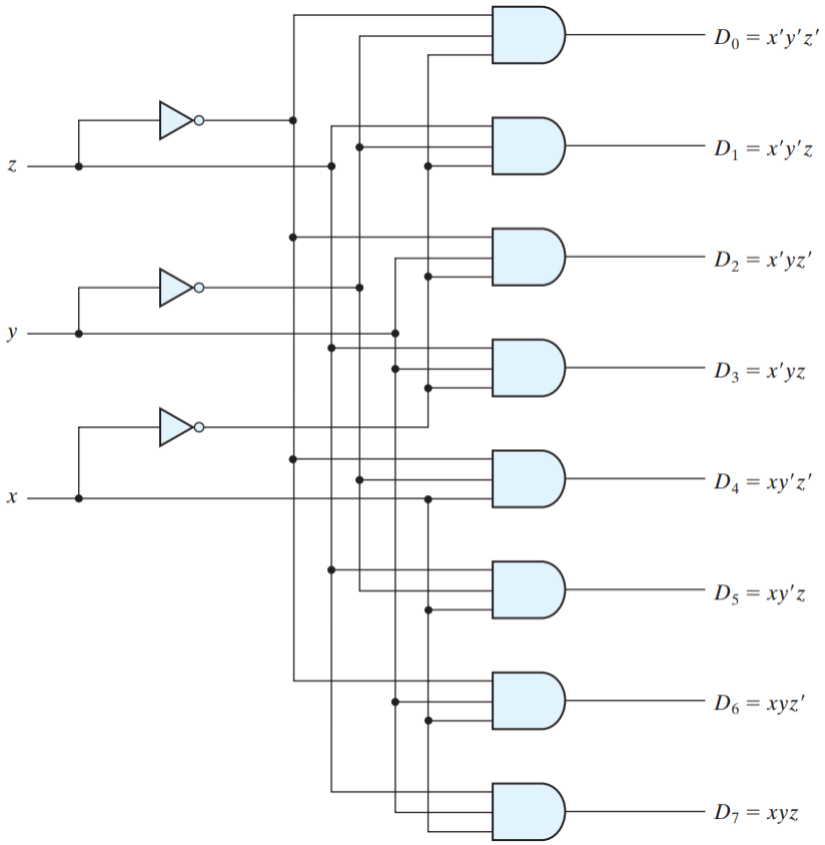
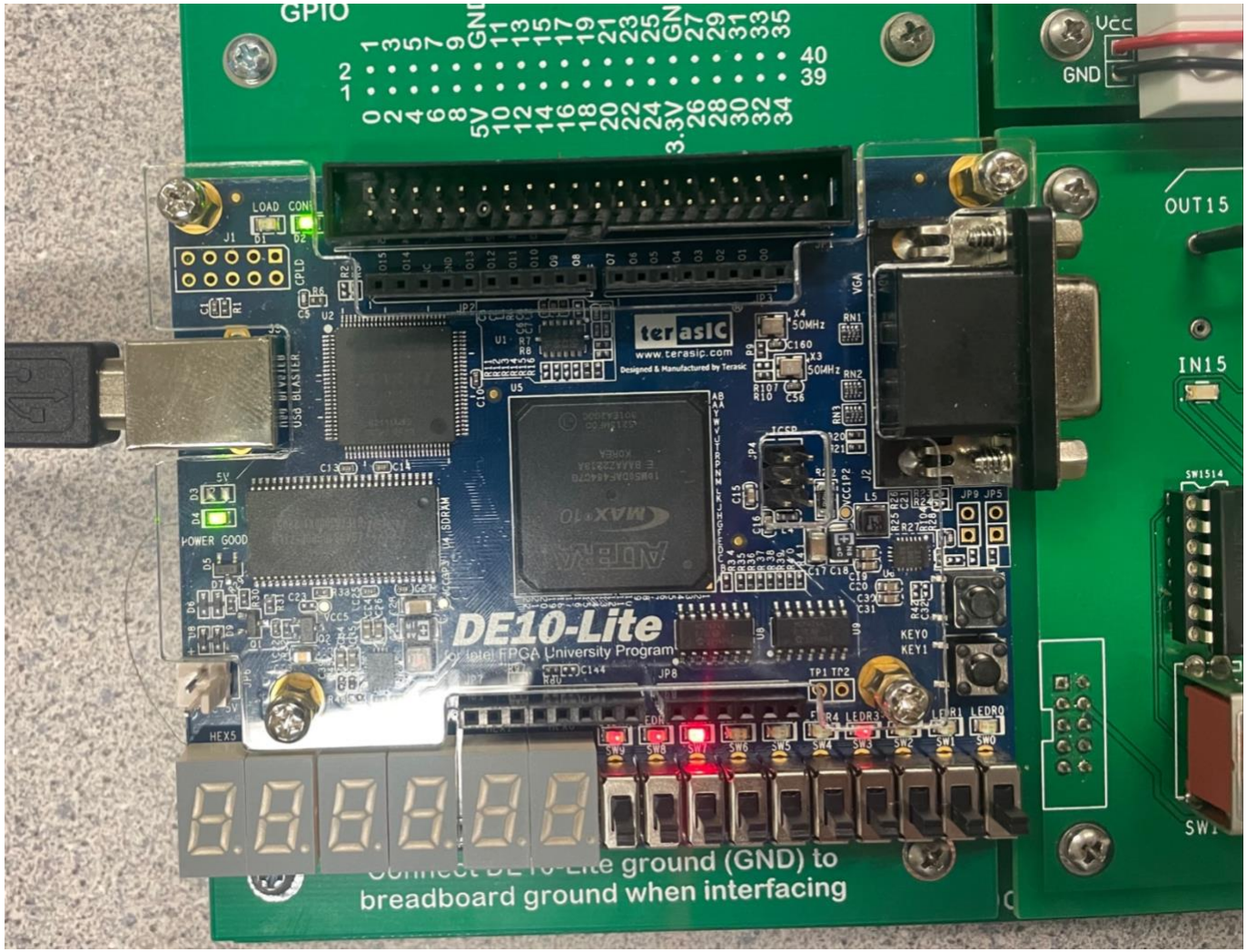
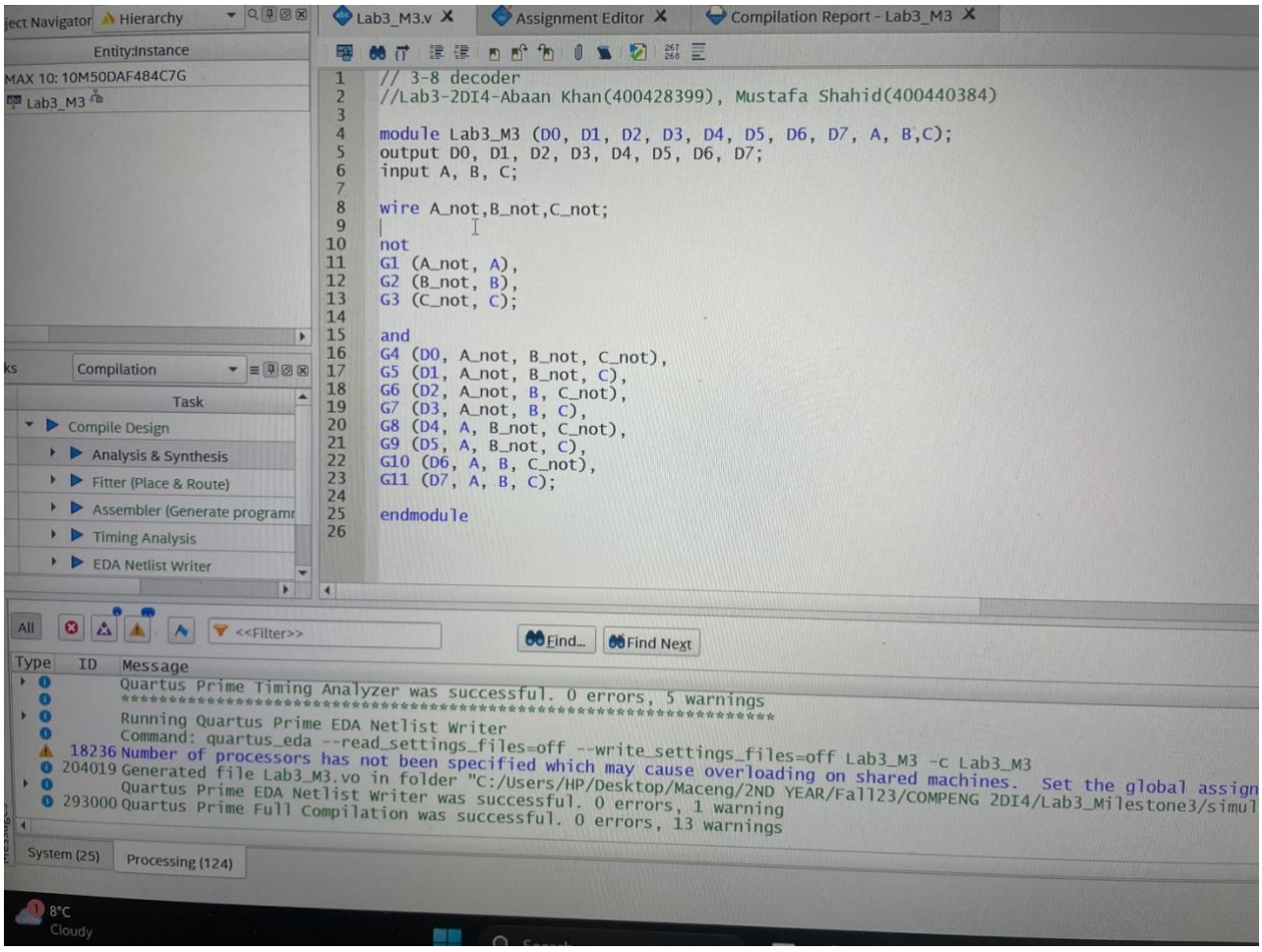


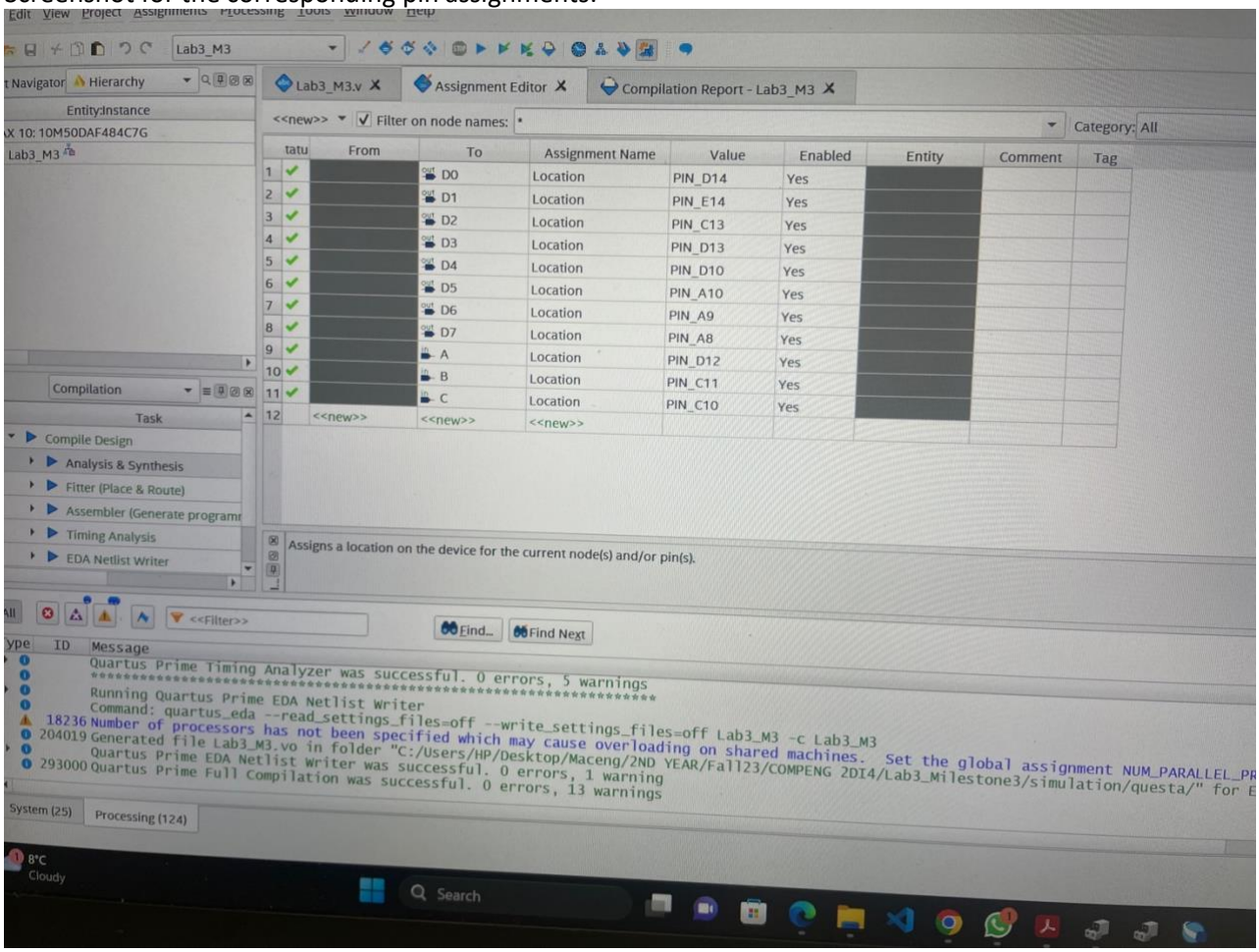
Figure r# 4: Circuit for 3:8 Decoder using primitive logic gates.


GPIO
Vcc
GND
OUT15
IN15
terasIC
www.terasic.com
DE10-Lite
for Intel FPGA University Program
POWER GOOD
HEX5
KEY0
KEY1
Connect DE10-Lite ground (GND) to
breadboard ground when interfacing

A screenshot of our Verilog code

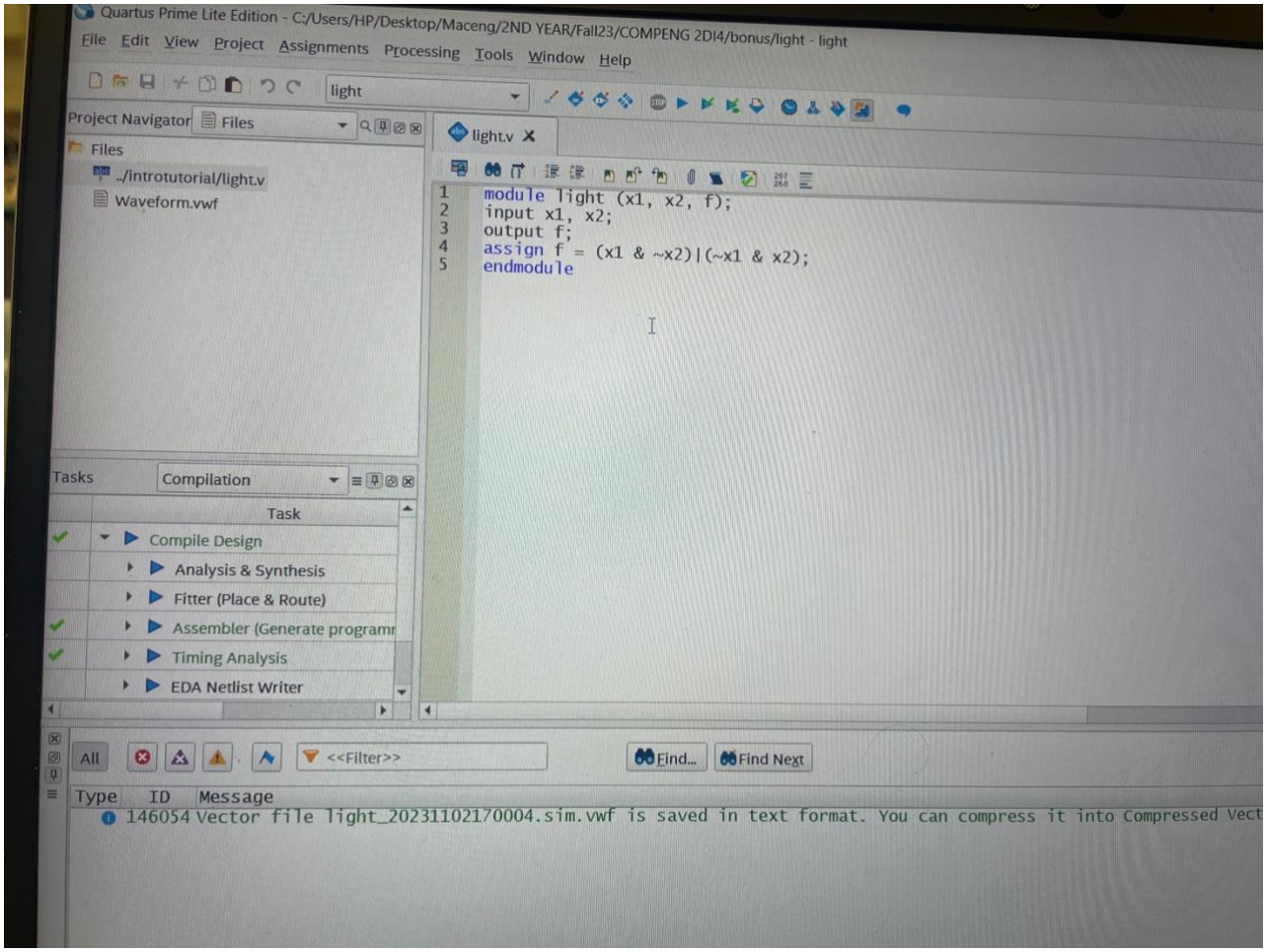


Screenshot for the corresponding pin assignments:

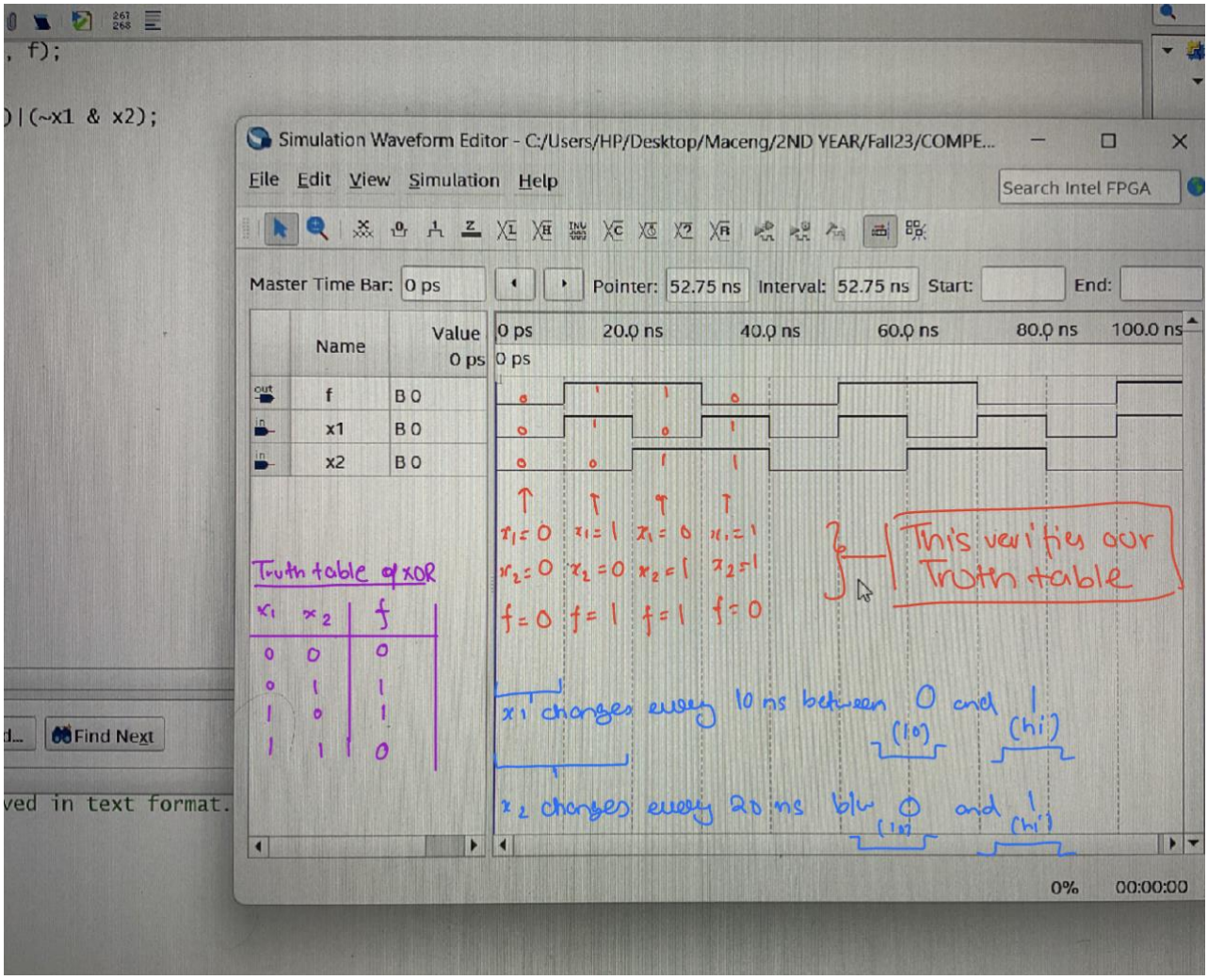


3.5.5 (Bonus) HDL Functional Simulation of Lamp Controller
Bonus Milestone: HDL Simulation of Lamp Controller
Return to your Lamp Controller, but instead of external switch connections you will run a basic simulation by manually creating a functional simulation with Vector Waveform Files or a testbench module to test all input combinations, and perform a functional simulation. Use Primitive Gates Model (AND, OR, NOT, etc.) for your design entry of the lamp controller. Note section 3.6 has additional information to assist with simulation.
For this bonus include in the report:

1. *Copy of Verilog HDL code entry defines the Lamp Controller (place in appendices) [4 marks],*



2. An annotated screenshot of functional simulation results with all combinations of bit inputs. The annotation should illustrate your understanding of the connection between the inputs and outputs. [2 marks],



3. *A short description of how you tested and verified the circuit [4 marks].*

ANSWER-3:

In the manual, we are instructed to use 20ns for the x1&x2. However, we modified the x1 value to 10ns and left x2 at 20ns because we are using an exclusive OR gate and this helps us to differentiate between the output and clearly view the results of our simulation.