Circuit Schematic

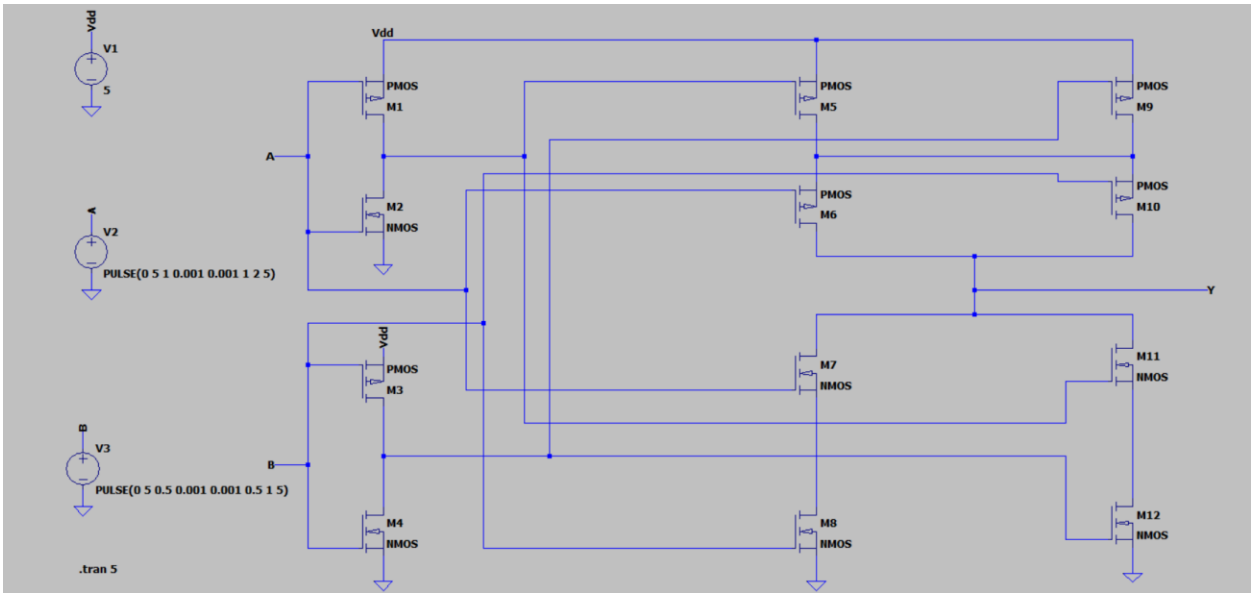


Figure 1: XOR Gate schematic using transistors

The LTSpice simulation gives us the outputs resembling an XOR gate. So, our schematic is functioning correctly.

Ideal Sizing

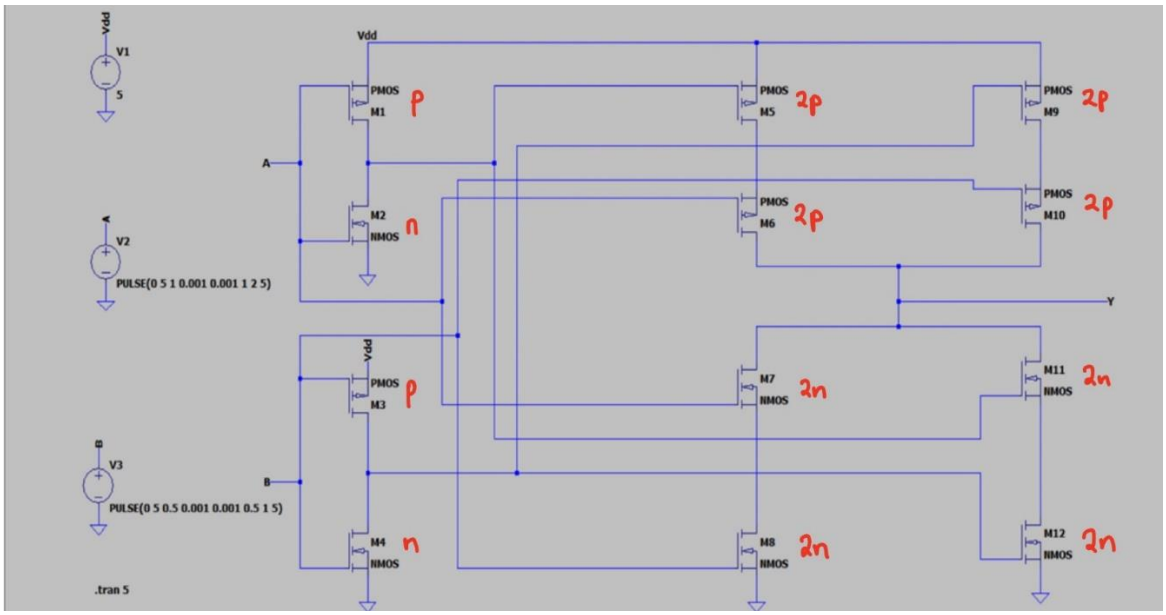


Figure 2: Sizing notations

Making sure all transistors in the current situation have identical resistances is the goal of the design.

$$R_{ON} \propto \frac{L}{W}$$

The transistor's resistance should be inversely proportional to the width / length. Assigning W and L values is more difficult than just setting them equal because NMOS and PMOS transistors have distinct charge mobilities. To guarantee that the resistances of the devices match, various ratios of **W/L** must be used. Since the electrons' charge mobility is often higher than the holes' charge mobility, we must follow $\left(\frac{W}{L}\right)p > \left(\frac{W}{L}\right)n$. Normally, $\left(\frac{W}{L}\right)p$ and $\left(\frac{W}{L}\right)n$ are made to be 5/1 and 2/1 in the designs, respectively. The size ratio comes out to be 5/2 and these values serve as a measure of control of τ_{HL} and τ_{LH} values for circuit. By ideal sizing we make sure that $\tau_{pHL} = \tau_{nHL} = \tau_{ref.}$ The p $[\left(\frac{W}{L}\right)p]$ and n $[\left(\frac{W}{L}\right)n]$ values of each MOSFET are then determined so that the resistance across all current paths does not surpass the resistance of the fundamental inverter. In the second figure of sizing notations, these values are displayed next to each transistor.

Implementing Ideal Sizing

It is impossible to get the perfect transistor sizing since we have no control over the width and length of the transistors we have. The MC14007UB IC's designers have determined the transistors' width and length. It is true that the MOSFETs roughly fit the sizing ratios we require, even though we are incapable of altering the transistors' sizes to our preferred dimensions. $\left(\frac{W}{L}\right)p = 2.5 \times \left(\frac{W}{L}\right)n$.

The detected delays of the rising and falling edges of inputs and outputs could be altered to be more consistent by precisely matching the resistances of the transistor. When included into bigger systems, this circuit design would be more beneficial because of the improved value of τ_{pHL} and better noise allowances. Therefore, optimum noise allowances and improved τ_{pHL} value cannot be anticipated as these modifications have not been implemented, but they can be expected to be right at the corner.

Functional Testing

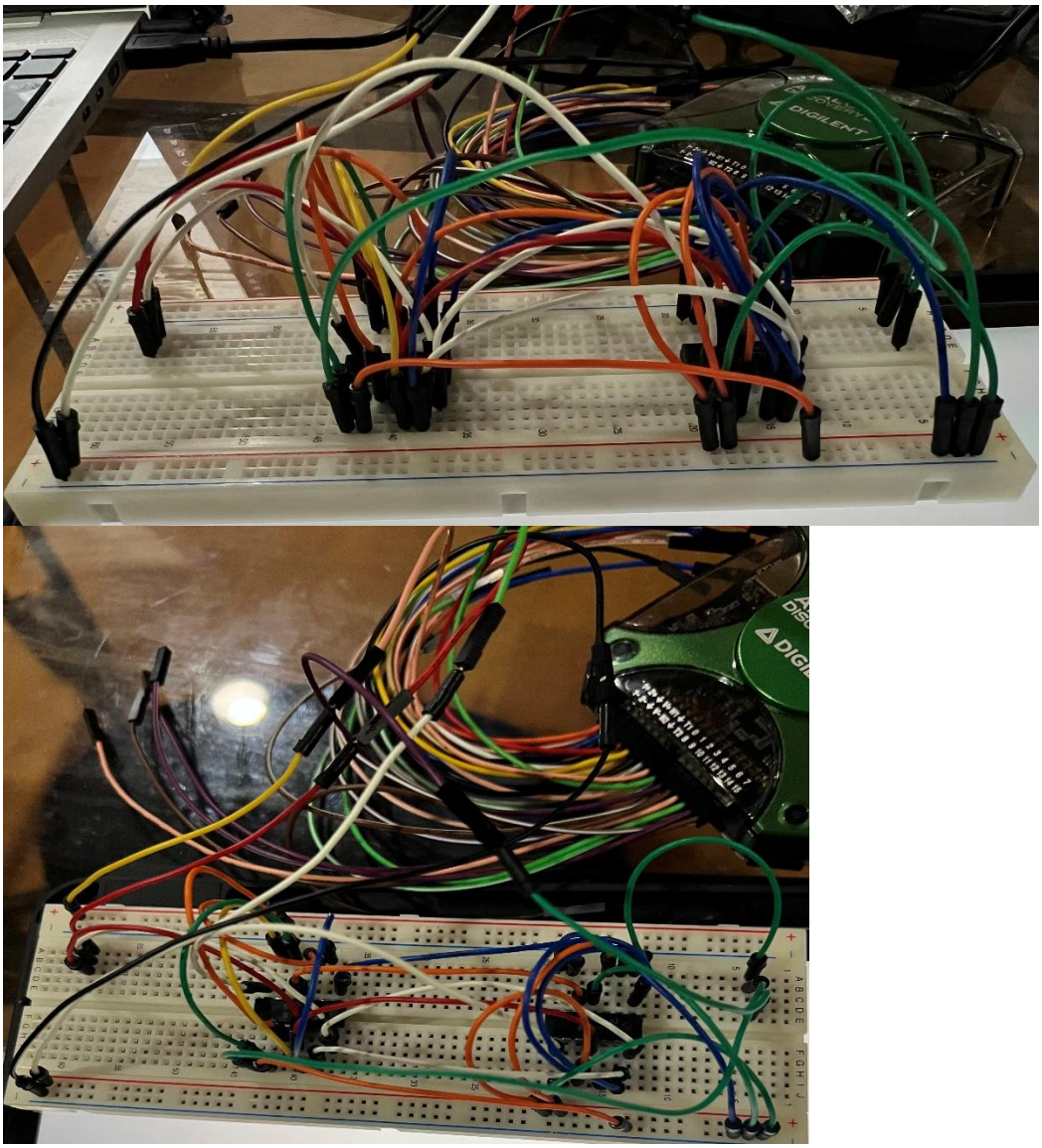


Figure 3: Physical circuit

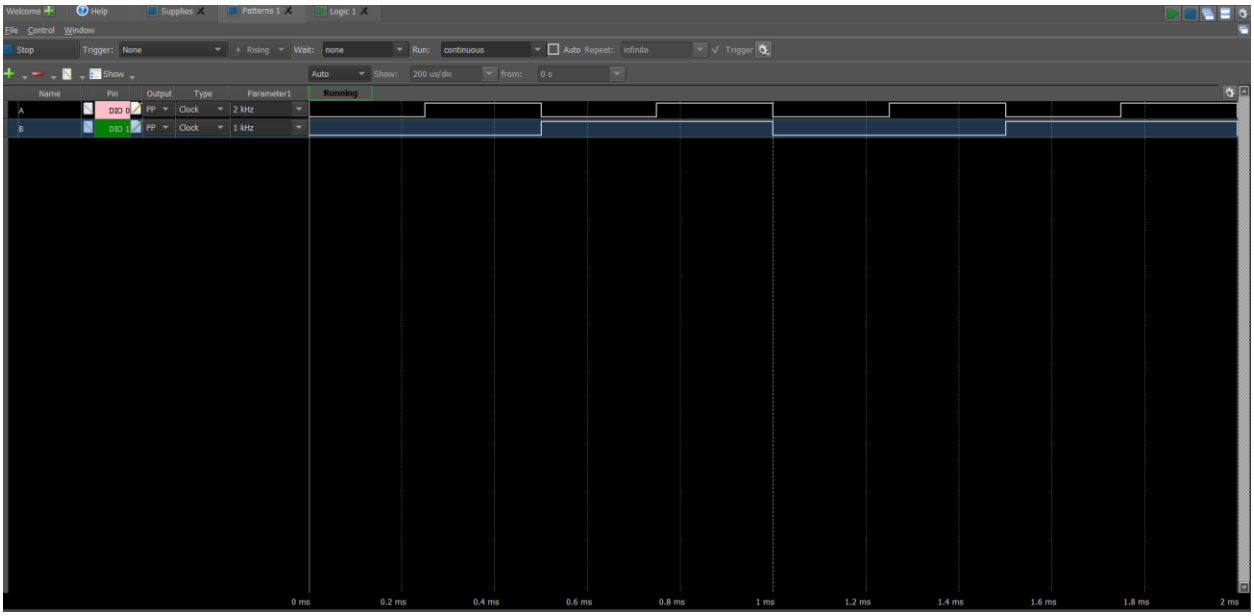


Figure 4: Patterns generation

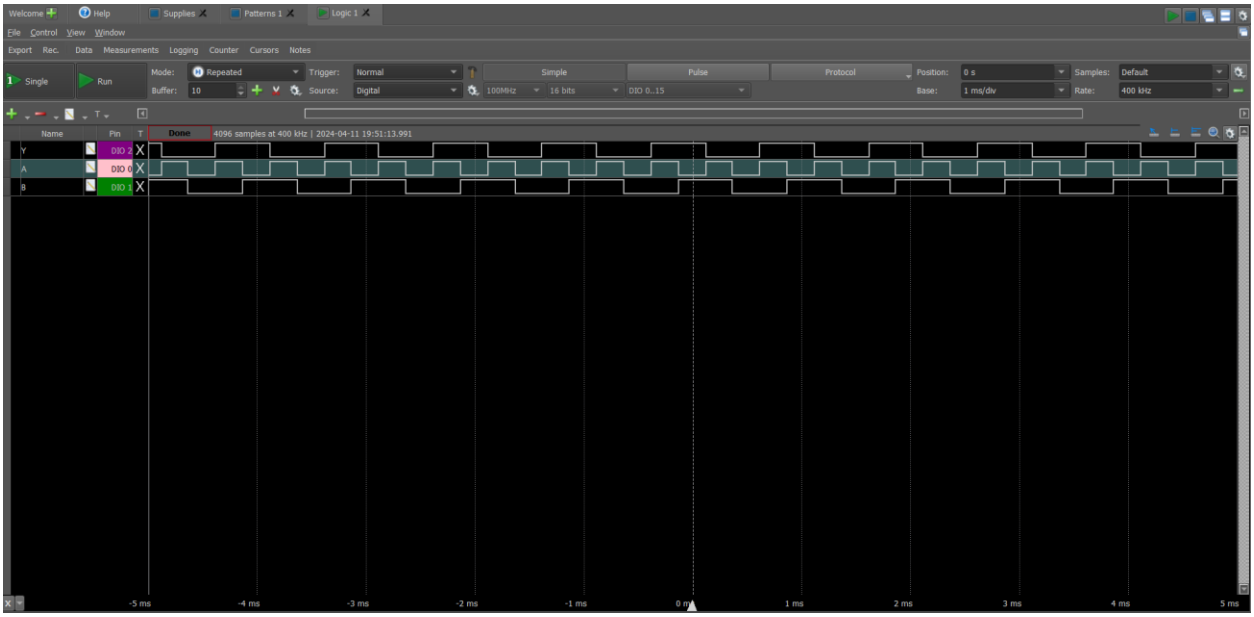


Figure 5: Logic analyzer output

So, the output Y is 0 when A and B are same (0,0 and 1,1) but when one of A and B is high (1) and other is low (0) the output Y is 1. This is the functionality of an XOR gate.

Static Testing

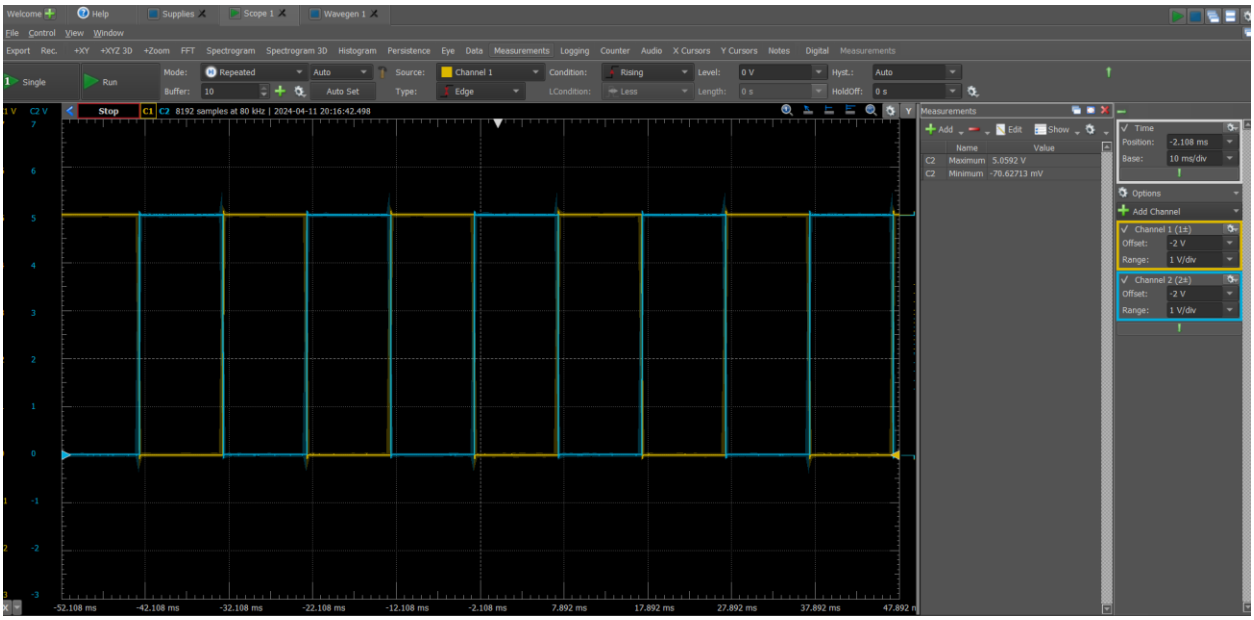


Figure 6: oscilloscope output

In the above oscilloscope A is 5V DC supply and B is a square wave of frequency 50Hz and going from 0V to 5V. The oscilloscope channel 1 (yellow) is B and channel 2 (blue) is the output Y.

The input A is always a DC value of 5V from the supply so when the input B is made a square wave that alternates between 0V and 5V, we get approximate values of V_L= 0V and V_H = 5.05 V as seen from the maximum and minimum measurement.

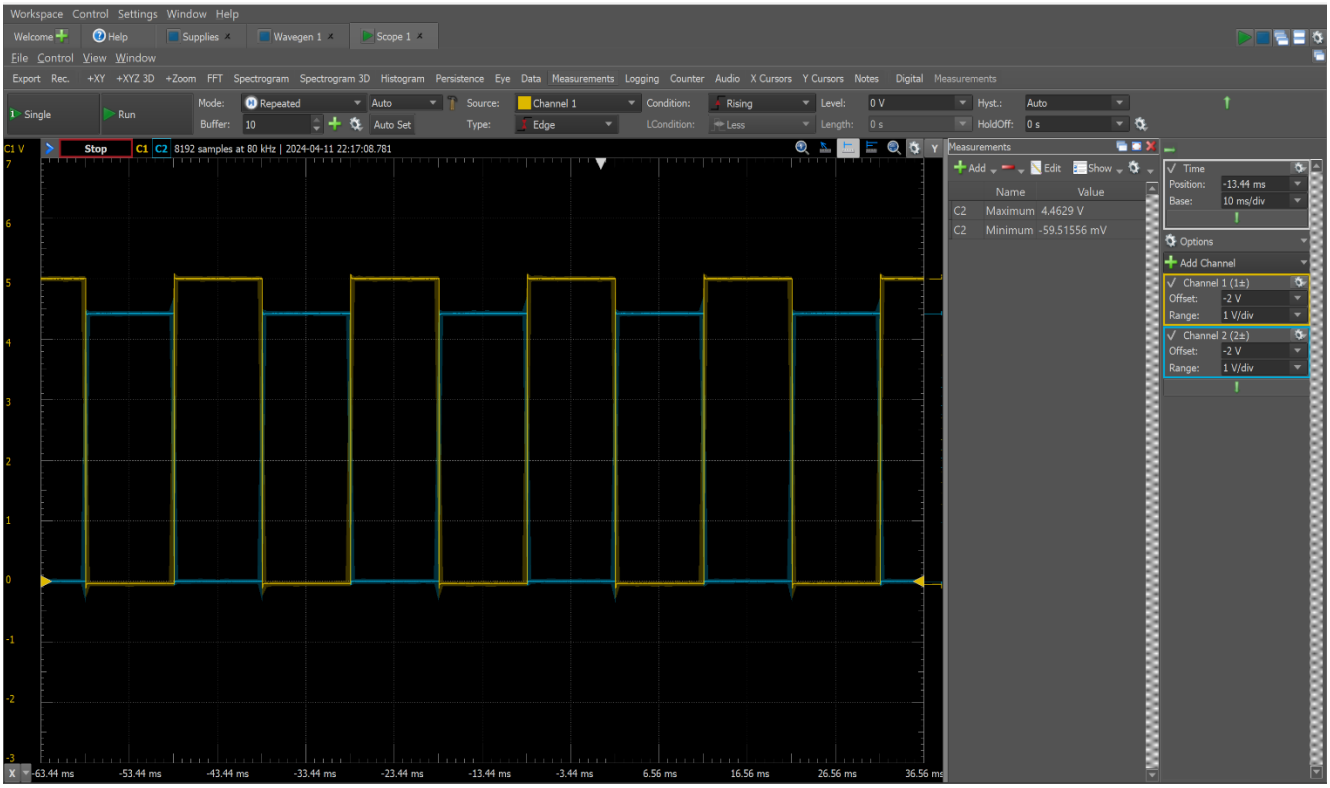


Figure 7: Oscilloscope results when inputs are switched

When the inputs are switched the channel 1 of oscilloscope represents A and B is a constant DC value of 5V. V_L is approximately 0 V and V_H is 4.46 V which is very similar to the output when the inputs were how we initially connected the inputs. The V_L and V_H values can still be used to represent a logic low and a logic high respectively.

Timing

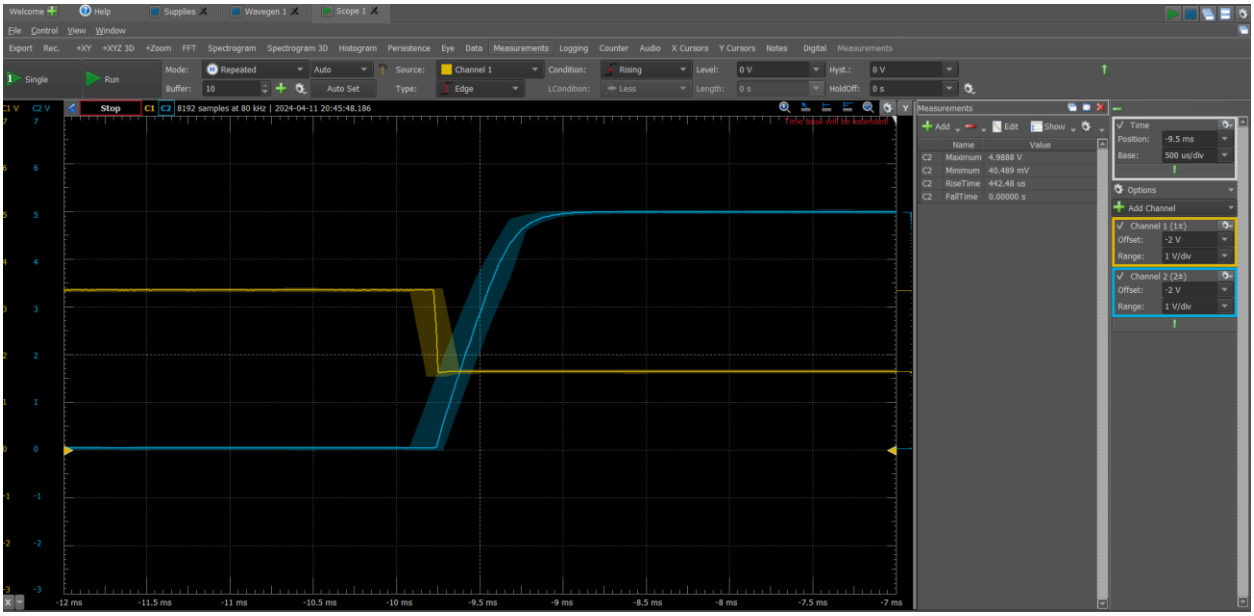


Figure 8: Rise time

As we can see, Rise time = 442.48 microseconds

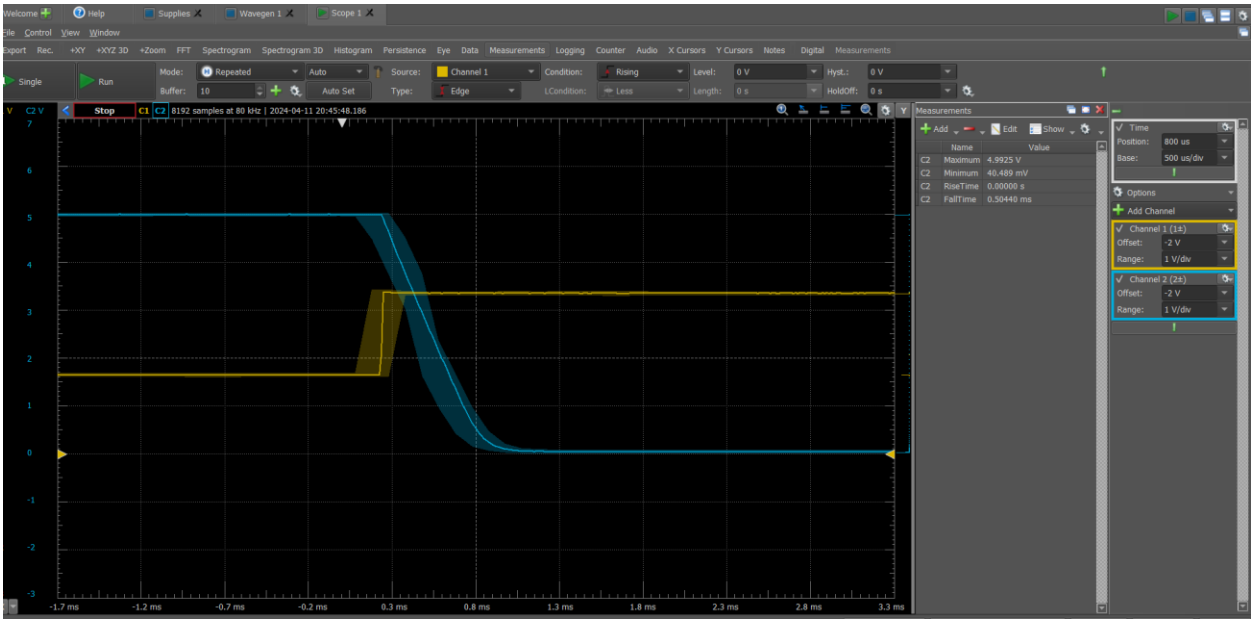
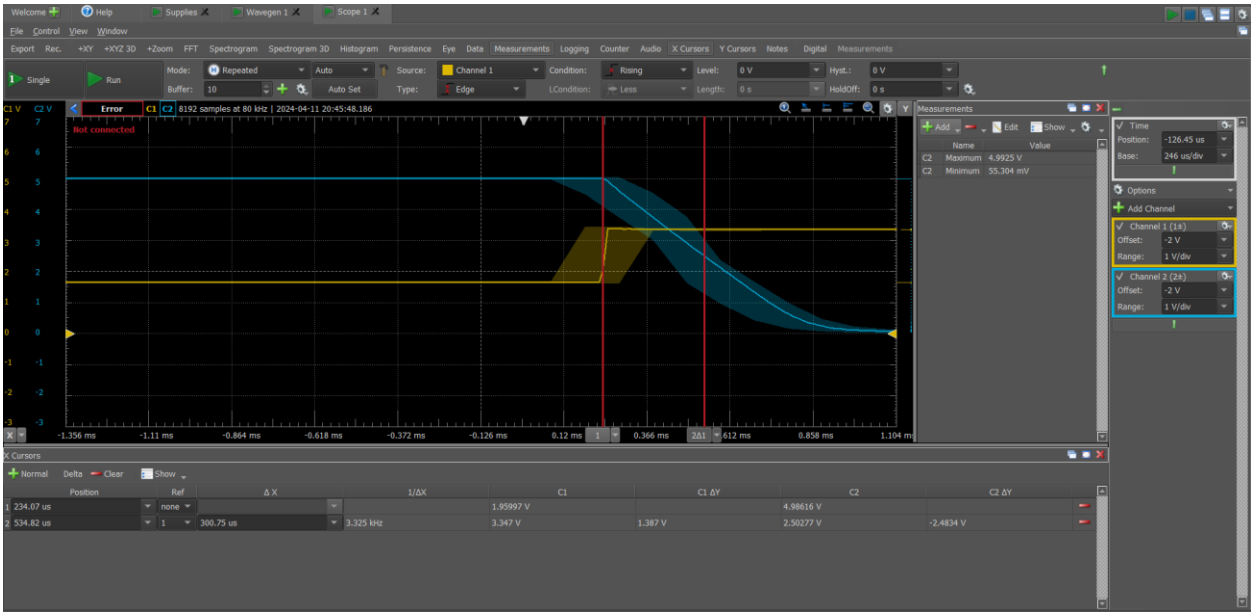
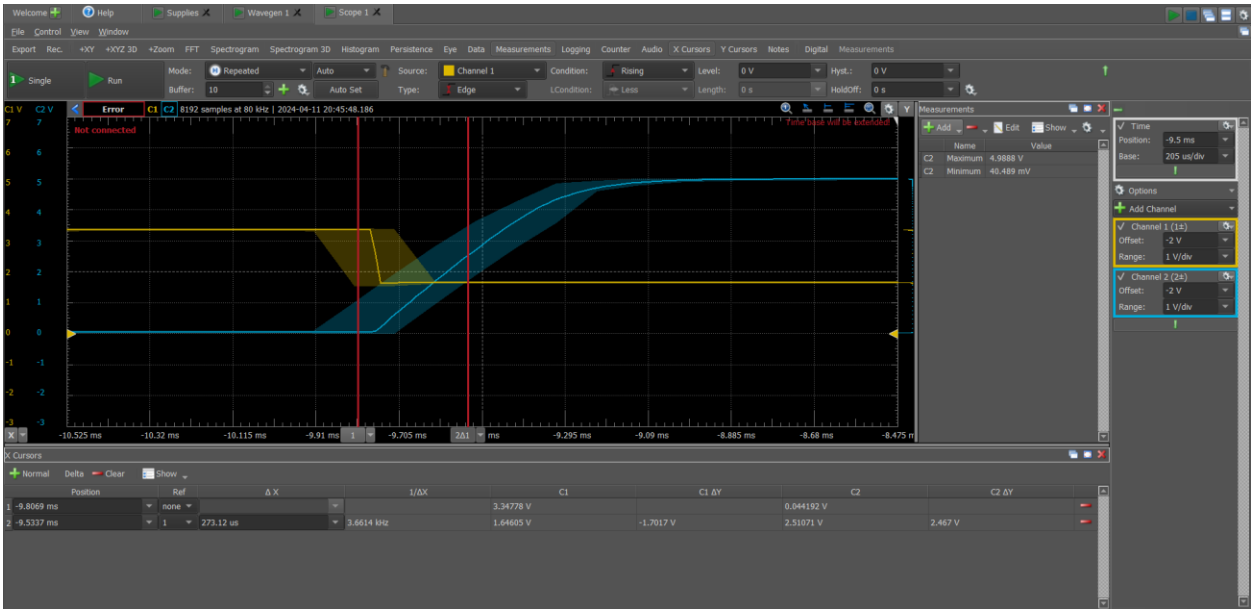


Figure 9: Fall time

As we can see, Fall time = 0.504 milliseconds



As we can see τ_{PHL} = 300.75 microseconds.



As we can see τ_{PLH} = 273.12 microseconds.

The values were measure using the normal cursor and the delta cursor by reading the difference in x values.

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2} = 286.935 \text{ microseconds}$$