Memory : 16x8 bit

AR, PC, DR, AC,INPR,OUTR : 4 Bit

IR : 8 Bit

**Instruction List**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Fetch** | T0: | | AR ←PC | |
| T1: | | IR ← M[AR], PC ← PC + 1 | |
| **Decode** | T2: | | DO...D15 ← Decode IR(4 - 7),  AR ← IR(0 – 3) | |
| **Memory Reference** | | | | |
| **AND** | D0T3 | | | DR ← M[AR] |
| d0t4 | | | AC ←AC ˄ DR, SC ← 0 |
| **ADD** | D1T3 | | | DR ← M[AR] |
| D1T4 | | | AC ←AC + DR, E ← Cout, SC ← 0 |
| **LDA** | D2T3 | | | DR ← M[AR] |
| D2T4 | | | AC ← DR, SC ← 0 |
| **STA** | D3T3 | | | M[AR] ←AC, SC ←0 |
| **BUN** | D4T3 | | | PC ←AR, SC ←0 |
| **BSA** | D5T3 | | | M[AR] ← PC, AR ← AR + 1 |
| D5T4 | | | PC ←AR, SC ←0 |
| **RET** | D6T3 | | | PC ← M[AR], SC ← 0 |
| **Register-Reference** | | | | |
| **CLA** | | D7T3: | | AC ←0 |
| **CLE** | | D8T3: | | E←0 |
| **CMA** | | D9T3: | | AC ←AC' |
| **INC** | | D10T3: | | AC ←AC + 1 |
| **CIR** | | D11T3: | | AC ← shr AC, AC(3) ← E, E ← AC(0) |
| **CIL** | | D12T3: | | AC ← shl AC, AC(0) ← E, E ←AC(3) |
| **INP** | | D13T3: | | AC ← INPR |
| **OUT** | | D14T3: | | OUTR ← AC |
| **HLT** | | D15T3: | | S←0 |