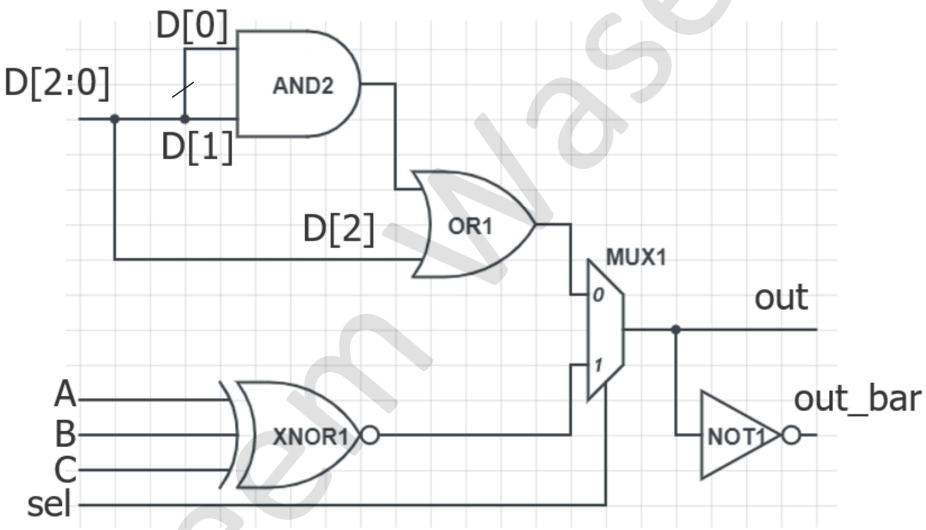
Combinational Circuit Design

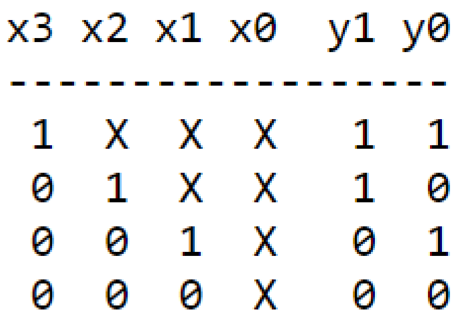
Design the following circuits using Verilog **and create a testbench (directed or randomized)** for each design to check its functionality.

1)

- The design has 5 inputs and 2 outputs
- Randomize the stimulus in the testbench and make sure that the output is correct from the waveform

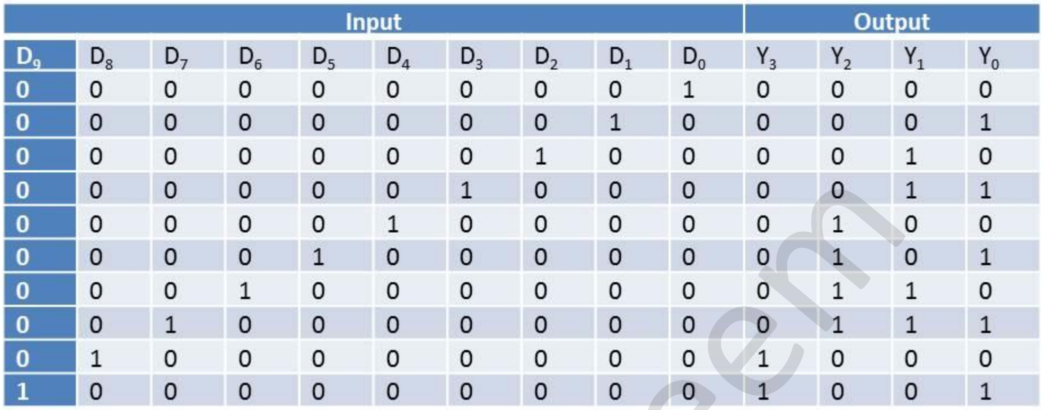


2) Design a 4-bit priority encoder, the following truth table is provided where x is 4-bit input and y is a 2-bit output. Randomize the stimulus in the testbench and add an expected result y in your testbench code and make the testbench self-checking.



x3	x2	x1	x0	y1	y0
1	X	X	X	1	1
0	1	X	X	1	0
0	0	1	X	0	1
0	0	0	X	0	0

3) Design a decimal to BCD “Binary Coded Decimal” encoder has 10 input lines D0 to D9 and 4 output lines Y0 to Y3 . Below is the truth table for a decimal to BCD encoder. Output should be held LOW if none of the following input patterns is observed. Randomize the stimulus in the testbench and add an expected result y in your testbench code and make the testbench self-checking.



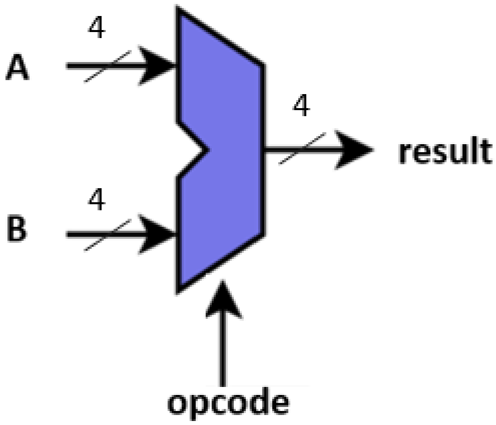
Input										Output			
D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	1	0	0	0	0	1	0
0	0	0	0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	0	0	1	0	1
0	0	0	1	0	0	0	0	0	0	0	1	1	0
0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	1	0	0	0	0	0	0	0	0	1	0	0	0
1	0	0	0	0	0	0	0	0	0	1	0	0	1

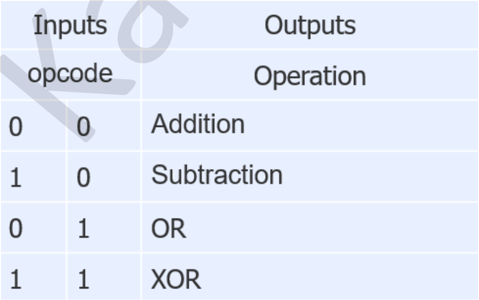
4) Implement N-bit adder using Dataflow modeling style

- The design takes 2 inputs (A, B) and the summation is assigned to output (C) ignoring the carry.
- Parameter N has default value = 1.
- Randomize the stimulus in the testbench and add an expected result y in your testbench code and make the testbench self-checking.

5) Design N-bit ALU that perform the following operations

- The design has 3 inputs and 1 output
- Instantiate the half adder from the previous design to implement the addition operation of the ALU
- For the subtraction, subtract B from A “A – B”
- Parameter N has default value = 4.
- Randomize the stimulus in the testbench and add an expected result y in your testbench code and make the testbench self-checking.



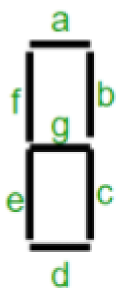


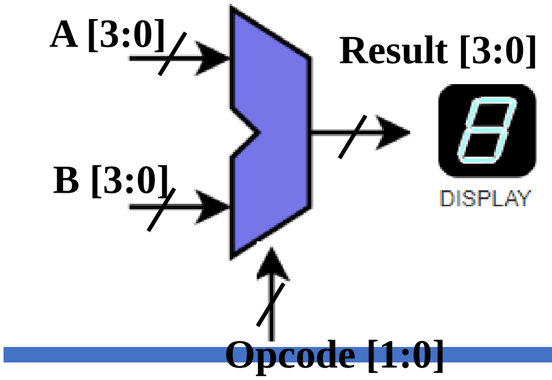
Inputs		Outputs
opcode		Operation
0	0	Addition
1	0	Subtraction
0	1	OR
1	1	XOR

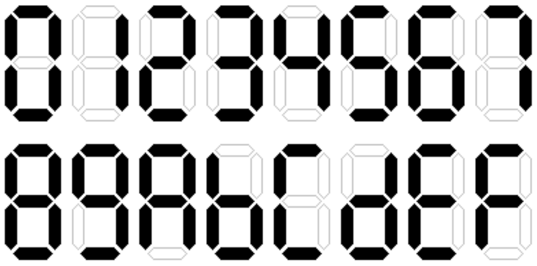
6) Implement 4-bit ALU display on 7 Segment LED Display

- The design has 4 inputs: A, B, opcode, enable.
- The design has 7 outputs (a-g)
- Instantiate the N-bit ALU designed in the previous design with parameter N = 4
- ALU should execute the operation on A and B depending on the input opcode
- ALU output should be considered as the digit to be displayed on the 7 segment LED display
- Below the truth table of the 7-segment decoder
- Since we have verified the ALU and Adder, we need to make sure that the outputs a to g are correct. Write 16 directed test vectors to exercise all the below digits with enable input equals to 1 then one directed test vector to drive the enable to 0. Make the testbench self-checking.

	Input	Output						
Digit	enable	a	b	c	d	e	f	g
0	1	1	1	1	1	1	1	0
1	1	0	1	1	0	0	0	0
2	1	1	1	0	1	1	0	1
3	1	1	1	1	1	0	0	1
4	1	0	1	1	0	0	1	1
5	1	1	0	1	1	0	1	1
6	1	1	0	1	1	1	1	1
7	1	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1	1
9	1	1	1	1	1	0	1	1
A	1	1	1	1	0	1	1	1
b	1	0	0	1	1	1	1	1
C	1	1	0	0	1	1	1	0
d	1	0	1	1	1	1	0	1
E	1	1	0	0	1	1	1	1
F	1	1	0	0	0	1	1	1
x	0	0	0	0	0	0	0	0







7-segment decoder

Deliverables:

1) The assignment should be submitted as a PDF file with this format <your_name>_Assignment2 for example Kareem_Waseem_Assignment2
2) Snippets from the waveforms captured from QuestaSim for each design with inputs assigned values and output values visible

Note that your document should be organized as 6 sections corresponding to each design above, and in each section, I am expecting the Verilog code for the design, testbench and the waveforms snippets