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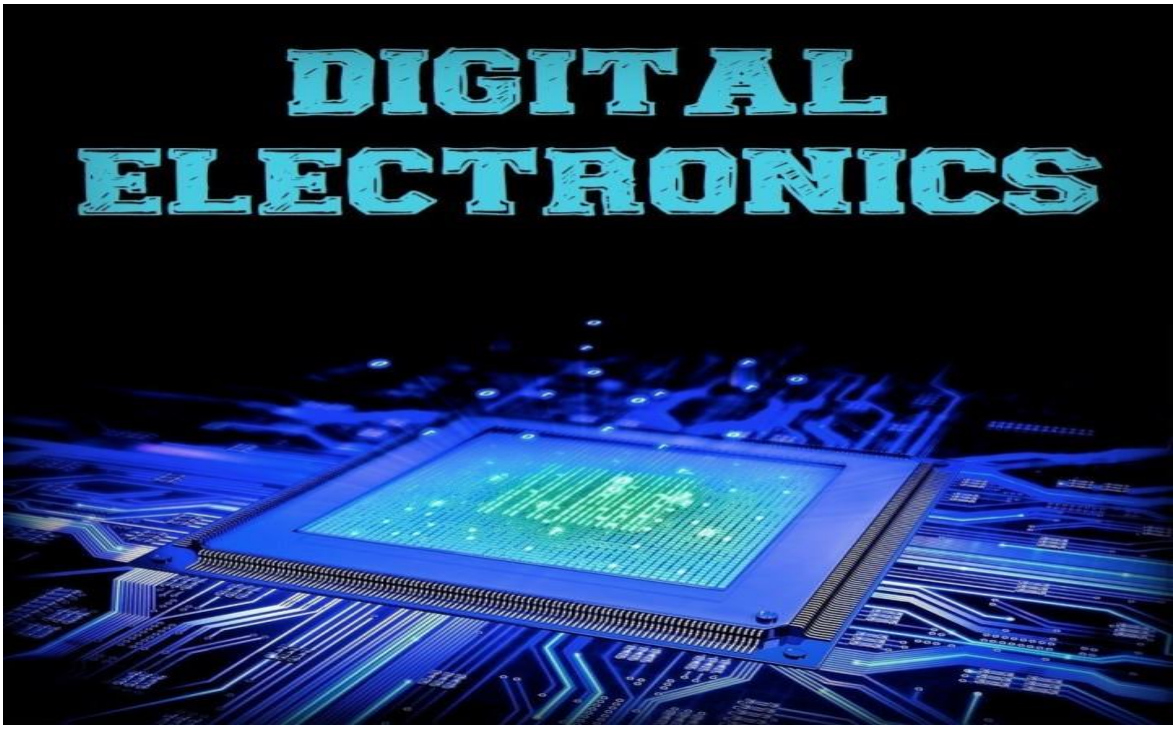
Spartan6-DSP48A1



[Q1]

The code of reg_mux module:

```
module reg_mux(data,rst,ce,clk,out);
 parameter WIDTH=18;
 parameter RSTTYPE = "SYNC";//SYNC or ASYNC
 parameter REGISTER_ENABLE=1;//1 or 0
 input [WIDTH-1:0] data;
 input clk,rst,ce;
 output  [WIDTH-1:0] out;
 reg [WIDTH-1:0] out_sync,out_async;

 always @(posedge clk ) begin
    if (RSTTYPE!="ASYNC") begin //default SYNC
        if(rst)
            out_sync<=0;
        else if(ce)
            out_sync<=data;
    end
 end
 always @(posedge clk or posedge rst) begin
    if (RSTTYPE=="ASYNC") begin
        if(rst)
            out_async<=0;
        else if(ce)
            out_async<=data;
    end
 end
assign out =(REGISTER_ENABLE&&RSTTYPE=="ASYNC")?out_async:(REGISTER_ENABLE&&RSTTYPE!="ASYNC")?out_sync:data ;
endmodule
```

The main module code:

```
module Spartan6_DSP48A1
#(
   parameter A0REG = 0,// if 1(register) ,0(no register)
             A1REG = 1,
             B0REG = 0,
             B1REG = 1,
             CREG = 1,
             DREG = 1,
             MREG = 1,
             PREG = 1,
             CARRYINREG = 1,
             CARRYOUTREG = 1,
             OPMODEREG = 1,
             CARRYINSEL = "OPMODE5",//CARRYIN or OPMODE5 else out=0
             B_INPUT = "DIRECT",//DIRECT or CASCADE
             RSTTYPE = "SYNC"//SYNC or ASYNC
)
(
 input [17:0] A,B,D,BCIN,
 input [47:0] C,PCIN,
 input [7:0] OPMODE,
 input CLK,CARRYIN,
 input RSTA, RSTB, RSTM, RSTP, RSTC, RSTD, RSTCARRYIN, RSTOPMODE,
 input CEA, CEB, CEM, CEP, CEC, CED, CECARRYIN, CEOPMODE,
  output [17:0] BCOUT,
  output [47:0] PCOUT,P,
  output [35:0] M,
  output CARRYOUT, CARRYOUTF
);
  wire [17:0] A0_m, A1_m, B0_m,B1_m,D_m,B0_in,B1_in,pre_adder_out;
  wire [47:0] C_m,Post_adder_out;
  wire [35:0] M_m,mult_out;
  wire [7:0] OPMODE_m;
  wire CYI_in,CYI_m,CYO_in;
  reg [47:0] X_m,Z_m;

  reg_mux #(18,RSTTYPE,A0REG)  A0_REG(A,RSTA,CEA,CLK,A0_m);
  reg_mux #(18,RSTTYPE,A1REG)  A1_REG(A0_m,RSTA,CEA,CLK,A1_m);
  reg_mux #(18,RSTTYPE,B0REG)  B0_REG(B0_in,RSTB,CEB,CLK,B0_m);
  reg_mux #(18,RSTTYPE,B1REG)  B1_REG(B1_in,RSTB,CEB,CLK,B1_m);
  reg_mux #(48,RSTTYPE,CREG)  C_REG(C,RSTC,CEC,CLK,C_m);
  reg_mux #(18,RSTTYPE,DREG)  D_REG(D,RSTD,CED,CLK,D_m);
  reg_mux #(36,RSTTYPE,MREG)  M_REG(mult_out,RSTM,CEM,CLK,M_m);
  reg_mux #(48,RSTTYPE,PREG)  P_REG(Post_adder_out,RSTP,CEP,CLK,P);
  reg_mux #(1,RSTTYPE,CARRYINREG)  CYI_REG(CYI_in,RSTCARRYIN,CECARRYIN,CLK,CYI_m);
  reg_mux #(1,RSTTYPE,CARRYOUTREG)  CYO_REG(CYO_in,RSTCARRYIN,CECARRYIN,CLK,CARRYOUT);
  reg_mux #(8,RSTTYPE,OPMODEREG)  OPMODE_REG(OPMODE,RSTOPMODE,CEOPMODE,CLK,OPMODE_m);

  assign CYI_in=(CARRYINSEL=="OPMODE5")?OPMODE_m[5]:(CARRYINSEL=="CARRYIN")?CARRYIN:0;

  assign B0_in=(B_INPUT=="DIRECT")?B:(B_INPUT=="CASCADE")?BCIN:0;
```

```
    reg_mux #(18,RSTTYPE,B1REG)  B1_REG(B1_in,RSTB,CEB,CLK,B1_m);
    reg_mux #(48,RSTTYPE,CREG)  C_REG(C,RSTC,CEC,CLK,C_m);
    reg_mux #(18,RSTTYPE,DREG)  D_REG(D,RSTD,CED,CLK,D_m);
    reg_mux #(36,RSTTYPE,MREG)  M_REG(mult_out,RSTM,CEM,CLK,M_m);
    reg_mux #(48,RSTTYPE,PREG)  P_REG(Post_adder_out,RSTP,CEP,CLK,P);
    reg_mux #(1,RSTTYPE,CARRYINREG)  CYI_REG(CYI_in,RSTCARRYIN,CECARRYIN,CLK,CYI_m);
    reg_mux #(1,RSTTYPE,CARRYOUTREG)  CYO_REG(CYO_in,RSTCARRYIN,CECARRYIN,CLK,CARRYOUT);
    reg_mux #(8,RSTTYPE,OPMODEREG)  OPMODE_REG(OPMODE,RSTOPMODE,CEOPMODE,CLK,OPMODE_m);

    assign CYI_in=(CARRYINSEL=="OPMODE5")?OPMODE_m[5]:(CARRYINSEL=="CARRYIN")?CARRYIN:0;

    assign B0_in=(B_INPUT=="DIRECT")?B:(B_INPUT=="CASCADE")?BCIN:0;

    assign  pre_adder_out=(OPMODE_m[6]==0)?(D_m+B0_m):(D_m-B0_m);

    assign  B1_in=(OPMODE_m[4]==1)?pre_adder_out:B0_m ;

    assign BCOUT = B1_m;

    assign  mult_out=A1_m*B1_m;

    assign  M = M_m;


  always @(*) begin
    case(OPMODE_m[1:0])
      0:X_m=0;
      1:X_m=M_m;
      2:X_m=P;
      3:X_m={D_m[11:0],A1_m[17:0],B1_m[17:0]};
    endcase
  end
   always @(*) begin
    case(OPMODE_m[3:2])
      0:Z_m=0;
      1:Z_m=PCIN;
      2:Z_m=P;
      3:Z_m=C_m;
    endcase
  end
  assign {CYO_in,Post_adder_out}=(OPMODE_m[7]==0)?(X_m+Z_m+CYI_m):(Z_m-(X_m+CYI_m));
  assign CARRYOUTF = CARRYOUT ;
  assign PCOUT = P ;
endmodule
```

The testbench code:

```
module DSP_tb();
 localparam A0REG = 0;// if 1(register) ,0(no register)
 localparam A1REG = 1;
 localparam B0REG = 0;
 localparam B1REG = 1;
 localparam CREG = 1;
 localparam DREG = 1;
 localparam MREG = 1;
 localparam PREG = 1;
 localparam CARRYINREG = 1;
 localparam CARRYOUTREG = 1;
 localparam OPMODEREG = 1;
 localparam CARRYINSEL = "OPMODE5";//CARRYIN or OPMODE5 else out=0
 localparam B_INPUT = "DIRECT";//DIRECT or CASCADE
 localparam RSTTYPE = "SYNC";//SYNC or ASYNC

 reg [17:0] A,B,D,BCIN;
 reg [47:0] C,PCIN;
 reg [7:0] OPMODE;
 reg CLK,CARRYIN;
 reg RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE;
 reg CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE;
 wire [17:0] BCOUT;
 wire [47:0] PCOUT,P;
 wire [35:0] M;
 wire CARRYOUT,CARRYOUTF;

 Spartan6_DSP48A1 #(A0REG,A1REG,B0REG,B1REG,CREG,DREG,MREG,PREG,CARRYINREG,CARRYOUTREG,OPMODEREG,CARRYINSEL,B_INPUT,RSTTYPE) dut(
    A,B,D,BCIN,C,PCIN,OPMODE,CLK,CARRYIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
 initial begin
    CLK=0;
    forever
        #1 CLK=~CLK;
 end
integer i;
initial begin
// Initialize and reset signals
    RSTA = 1; RSTB = 1; RSTM = 1; RSTP = 1; RSTC = 1; RSTD = 1; RSTCARRYIN = 1; RSTOPMODE = 1;
    CEA = 1; CEB = 1; CEM = 1; CEP = 1; CEC = 1; CED = 1; CECARRYIN = 1; CEOPMODE = 1;
    A = 0; B = 0; C = 0; D = 0; CARRYIN = 0; BCIN = 0; PCIN = 0;
    OPMODE = 8'b00000000;
    repeat(5)
     @(negedge CLK);

    // put reset signal =1
    RSTA = 0; RSTB = 0; RSTM = 0; RSTP = 0; RSTC = 0; RSTD = 0; RSTCARRYIN = 0; RSTOPMODE = 0;
    $display("Case : 1");
    //B*A+C+opmode[5] =(15*2)+10+1=41
    OPMODE=8'b01101101;
    A=15;B=2;C=10;
    repeat(5)
```

```
49          OPMODE=8'b01101101;
50          A=15;B=2;C=10;
51          repeat(5)
52          @(negedge CLK);
53
54          $display("Case : 2");
55          //C-((D-B)*A)=1000-((13-3)*10)=900
56          OPMODE=8'b11011101;
57          D=13;B=3;A=10;C=1000;
58          repeat(5)
59          @(negedge CLK);
60
61          $display("Case : 3");
62          //X_m=P,Z_m=P:x+z=900+900=1800
63          OPMODE=8'b01011010;
64          repeat(2)
65          @(negedge CLK);
66
67          $display("Case : 4");
68          //P=PCIN=12345;
69          OPMODE=8'b01010100;
70          PCIN=12345;
71          repeat(2)
72          @(negedge CLK);
73
74          $display("Case : 5");
75          //(D+B)*A=(3+2)*5=25
76          OPMODE=8'b00010001;
77          D=3;B=2;A=5;
78          repeat(5)
79          @(negedge CLK);
80
81          $display("Case : 6");
82          //Output equal the concatinated numbe
83          //=10_1010_1010_0101_0101_1010_1010_1010_0101_0101_1010_1010_1010_0101_0101
84          OPMODE = 8'b00010011;
85          D=18'b1010_1010_1010_0101_0101;
86          B=0;
87          A=18'b1010_1010_1010_0101_0101;
88          repeat(5)
89          @(negedge CLK);
90          $display("P=%b",P);
91
92          $display("Case : 7");
93          //Note the output from subtracter will be N_num so the out will be big num
94          OPMODE=8'b11011111;
95          B=47;
96          A=33;
97          C=47;
98          D=30;
99          PCIN=7;
100         repeat(5)
```

```
    D=18'b1010_1010_1010_0101_0101;
    B=0;
    A=18'b1010_1010_1010_0101_0101;
    repeat(5)
    @(negedge CLK);
    $display("P=%b",P);

    $display("Case : 7");
    //Note the output from subtracter will be N_num so the out will be big num
    OPMODE=8'b11011111;
    B=47;
    A=33;
    C=47;
    D=30;
    PCIN=7;
    repeat(5)
    @(negedge CLK);

    $display("PCIN+M_m+CIN,M_m=(D+B)*A ,so P=PCIN+(D+B)*A+CIN");
    OPMODE = 8'b00110101;
    for(i=0;i<5;i=i+1) begin
        $display("iteration : %d",i);
        A=$urandom_range(1,50);
        B=$urandom_range(1,50);
        D=$urandom_range(1,50);
        PCIN=$urandom_range(1,50);
        repeat(5)
        @(negedge CLK);
    end

    $display("Randomize cases");
    for(i=0;i<1000;i=i+1) begin
        A = $urandom_range(1, 50);
        B = $urandom_range(1, 50);
        D = $urandom_range(1, 50);
        C = $urandom_range(1, 50);
        PCIN = $urandom_range(1, 50);
        OPMODE = $random;
        repeat(5)
        @(negedge CLK);

    end

    $stop;
end

initial begin
    $monitor("A=%d, B=%d, C=%d, D=%d, CARRYIN=%d ,PCIN=%d , OPMODE=%b, P=%d,BCOUT=%d ,M=%d ,CARRYOUT=%d", A, B, C, D,CARRYIN ,PCIN , OPMODE, P,BCOUT ,M , CARRYOUT);
end
endmodule
```

The do file code:

```
vlib work

vlog Spartan6_DSP48A1.v reg_mux.v DSP_tb.v

vsim -voptargs=+acc DSP_tb

add wave *

run -all

#quit -sim
```

The constraint file:

```
create_debug_core u_ila_0 ila
set_property ALL_PROBE_SAME_MU true [get_debug_cores u_ila_0]
set_property ALL_PROBE_SAME_MU_CNT 1 [get_debug_cores u_ila_0]
set_property C_ADV_TRIGGER false [get_debug_cores u_ila_0]
set_property C_DATA_DEPTH 1024 [get_debug_cores u_ila_0]
set_property C_EN_STRG_QUAL false [get_debug_cores u_ila_0]
set_property C_INPUT_PIPE_STAGES 0 [get_debug_cores u_ila_0]
set_property C_TRIGIN_EN false [get_debug_cores u_ila_0]
set_property C_TRIGOUT_EN false [get_debug_cores u_ila_0]
set_property port_width 1 [get_debug_ports u_ila_0/clk]
connect_debug_port u_ila_0/clk [get_nets [list CLK_IBUF_BUFG]]
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe0]
set_property port_width 18 [get_debug_ports u_ila_0/probe0]
connect_debug_port u_ila_0/probe0 [get_nets [list {B_IBUF[0]} {B_IBUF[1]} {B_IBUF[2]} {B_IBUF[3]} {B_IB
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe1]
set_property port_width 48 [get_debug_ports u_ila_0/probe1]
connect_debug_port u_ila_0/probe1 [get_nets [list {C_IBUF[0]} {C_IBUF[1]} {C_IBUF[2]} {C_IBUF[3]} {C_IB
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe2]
set_property port_width 18 [get_debug_ports u_ila_0/probe2]
connect_debug_port u_ila_0/probe2 [get_nets [list {BCOUT_OBUF[0]} {BCOUT_OBUF[1]} {BCOUT_OBUF[2]} {BCOU
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe3]
set_property port_width 18 [get_debug_ports u_ila_0/probe3]
connect_debug_port u_ila_0/probe3 [get_nets [list {A_IBUF[0]} {A_IBUF[1]} {A_IBUF[2]} {A_IBUF[3]} {A_IB
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe4]
set_property port_width 18 [get_debug_ports u_ila_0/probe4]
connect_debug_port u_ila_0/probe4 [get_nets [list {D_IBUF[0]} {D_IBUF[1]} {D_IBUF[2]} {D_IBUF[3]} {D_IB
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe5]
set_property port_width 36 [get_debug_ports u_ila_0/probe5]
connect_debug_port u_ila_0/probe5 [get_nets [list {M_OBUF[0]} {M_OBUF[1]} {M_OBUF[2]} {M_OBUF[3]} {M_OB
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe6]
set_property port_width 8 [get_debug_ports u_ila_0/probe6]
connect_debug_port u_ila_0/probe6 [get_nets [list {OPMODE_IBUF[0]} {OPMODE_IBUF[1]} {OPMODE_IBUF[2]} {O
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe7]
set_property port_width 48 [get_debug_ports u_ila_0/probe7]
connect_debug_port u_ila_0/probe7 [get_nets [list {PCIN_IBUF[0]} {PCIN_IBUF[1]} {PCIN_IBUF[2]} {PCIN_IB
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe8]
set_property port_width 48 [get_debug_ports u_ila_0/probe8]
connect_debug_port u_ila_0/probe8 [get_nets [list {P_OBUF[0]} {P_OBUF[1]} {P_OBUF[2]} {P_OBUF[3]} {P_OB
create_debug_port u_ila_0 probe
set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe9]
set_property port_width 1 [get_debug_ports u_ila_0/probe9]
connect_debug_port u_ila_0/probe9 [get_nets [list CARRYOUTF_OBUF]]
```

```
209    set_property port_width 1 [get_debug_ports u_ila_0/probe9]
210    connect_debug_port u_ila_0/probe9 [get_nets [list CARRYOUTF_OBUF]]
211    create_debug_port u_ila_0 probe
212    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe10]
213    set_property port_width 1 [get_debug_ports u_ila_0/probe10]
214    connect_debug_port u_ila_0/probe10 [get_nets [list CEA_IBUF]]
215    create_debug_port u_ila_0 probe
216    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe11]
217    set_property port_width 1 [get_debug_ports u_ila_0/probe11]
218    connect_debug_port u_ila_0/probe11 [get_nets [list CEB_IBUF]]
219    create_debug_port u_ila_0 probe
220    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe12]
221    set_property port_width 1 [get_debug_ports u_ila_0/probe12]
222    connect_debug_port u_ila_0/probe12 [get_nets [list CEC_IBUF]]
223    create_debug_port u_ila_0 probe
224    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe13]
225    set_property port_width 1 [get_debug_ports u_ila_0/probe13]
226    connect_debug_port u_ila_0/probe13 [get_nets [list CECARRYIN_IBUF]]
227    create_debug_port u_ila_0 probe
228    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe14]
229    set_property port_width 1 [get_debug_ports u_ila_0/probe14]
230    connect_debug_port u_ila_0/probe14 [get_nets [list CED_IBUF]]
231    create_debug_port u_ila_0 probe
232    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe15]
233    set_property port_width 1 [get_debug_ports u_ila_0/probe15]
234    connect_debug_port u_ila_0/probe15 [get_nets [list CEM_IBUF]]
235    create_debug_port u_ila_0 probe
236    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe16]
237    set_property port_width 1 [get_debug_ports u_ila_0/probe16]
238    connect_debug_port u_ila_0/probe16 [get_nets [list CEOPMODE_IBUF]]
239    create_debug_port u_ila_0 probe
240    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe17]
241    set_property port_width 1 [get_debug_ports u_ila_0/probe17]
242    connect_debug_port u_ila_0/probe17 [get_nets [list CEP_IBUF]]
243    create_debug_port u_ila_0 probe
244    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe18]
245    set_property port_width 1 [get_debug_ports u_ila_0/probe18]
246    connect_debug_port u_ila_0/probe18 [get_nets [list CLK_IBUF]]
247    create_debug_port u_ila_0 probe
248    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe19]
249    set_property port_width 1 [get_debug_ports u_ila_0/probe19]
250    connect_debug_port u_ila_0/probe19 [get_nets [list RSTA_IBUF]]
251    create_debug_port u_ila_0 probe
252    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe20]
253    set_property port_width 1 [get_debug_ports u_ila_0/probe20]
254    connect_debug_port u_ila_0/probe20 [get_nets [list RSTB_IBUF]]
255    create_debug_port u_ila_0 probe
256    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe21]
257    set_property port_width 1 [get_debug_ports u_ila_0/probe21]
258    connect_debug_port u_ila_0/probe21 [get_nets [list RSTC_IBUF]]
```

```
233    set_property port_width 1 [get_debug_ports u_ila_0/probe15]
234    connect_debug_port u_ila_0/probe15 [get_nets [list CEM_IBUF]]
235    create_debug_port u_ila_0 probe
236    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe16]
237    set_property port_width 1 [get_debug_ports u_ila_0/probe16]
238    connect_debug_port u_ila_0/probe16 [get_nets [list CEOPMODE_IBUF]]
239    create_debug_port u_ila_0 probe
240    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe17]
241    set_property port_width 1 [get_debug_ports u_ila_0/probe17]
242    connect_debug_port u_ila_0/probe17 [get_nets [list CEP_IBUF]]
243    create_debug_port u_ila_0 probe
244    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe18]
245    set_property port_width 1 [get_debug_ports u_ila_0/probe18]
246    connect_debug_port u_ila_0/probe18 [get_nets [list CLK_IBUF]]
247    create_debug_port u_ila_0 probe
248    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe19]
249    set_property port_width 1 [get_debug_ports u_ila_0/probe19]
250    connect_debug_port u_ila_0/probe19 [get_nets [list RSTA_IBUF]]
251    create_debug_port u_ila_0 probe
252    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe20]
253    set_property port_width 1 [get_debug_ports u_ila_0/probe20]
254    connect_debug_port u_ila_0/probe20 [get_nets [list RSTB_IBUF]]
255    create_debug_port u_ila_0 probe
256    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe21]
257    set_property port_width 1 [get_debug_ports u_ila_0/probe21]
258    connect_debug_port u_ila_0/probe21 [get_nets [list RSTC_IBUF]]
259    create_debug_port u_ila_0 probe
260    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe22]
261    set_property port_width 1 [get_debug_ports u_ila_0/probe22]
262    connect_debug_port u_ila_0/probe22 [get_nets [list RSTCARRYIN_IBUF]]
263    create_debug_port u_ila_0 probe
264    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe23]
265    set_property port_width 1 [get_debug_ports u_ila_0/probe23]
266    connect_debug_port u_ila_0/probe23 [get_nets [list RSTD_IBUF]]
267    create_debug_port u_ila_0 probe
268    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe24]
269    set_property port_width 1 [get_debug_ports u_ila_0/probe24]
270    connect_debug_port u_ila_0/probe24 [get_nets [list RSTM_IBUF]]
271    create_debug_port u_ila_0 probe
272    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe25]
273    set_property port_width 1 [get_debug_ports u_ila_0/probe25]
274    connect_debug_port u_ila_0/probe25 [get_nets [list RSTOPMODE_IBUF]]
275    create_debug_port u_ila_0 probe
276    set_property PROBE_TYPE DATA_AND_TRIGGER [get_debug_ports u_ila_0/probe26]
277    set_property port_width 1 [get_debug_ports u_ila_0/probe26]
278    connect_debug_port u_ila_0/probe26 [get_nets [list RSTP_IBUF]]
279    set_property C_CLK_INPUT_FREQ_HZ 300000000 [get_debug_cores dbg_hub]
280    set_property C_ENABLE_CLK_DIVIDER false [get_debug_cores dbg_hub]
281    set_property C_USER_SCAN_CHAIN 1 [get_debug_cores dbg_hub]
282    connect_debug_port dbg_hub/clk [get_nets CLK_IBUF_BUFG]
```

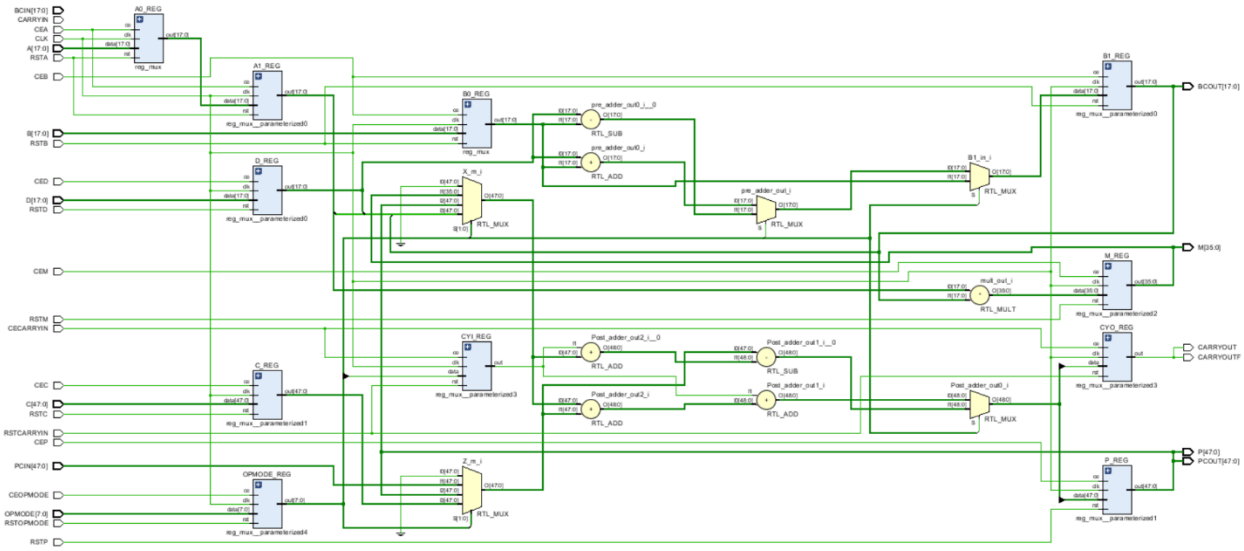
1-Elaboration (messages_tab)

Tcl Console | Messages | Log | Reports | Design Runs

Info (5) | Status (9) | Show All

- Vivado Commands (3 infos)
  - General Messages (3 infos)
    - [IP_Flow 19-234] Refreshing IP repositories
    - [IP_Flow 19-1704] No user IP repositories specified
    - [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Vivado/Vivado/2018.2/data/ip'.
- Elaborated Design (2 infos)
  - General Messages (2 infos)
    - [Project 1-570] Preparing netlist for logic optimization
    - [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

2-Elaboration(Schematic)



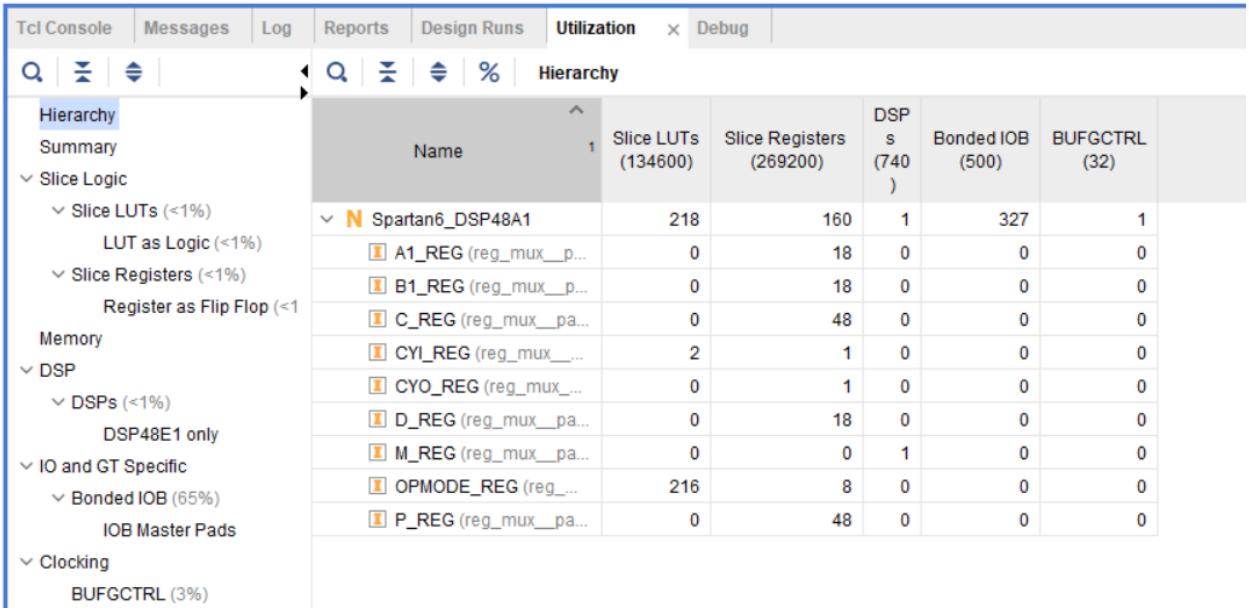
3-synthesis(messages_tab)

Tcl Console | Messages | Log | Reports | Design Runs

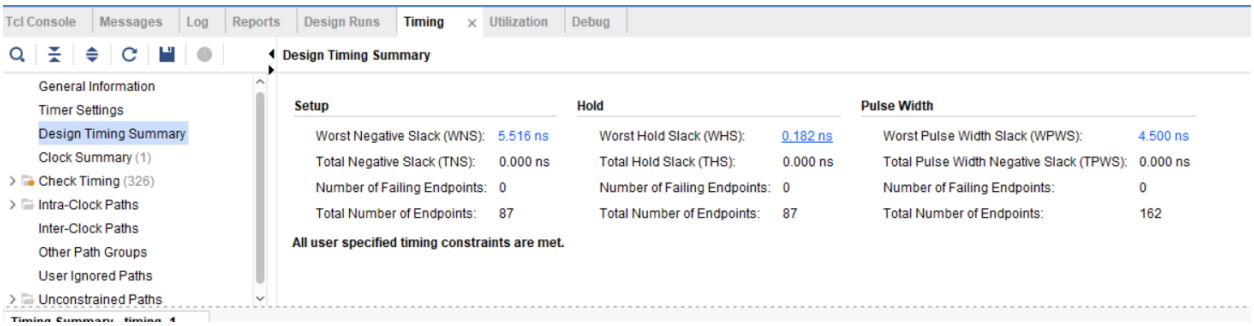
Warning (42) | Info (37) | Status (22) | Show All

- Synthesis (42 warnings)
  - [Synth 8-3331] design reg_mux has unconnected port rst (40 more like this)
  - [Constraints 18-5210] No constraint will be written out.

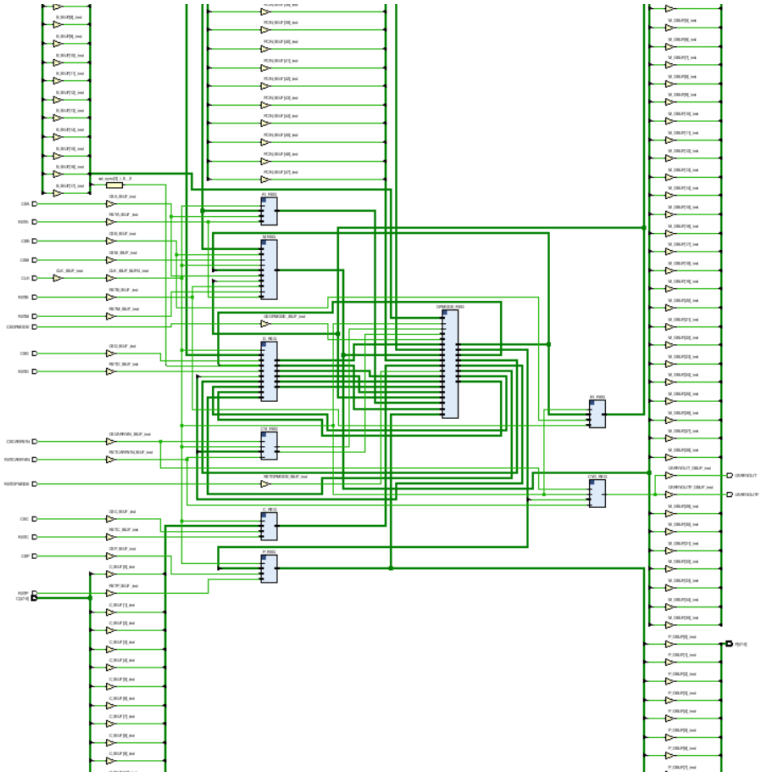
4-synthesis(Utilization_report)



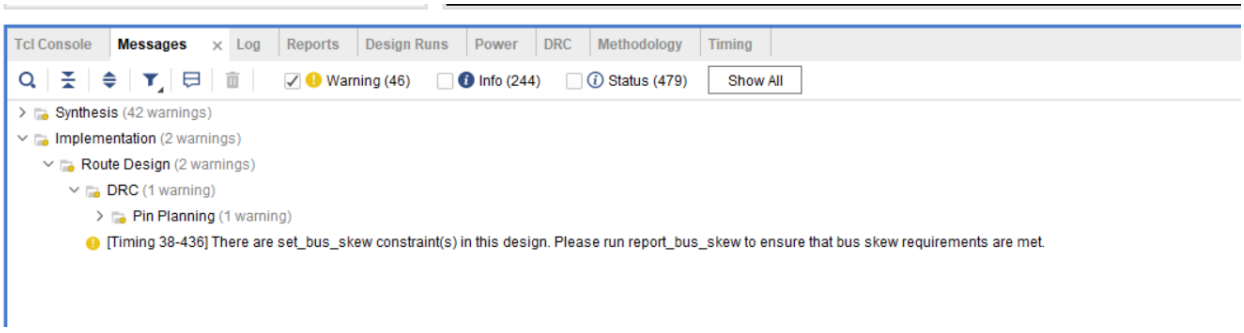
5-synthesis(Timing_report)



6-synthesis(Schematic)



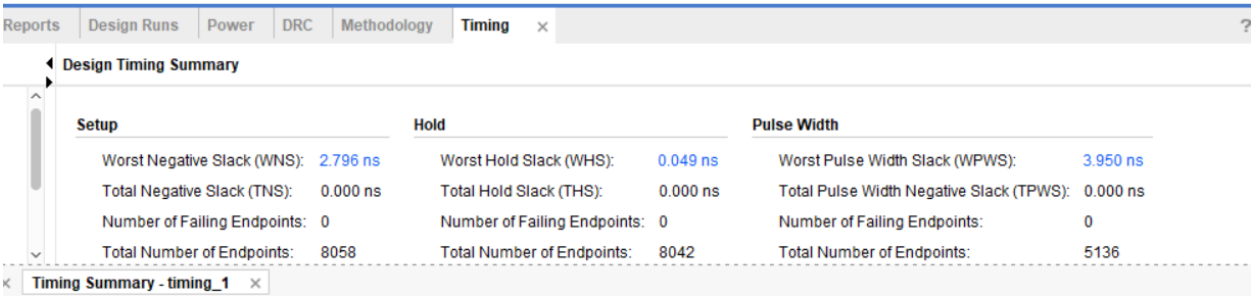
7-implmentation(messages_tab)



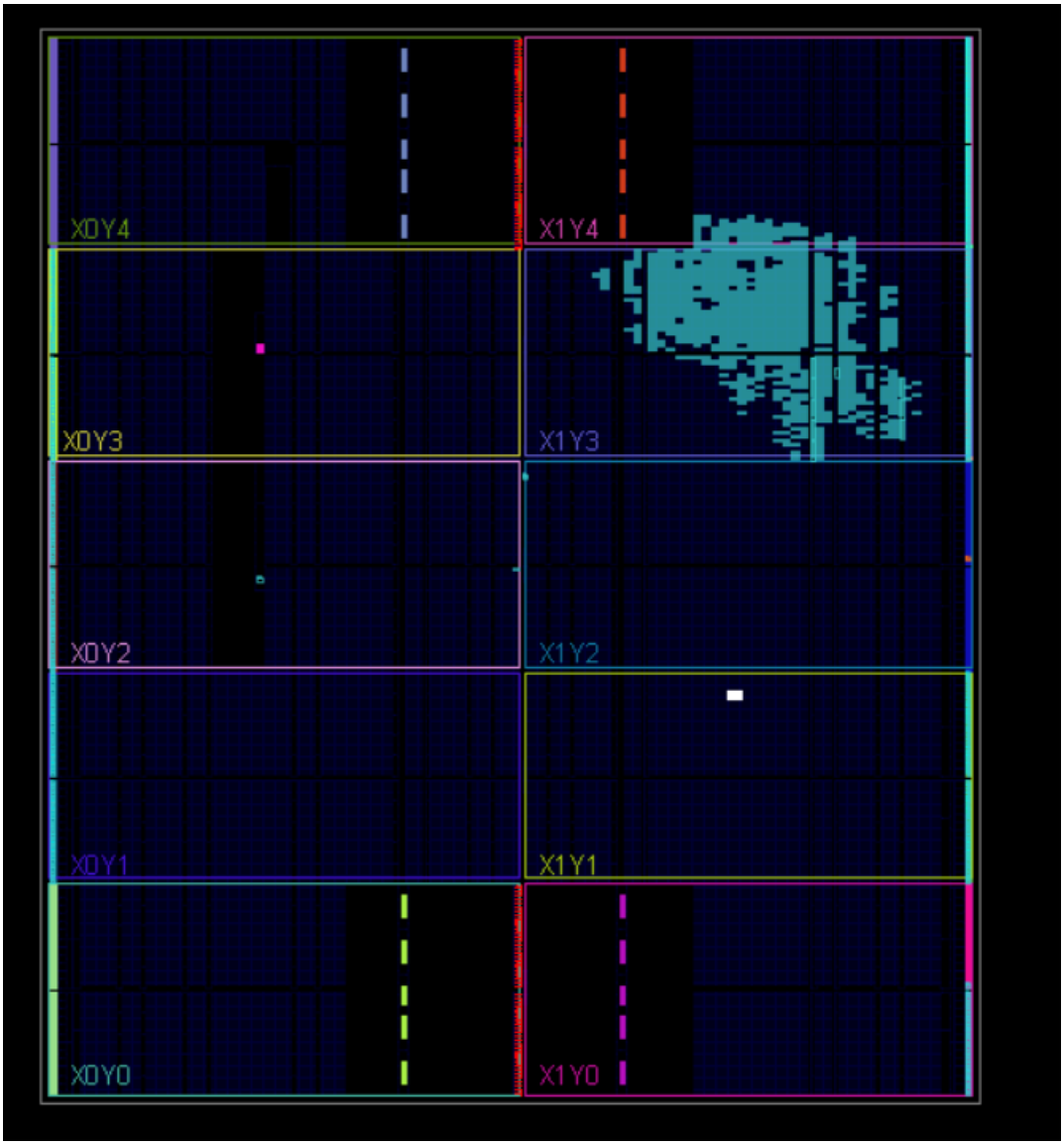
8-Implmentation(Utilization_report)

Name	Slice LUTs (133800)	Slice Registers (267600)	F7 Muxes (66900)	F8 Muxes (33450)	Slice (33450)	LUT as Logic (133800)	LUT as Memory (46200)	LUT Flip Flop Pairs (133800)	Block RAM Tile (365)	DSPs (740)	Bonded IOB (500)	BUFGCTRL (32)	BSCANE2 (4)
Spartan6_DSP48A1	2690	4225	97	12	1484	2216	474	1569	8	1	327	2	1
A1_REG (reg_mux__p...	0	18	0	0	7	0	0	0	0	0	0	0	0
B1_REG (reg_mux__p...	0	18	0	0	6	0	0	0	0	0	0	0	0
C_REG (reg_mux__pa...	0	48	0	0	15	0	0	0	0	0	0	0	0
CYI_REG (reg_mux__...	2	1	0	0	2	2	0	1	0	0	0	0	0
CYO_REG (reg_mux_...	0	1	0	0	1	0	0	0	0	0	0	0	0
D_REG (reg_mux__pa...	0	18	0	0	10	0	0	0	0	0	0	0	0
dbg_hub (dbg_hub)	476	727	0	0	254	452	24	301	0	0	0	1	1
M_REG (reg_mux__pa...	0	0	0	0	0	0	0	0	0	1	0	0	0
OPMODE_REG (reg_...	216	8	0	0	65	216	0	0	0	0	0	0	0
P_REG (reg_mux__pa...	0	48	0	0	12	0	0	0	0	0	0	0	0
u_ila_0 (u_ila_0)	1996	3338	97	12	1168	1546	450	1211	8	0	0	0	0

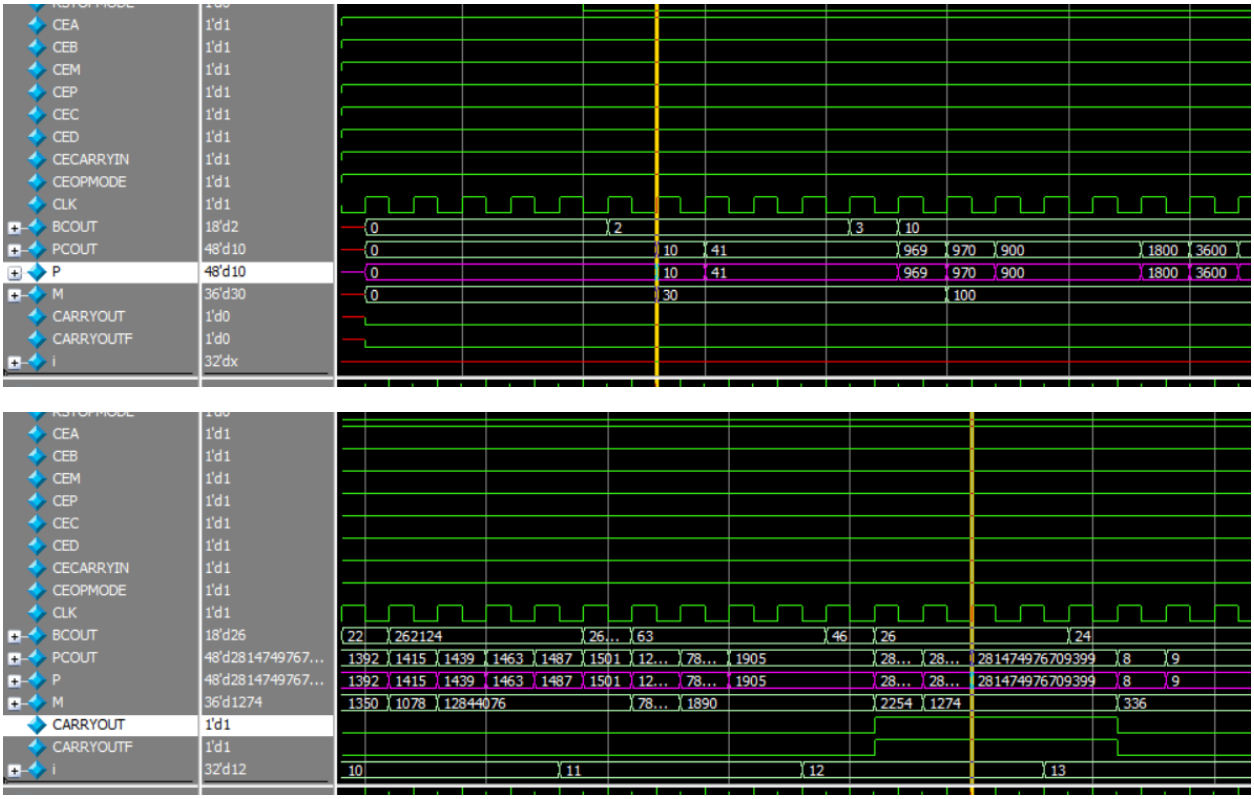
9-Implmentation(Timing_report)



10-Implmentation(device)



Some snippets from questa_sim:




```
# A=     0, B=     0, C=             0, D=     0, CARRYIN=0 ,PCIN=             0 , OPMODE=00000000, P=             x,BCOUT=     x ,M=          x ,CARRYOUT=x
# A=     0, B=     0, C=             0, D=     0, CARRYIN=0 ,PCIN=             0 , OPMODE=00000000, P=             0,BCOUT=     0 ,M=          0 ,CARRYOUT=0
# Case : 1
# A=    15, B=     2, C=            10, D=     0, CARRYIN=0 ,PCIN=             0 , OPMODE=01101101, P=             0,BCOUT=     0 ,M=          0 ,CARRYOUT=0
# A=    15, B=     2, C=            10, D=     0, CARRYIN=0 ,PCIN=             0 , OPMODE=01101101, P=             0,BCOUT=     2 ,M=          0 ,CARRYOUT=0
# A=    15, B=     2, C=            10, D=     0, CARRYIN=0 ,PCIN=             0 , OPMODE=01101101, P=            10,BCOUT=     2 ,M=         30 ,CARRYOUT=0
# A=    15, B=     2, C=            10, D=     0, CARRYIN=0 ,PCIN=             0 , OPMODE=01101101, P=            41,BCOUT=     2 ,M=         30 ,CARRYOUT=0
# Case : 2
# A=    10, B=     3, C=          1000, D=    13, CARRYIN=0 ,PCIN=             0 , OPMODE=11011101, P=            41,BCOUT=     2 ,M=         30 ,CARRYOUT=0
# A=    10, B=     3, C=          1000, D=    13, CARRYIN=0 ,PCIN=             0 , OPMODE=11011101, P=            41,BCOUT=     3 ,M=         30 ,CARRYOUT=0
# A=    10, B=     3, C=          1000, D=    13, CARRYIN=0 ,PCIN=             0 , OPMODE=11011101, P=           969,BCOUT=    10 ,M=         30 ,CARRYOUT=0
# A=    10, B=     3, C=          1000, D=    13, CARRYIN=0 ,PCIN=             0 , OPMODE=11011101, P=           970,BCOUT=    10 ,M=        100 ,CARRYOUT=0
# A=    10, B=     3, C=          1000, D=    13, CARRYIN=0 ,PCIN=             0 , OPMODE=11011101, P=           900,BCOUT=    10 ,M=        100 ,CARRYOUT=0
# Case : 3
# A=    10, B=     3, C=          1000, D=    13, CARRYIN=0 ,PCIN=             0 , OPMODE=01011010, P=           900,BCOUT=    10 ,M=        100 ,CARRYOUT=0
# A=    10, B=     3, C=          1000, D=    13, CARRYIN=0 ,PCIN=             0 , OPMODE=01011010, P=          1800,BCOUT=    10 ,M=        100 ,CARRYOUT=0
# Case : 4
# A=    10, B=     3, C=          1000, D=    13, CARRYIN=0 ,PCIN=         12345 , OPMODE=01010100, P=          1800,BCOUT=    10 ,M=        100 ,CARRYOUT=0
# A=    10, B=     3, C=          1000, D=    13, CARRYIN=0 ,PCIN=         12345 , OPMODE=01010100, P=          3600,BCOUT=    10 ,M=        100 ,CARRYOUT=0
# A=    10, B=     3, C=          1000, D=    13, CARRYIN=0 ,PCIN=         12345 , OPMODE=01010100, P=         12345,BCOUT=    10 ,M=        100 ,CARRYOUT=0
# Case : 5
# A=     5, B=     2, C=          1000, D=     3, CARRYIN=0 ,PCIN=         12345 , OPMODE=00010001, P=         12345,BCOUT=    10 ,M=        100 ,CARRYOUT=0
# A=     5, B=     2, C=          1000, D=     3, CARRYIN=0 ,PCIN=         12345 , OPMODE=00010001, P=         12345,BCOUT=    11 ,M=        100 ,CARRYOUT=0
# A=     5, B=     2, C=          1000, D=     3, CARRYIN=0 ,PCIN=         12345 , OPMODE=00010001, P=           100,BCOUT=     5 ,M=         55 ,CARRYOUT=0
# A=     5, B=     2, C=          1000, D=     3, CARRYIN=0 ,PCIN=         12345 , OPMODE=00010001, P=            55,BCOUT=     5 ,M=         25 ,CARRYOUT=0
# A=     5, B=     2, C=          1000, D=     3, CARRYIN=0 ,PCIN=         12345 , OPMODE=00010001, P=            25,BCOUT=     5 ,M=         25 ,CARRYOUT=0
# Case : 6
# A=174677, B=     0, C=          1000, D=174677, CARRYIN=0 ,PCIN=         12345 , OPMODE=00010011, P=            25,BCOUT=     5 ,M=         25 ,CARRYOUT=0
# A=174677, B=     0, C=          1000, D=174677, CARRYIN=0 ,PCIN=         12345 , OPMODE=00010011, P=            25,BCOUT=     3 ,M=         25 ,CARRYOUT=0
# A=174677, B=     0, C=          1000, D=174677, CARRYIN=0 ,PCIN=         12345 , OPMODE=00010011, P=181808806494211,BCOUT=174677 ,M=     524031 ,CARRYOUT=0
# A=174677, B=     0, C=          1000, D=174677, CARRYIN=0 ,PCIN=         12345 , OPMODE=00010011, P=181808806668885,BCOUT=174677 ,M=30512054329 ,CARRYOUT=0
# P=101001010101101010101001010101101010101001010101
# Case : 7
# A=    33, B=    47, C=            47, D=    30, CARRYIN=0 ,PCIN=             7 , OPMODE=11011111, P=181808806668885,BCOUT=174677 ,M=30512054329 ,CARRYOUT=0
# A=    33, B=    47, C=            47, D=    30, CARRYIN=0 ,PCIN=             7 , OPMODE=11011111, P=181808806668885,BCOUT=174724 ,M=30512054329 ,CARRYOUT=0
# A=    33, B=    47, C=            47, D=    30, CARRYIN=0 ,PCIN=             7 , OPMODE=11011111, P=279413383583147,BCOUT=262127 ,M=    5765892 ,CARRYOUT=1
# A=    33, B=    47, C=            47, D=    30, CARRYIN=0 ,PCIN=             7 , OPMODE=11011111, P=279413383495744,BCOUT=262127 ,M=    8650191 ,CARRYOUT=1
```