

Nucleo144 H7 SMPS with STLINK V3

MB1363

H755ZIQ

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Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.

▲ Notes to generate the board layout.

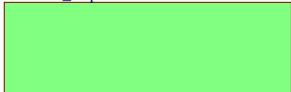
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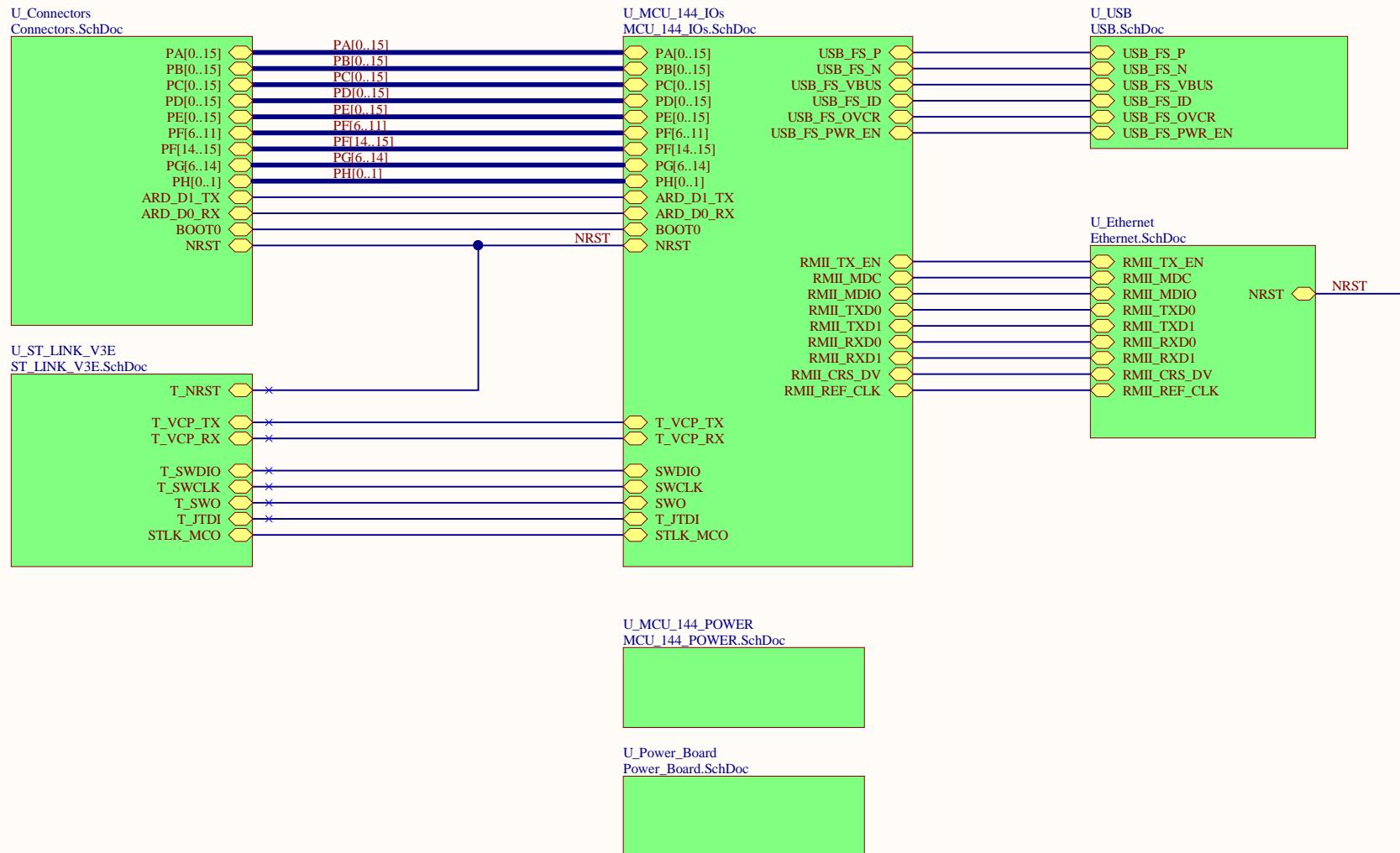
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U_MB1363_Top
MB1363_Top.SchDoc

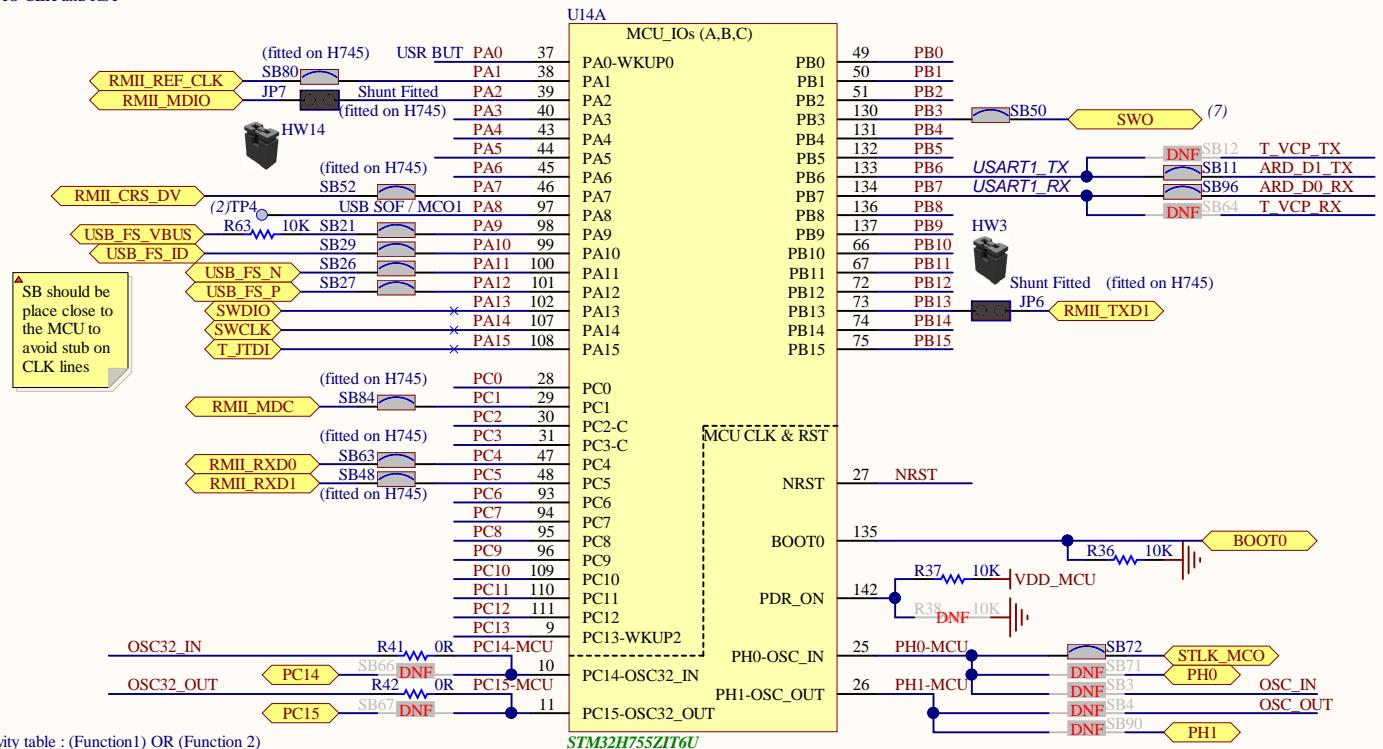


Title: Project overview	Project: Nucleo144 H7 SMPS with STLINK V3	Variant: H755ZIQ	Revision: D-01	Reference: MB1363	Size: A4	Date: 09-OCT-19	Sheet: 1 of 9
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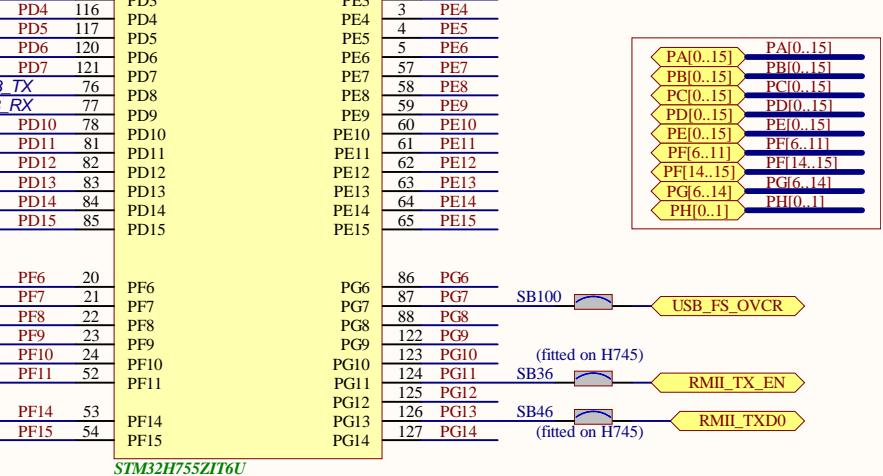
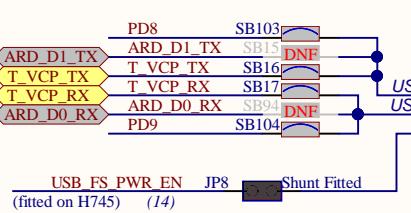




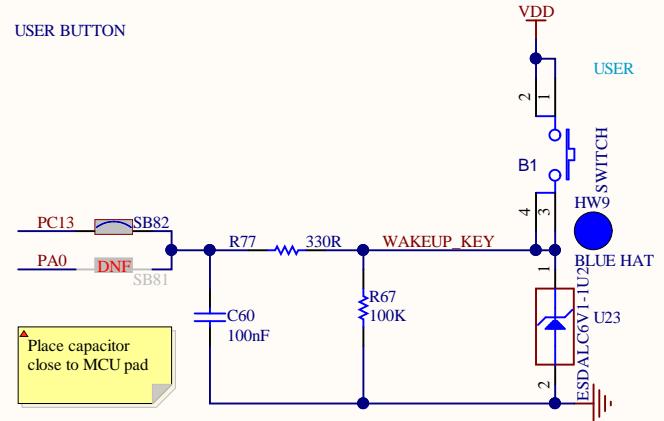
MCU IO CLK and RST



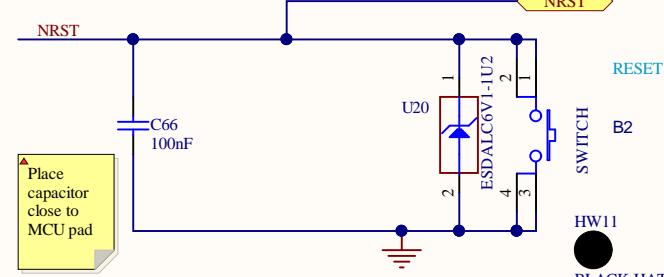
I/O	ARDUINO / ZIO	OTHER
(2)	PA8	D6
(5)	PA2	A8
(6)	PB13	D18
(7)	PB3	D23
(14)	PB10	D64
(15)	PB14	D65
		USB_SOF / MCO1
		RMII_MDIO
		RMII_TXD1
		SWO
		USB_FS_PWR_EN
		LED_RED



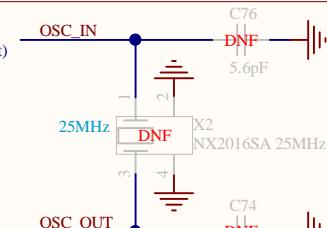
USER BUTTON



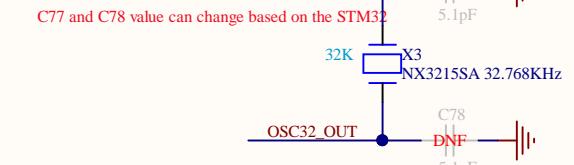
RESET FUNCTION



EXTERNAL HSE CLK (OPTIONAL : not fitted by default)



EXTERNAL LSE CLK



Title: MCU 144 I/Os

Project: Nucleo144 H7 SMPS with STLINK V3

Variant: H755ZIQ

Revision: D-01

Date: 09-OCT-19

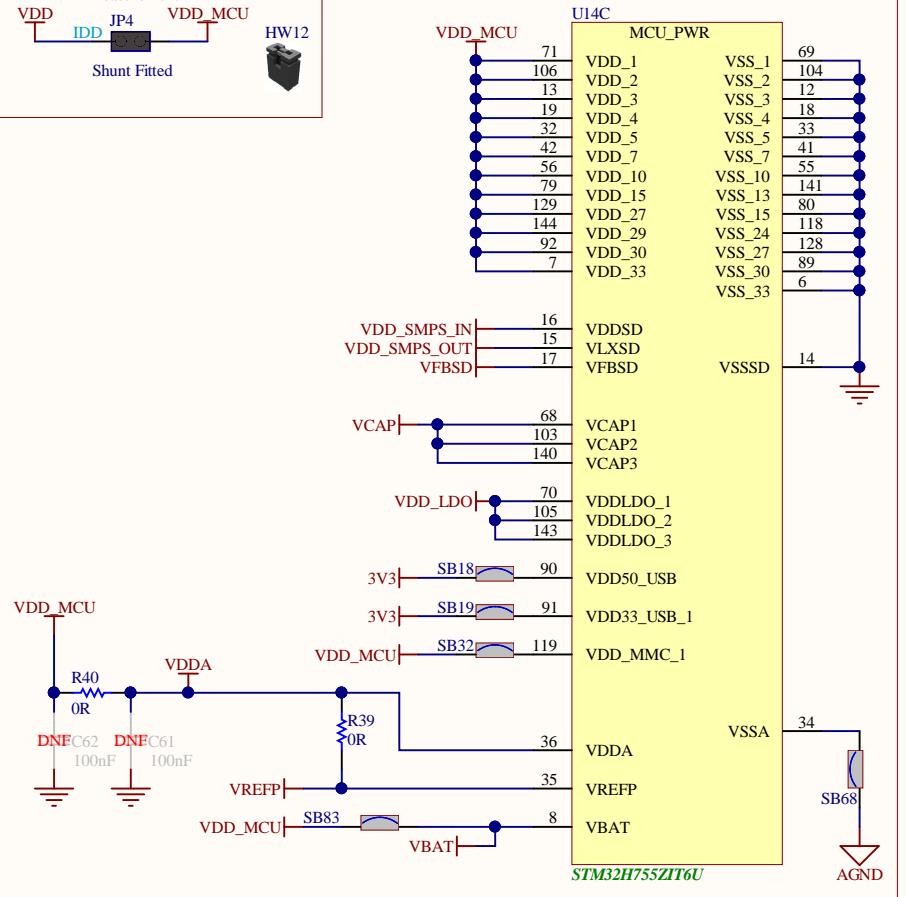
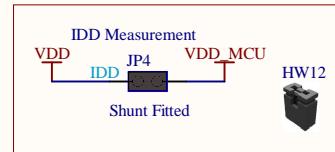
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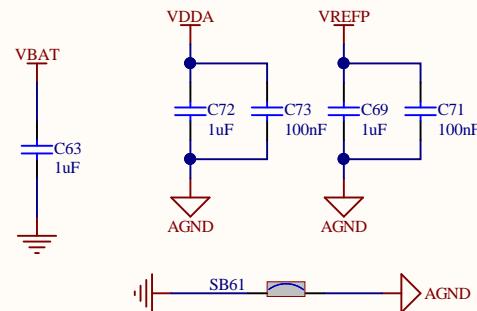
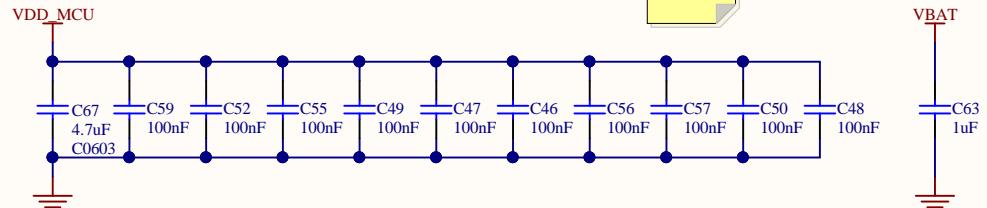


MCU PWR SUPPLIES



MCU DECAPS

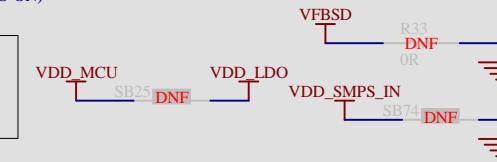
Ceramic capacitor (Low ESR, ESR<1ohm)



SMPS MCU Supply Config

Supply Config 1 : LDO only (SMPS OFF, LDO ON)

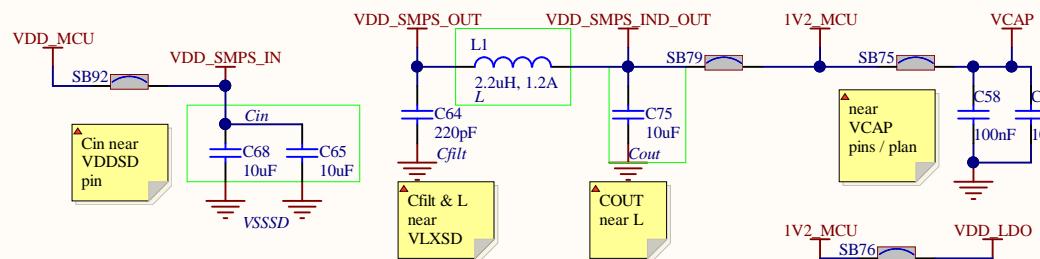
Disconnect 3V3_SMPS_IN from 3V3_MCU
Connect 3V3_SMPS_IN to GND
Connect VDD_SMPS_IND_OUT to GND
Connect VDD_LDO to 3V3_MCU
2x 2.2uF near VCAP pins/pins



Supply Config 2 : Internal SMPS only (SMPS ON, LDO OFF)

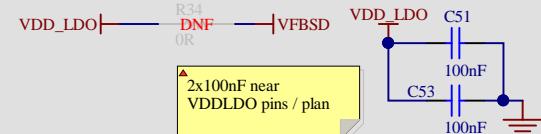
Default config

Connect VDD_SMPS_IN to VDD MCU
Connect VDD_SMPS_IND_OUT to VCAP1/2/3



Supply Config 3 : SMPS & LDO cascaded (SMPS & LDO ON)

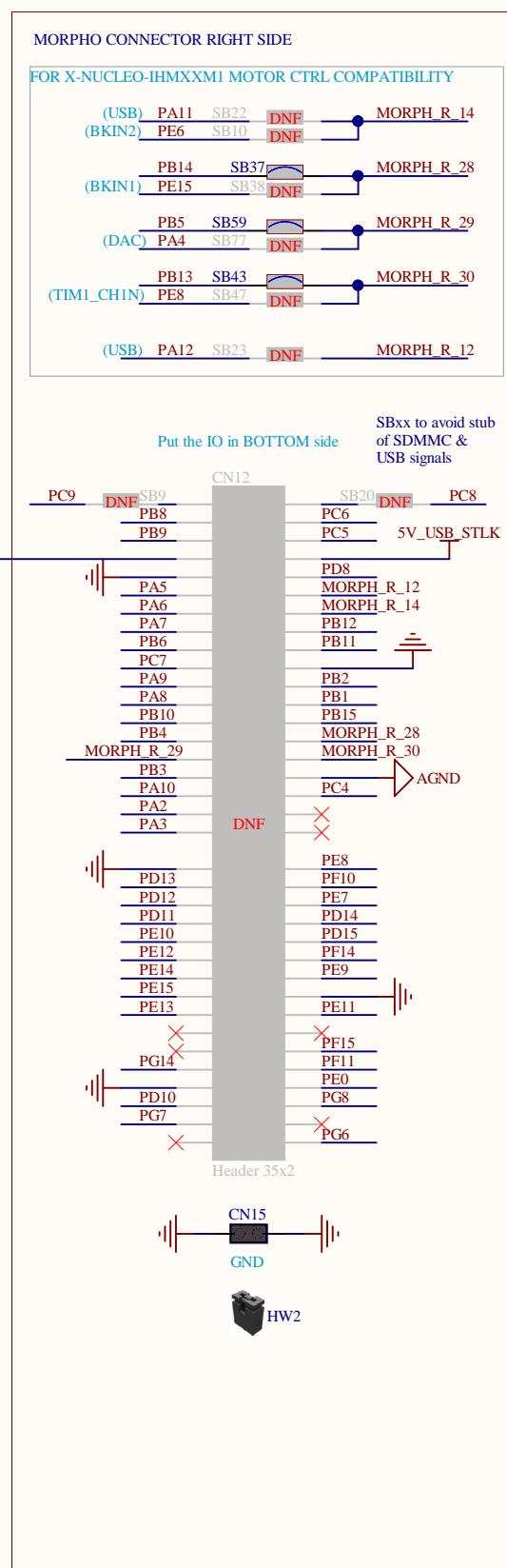
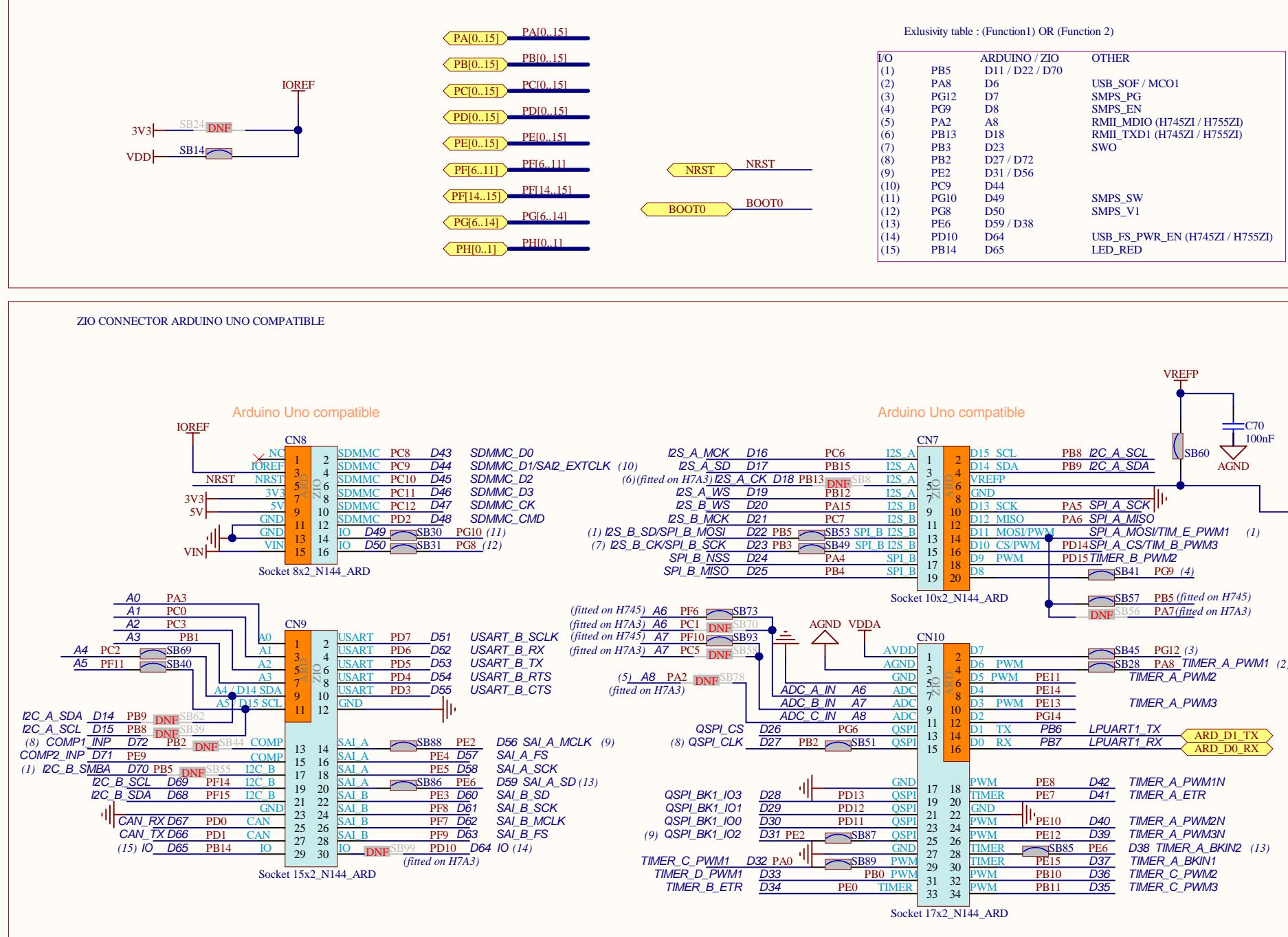
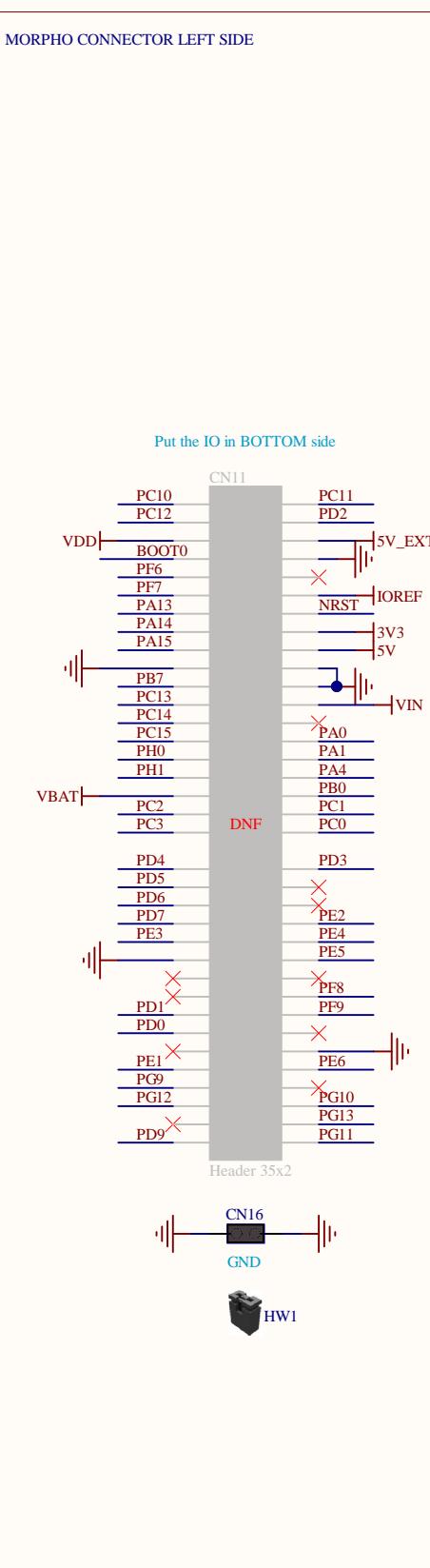
Compared to config 2 :
Disconnect VDD_SMPS_IND_OUT from VCAP
Connect VDD_SMPS_IND_OUT to VDD_LDO
Add 2x100nF near VDDLDO pins/plans
Add 2x2.2uF near VCAP pins/plans (see config 1)



Supply Config 5 : external SMPS

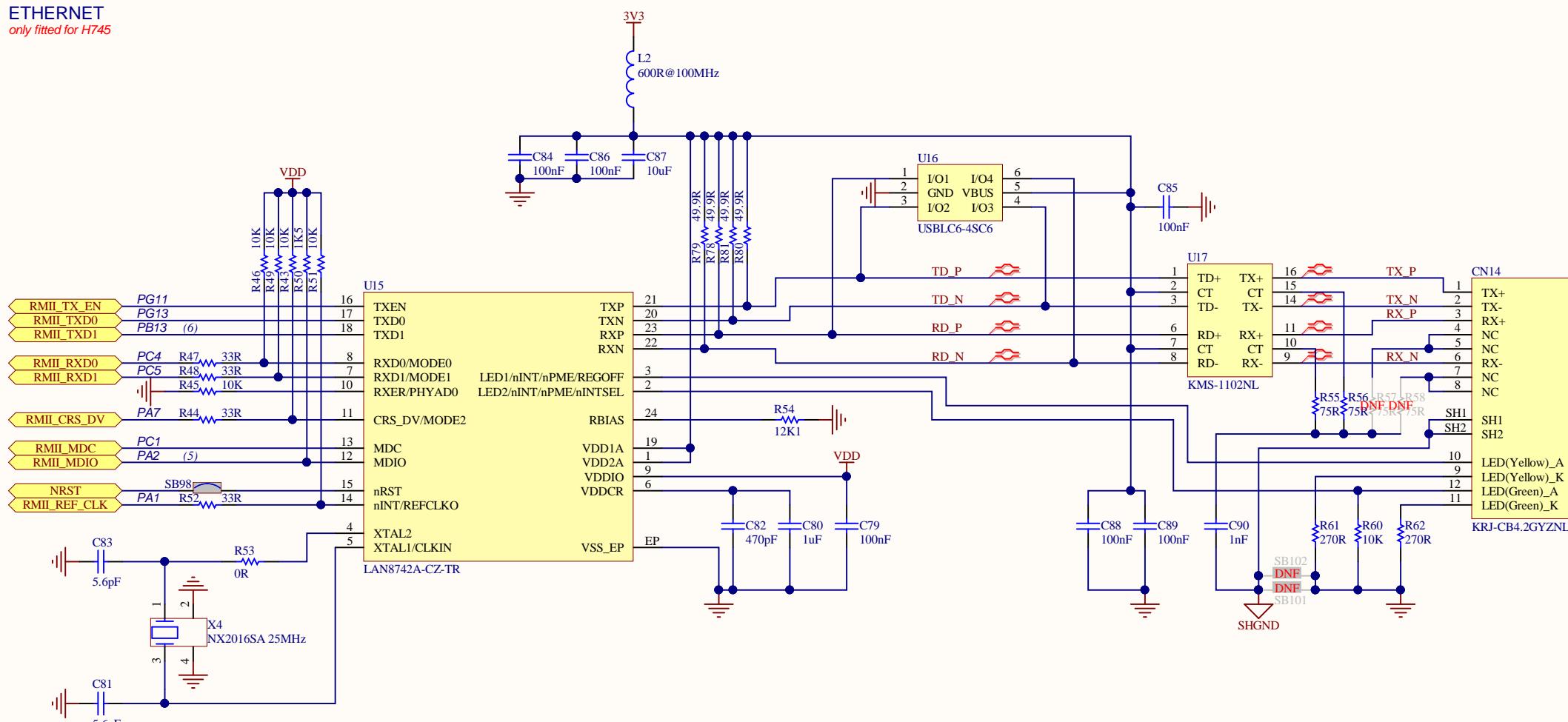
Disconnect 1V2_MCU from VDD_SMPS_IND_OUT
Connect 1V2_MCU to 1V2_VOUTCORE (Connectors page)

Title: MCU 144 POWER	
Project: Nucleo144 H7 SMPS with STLINK V3	
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ETHERNET

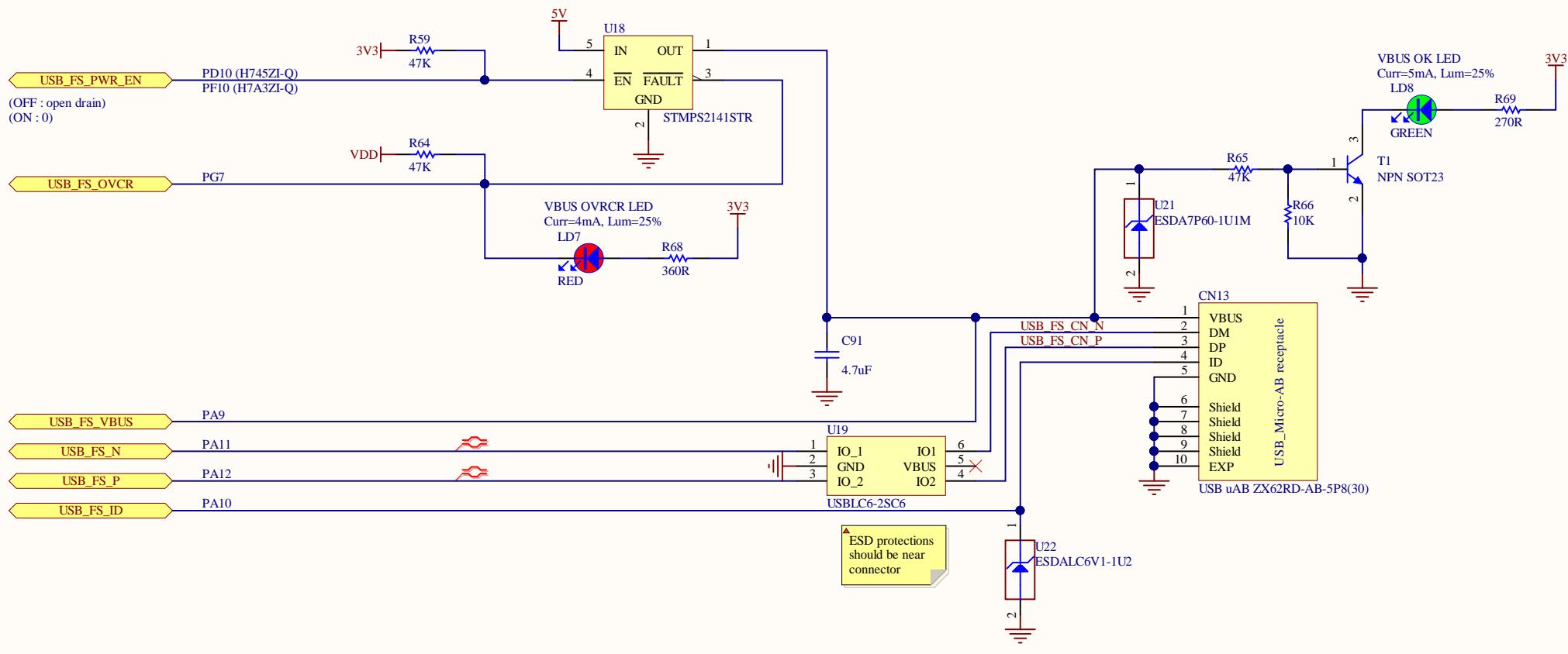
only fitted for H745



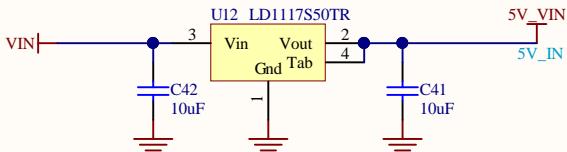
Title: Ethernet PHY with RJ45 connector	
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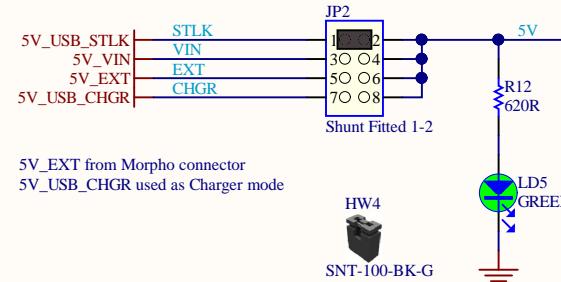
USB FS



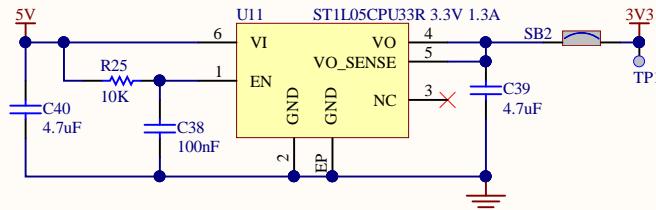
VIN / 5V PWR



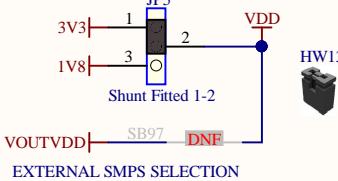
5V PWR SELECTION



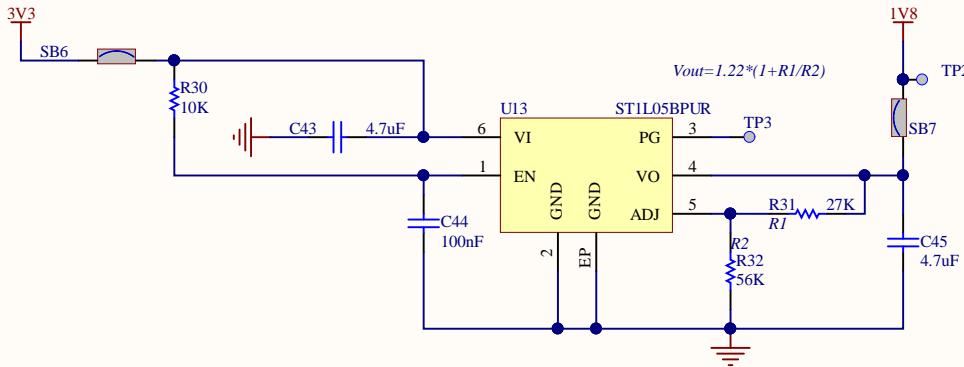
3V3 PWR



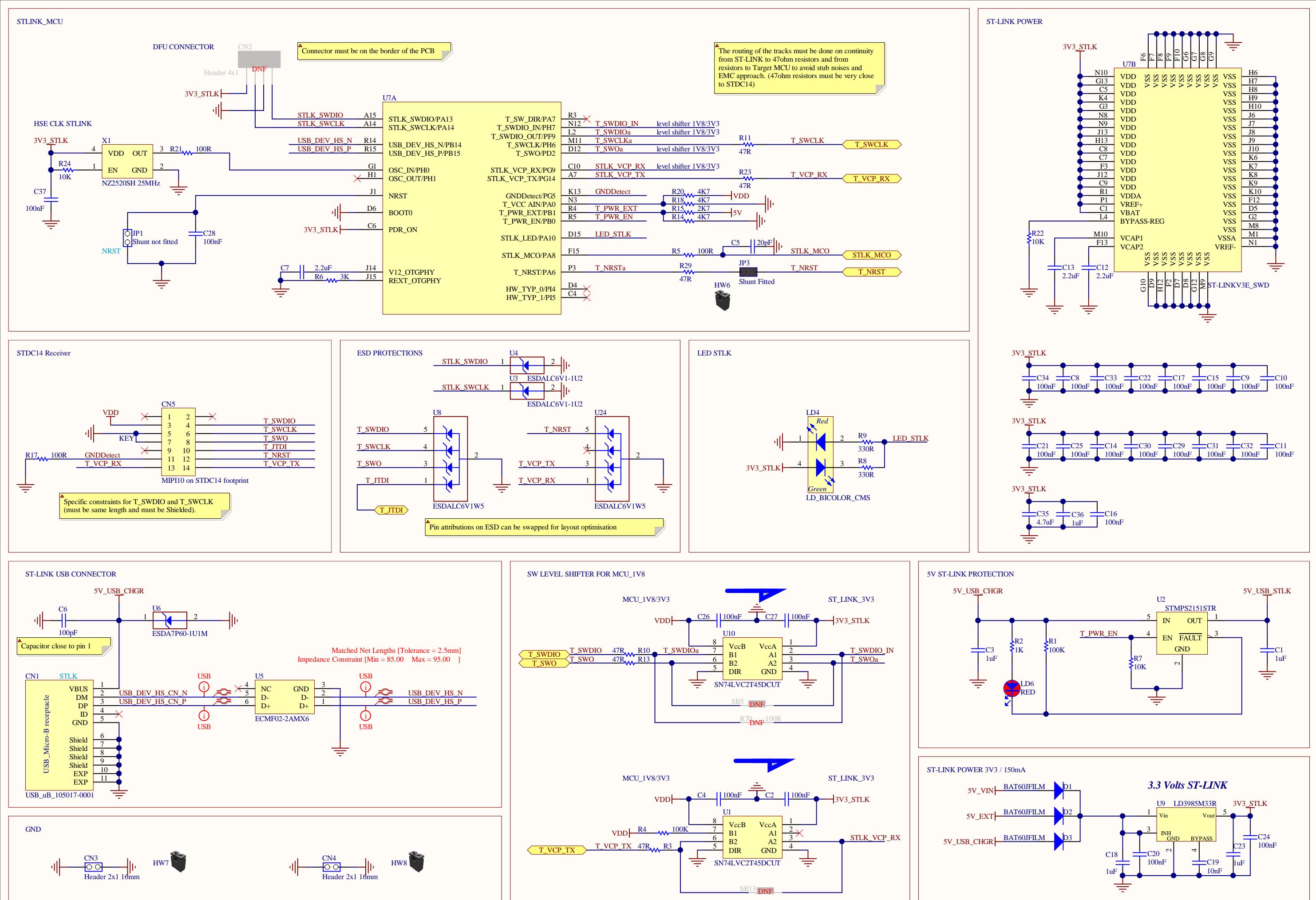
3V3/1V8 SELECTION

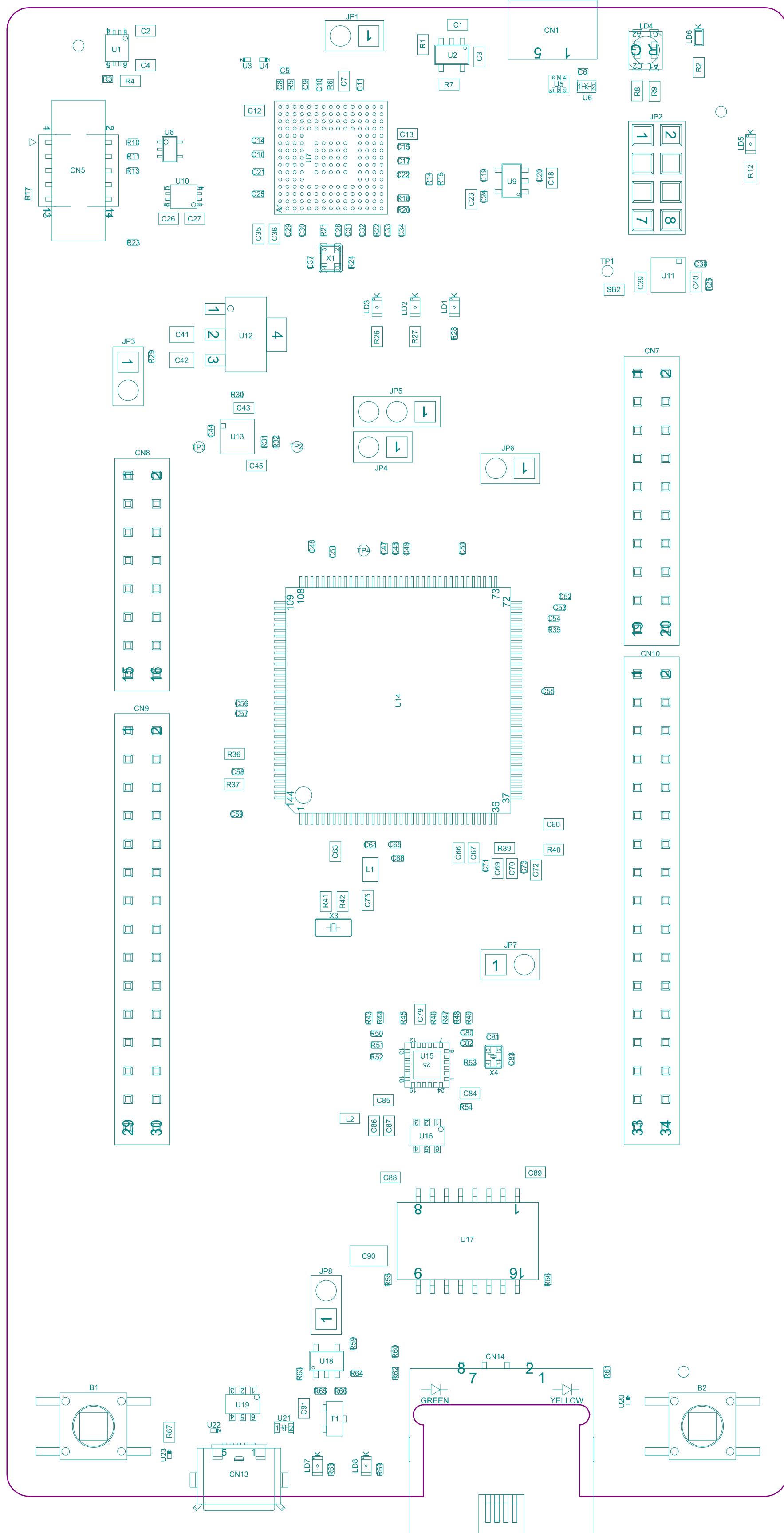


1V8 PWR



Title:	MAIN POWER 5V / 3V3 / 1V8
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Project: Nucleo144 H7 SMPS with STLINK V3

Layer: M14-Top Assembly

Gerber: .GM14

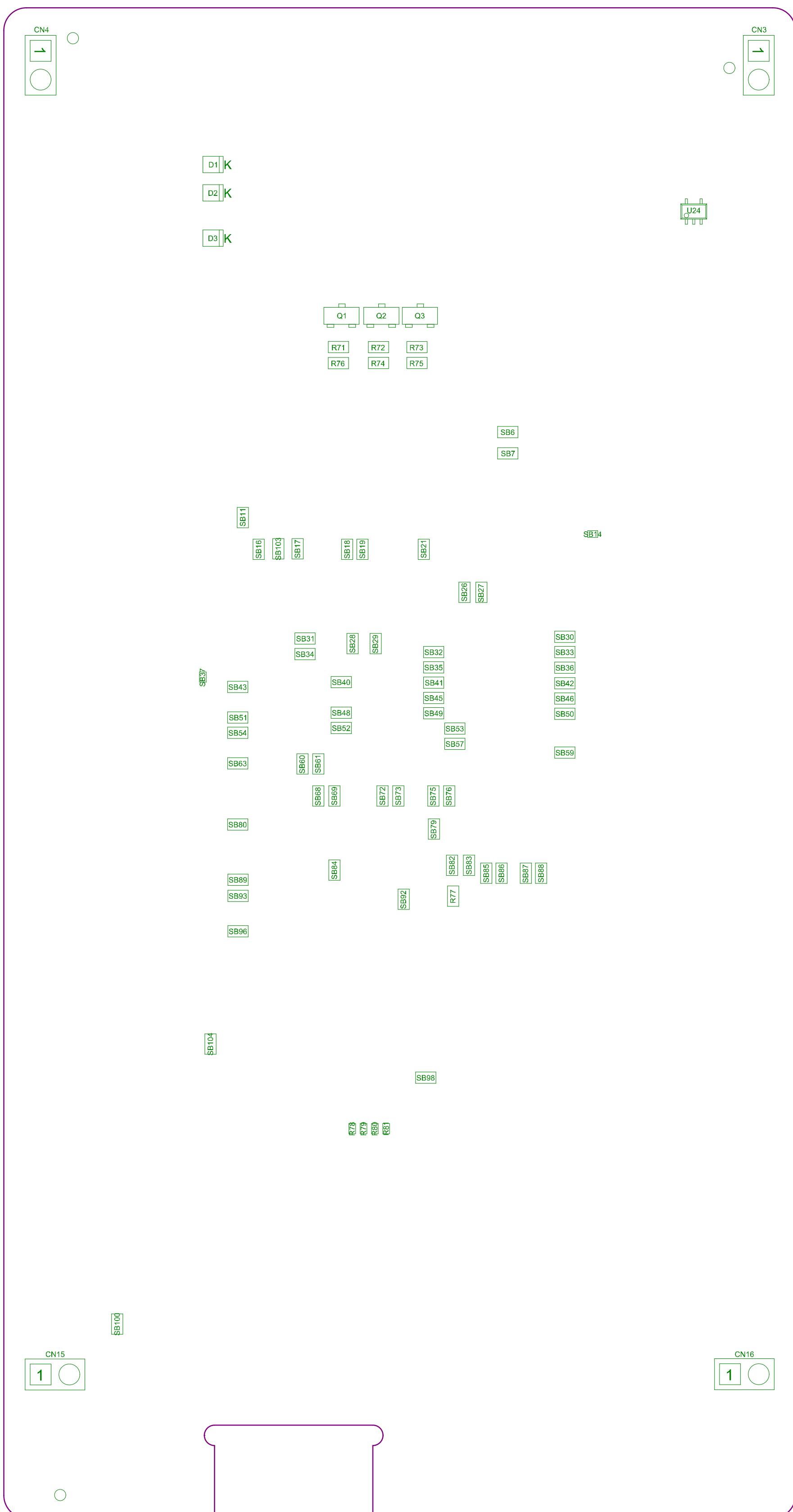
Variant: H755ZIQ

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Date: 09-OCT-19

Rev: D





Project: Nucleo144 H7 SMPS with STLINK V3

Layer: M15-Bottom Assembly

Gerber: GM15

Variant: H755ZIO

Ref·ME

