1. **Requirements**

* Linear regulator -1- “**ASM1117**” 3.3V
* Linear regulator -2- “**TPS7A7001DDA**” 3.3V (Valve & Motor )
* Boost converter 1- 5V “**TPS61023DRLR**” from TEXAS instrument with simulation
* Boost converter 2- 5V “**TPS61090RSAR** Boost Converter With 2-A All Single Cell Li or Dual Cell Battery or USB drain. During the shutdown, the load is completely Powered Operated Products
* Battery charger one cell with NTC “**MCP73871-2CCI/ML**”
* Shunt regulator with output 2.5V “**LM4040A25IDCKR**”
* **USB Type C** for debugging
* 3Xconnectors **stemma** for I2C two mounted external and one internal in the enclosure
* Connector **HDMI**
* Circuit BOOT and Enable **for ESP32 S3**
* Main MCU is **ESP32-S3**
* **Flash memory** 8M connect with QSPI to **ESP32-S3**
* SRAM 8M Connect with same **PROTOCOL** **QSPI** with **ESP32-S3**
* Connector **SD-Card**
* 2X **Connector SPI** one is internal and the second is external
* **RGB LED**
* **Fuel Gauge** monitoring Battery
* **TMP117** sensor of temperature
* **Connector** for testing all test points
* Spo2 sensor **AFE4490**
* Sensor **ADS1263** with resolution 32Bit
* **LD910** Drive motor & Valve
* sensor **ICM20948**
* Pressure sensor **MPRLS0025PA00001A**

1. **LEDs**

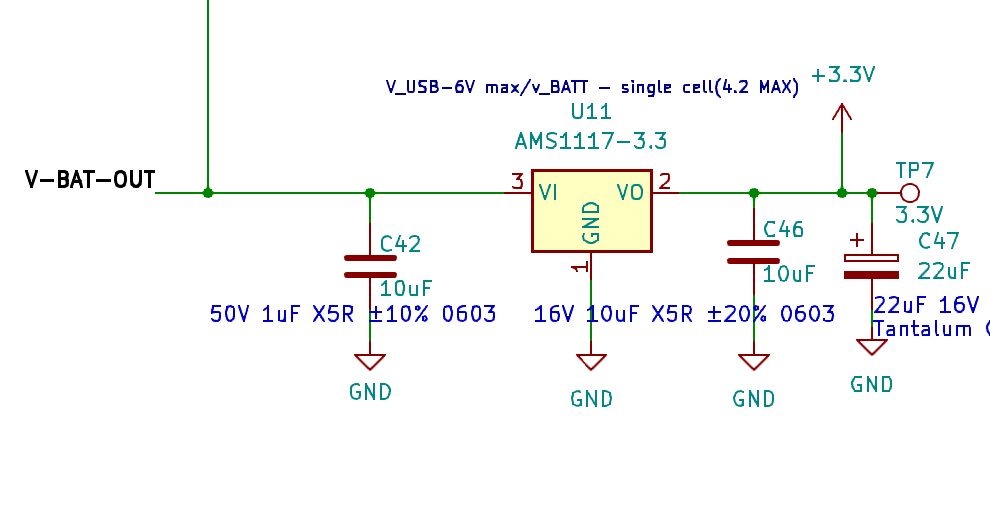
-POWER LED to indicate full charge **RED**

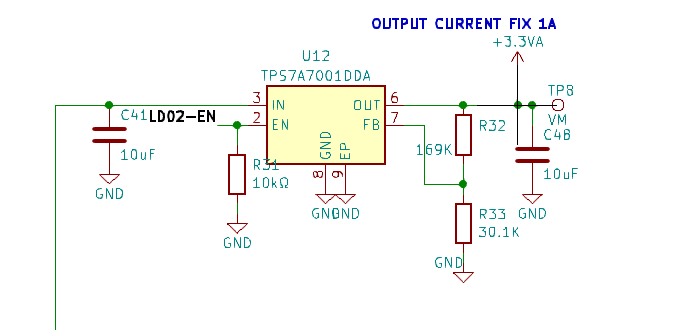
**-** Power LED to indicate Low battery **– ORANGE**

**- RGB** LED status of the boot, debugging, and RESET

1. Linear regulator

**LDO 1**

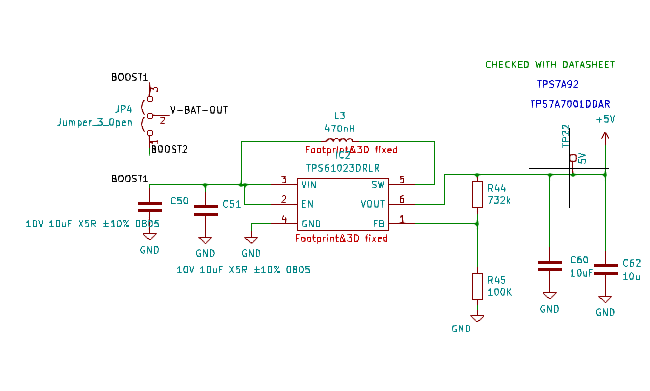




**LDO 2**

1. **Boost converter**

The boost converter 3.3V to 5V to power the ADS1263 I added two examples of boots from TEXS with their simulation

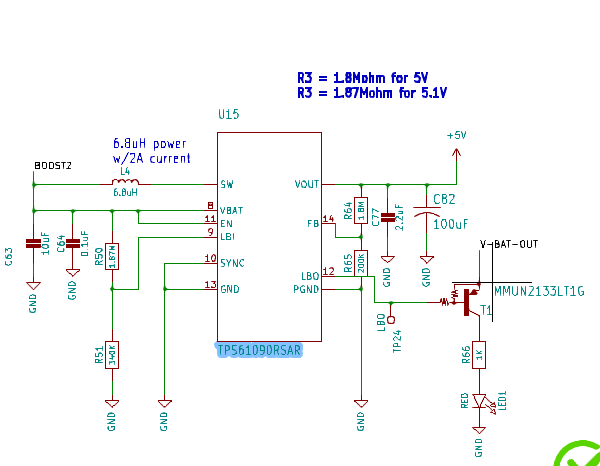


**BOOST 1 TPS61023DRLR**

Simulation on **WEEBENCH**

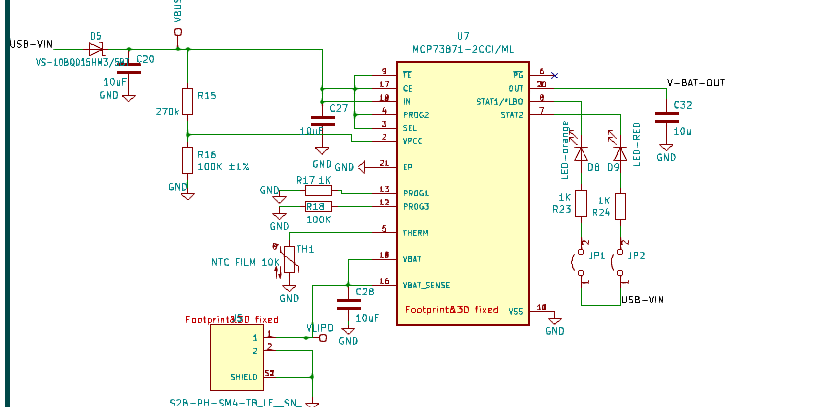
<https://webench.ti.com/power-designer/switching-regulator/customize/251>

**BOOST 2 TPS61090RSAR**



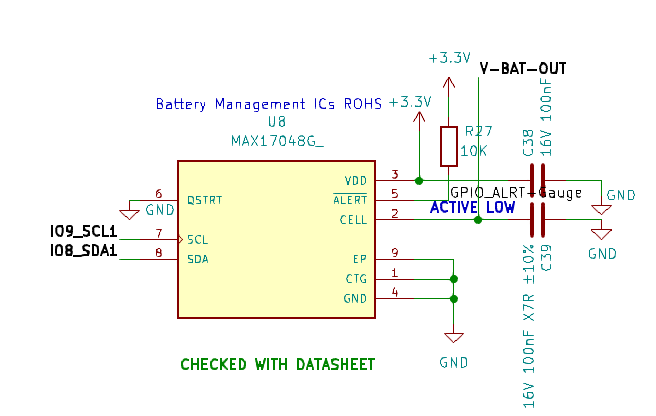
<https://www.adafruit.com/product/4654>

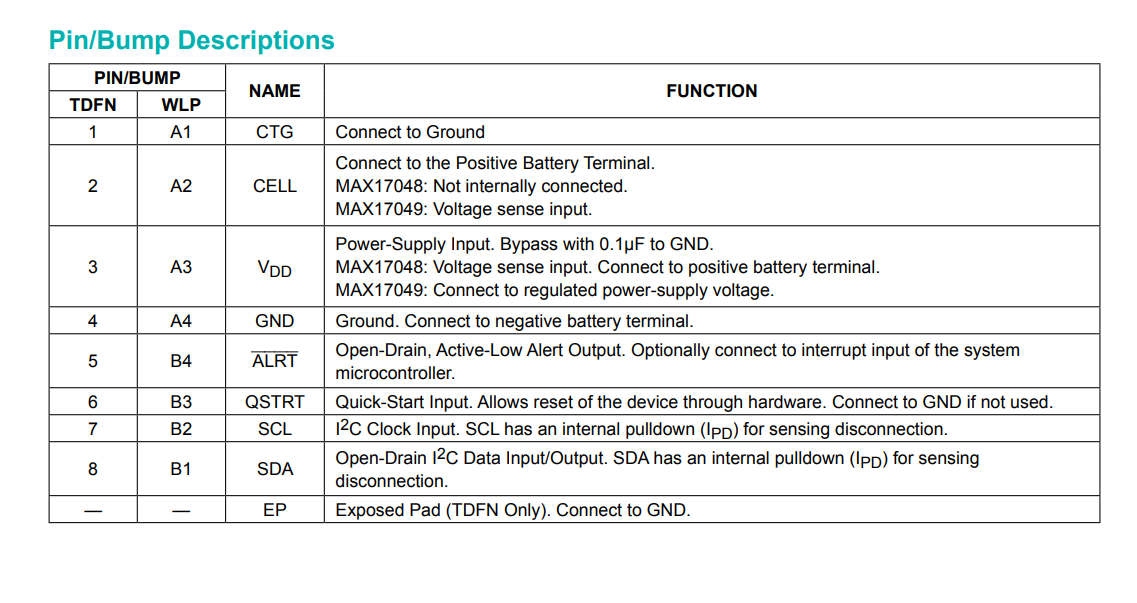
1. **Battery charger one cell with NTC**



<https://learn.adafruit.com/assets/24638>

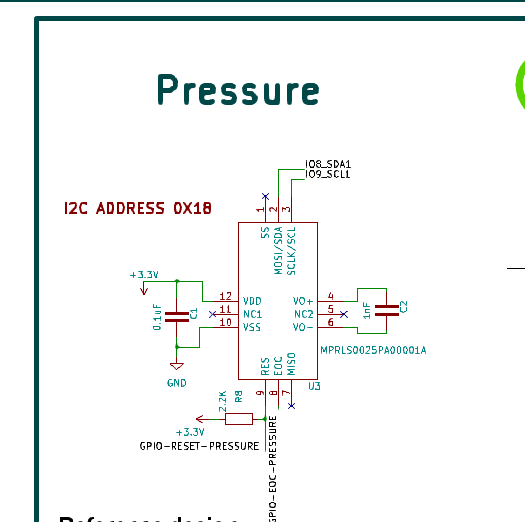
1. **Fuel Gauge**





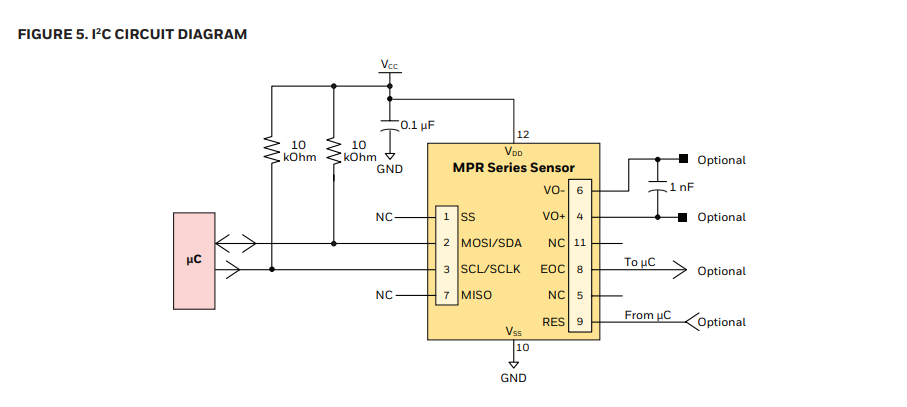
<https://cdn-learn.adafruit.com/downloads/pdf/adafruit-max17048-lipoly-liion-fuel-gauge-and-battery-monitor.pdf>

1. **Pressure sensor**

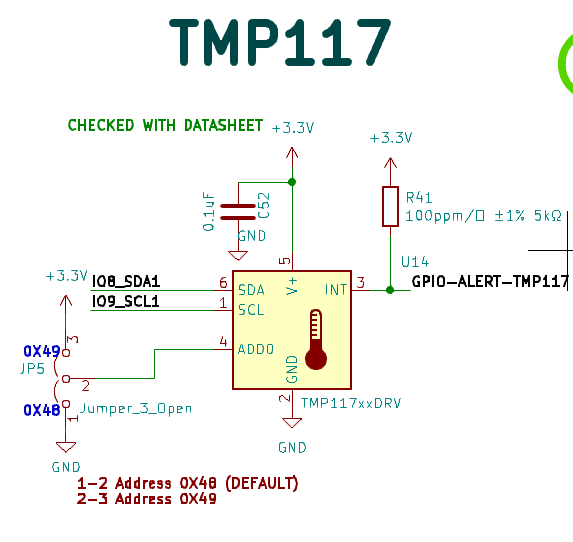


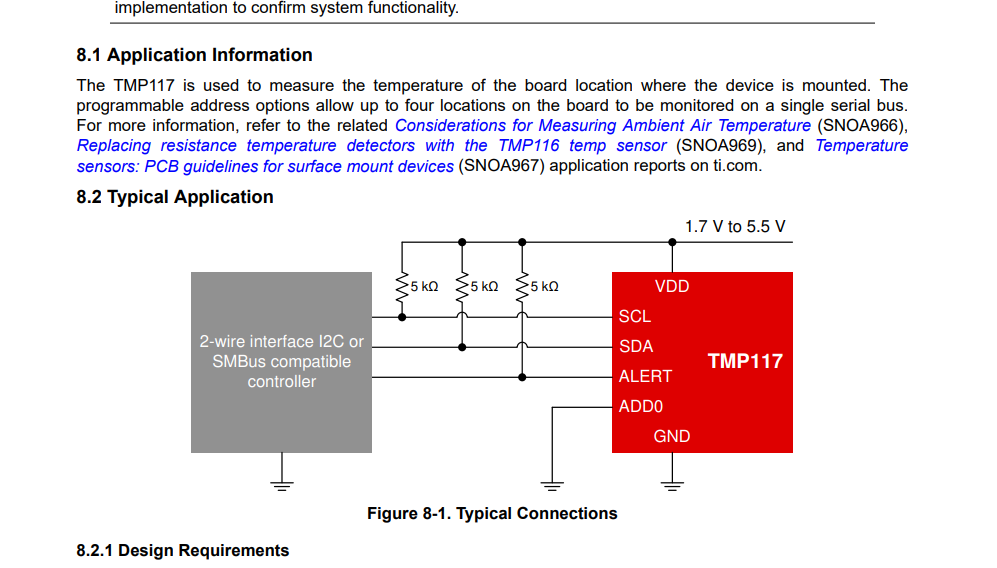
<https://www.sparkfun.com/products/16476>

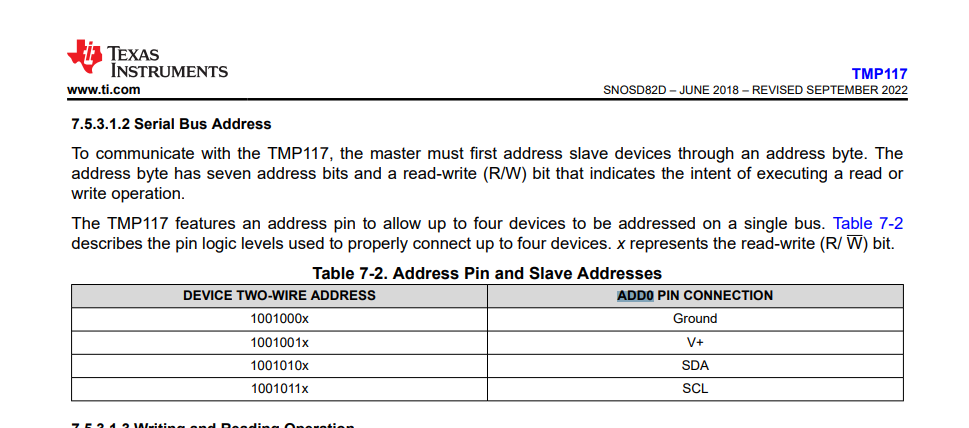
[https://cdn.sparkfun.com/assets/8/7/2/1/f/SparkFun\_MicroPressure\_Sensor\_Schematic.pdf?\_gl=1\*el18zc\*\_ga\*MTAxMTUyMjM2LjE3MDU5MTQ3Njc.\*\_ga\_T369JS7J9N\*MTcwNzMwMTc2NS43LjAuMTcwNzMwMTc2NS42MC4wLjA](https://cdn.sparkfun.com/assets/8/7/2/1/f/SparkFun_MicroPressure_Sensor_Schematic.pdf?_gl=1*el18zc*_ga*MTAxMTUyMjM2LjE3MDU5MTQ3Njc.*_ga_T369JS7J9N*MTcwNzMwMTc2NS43LjAuMTcwNzMwMTc2NS42MC4wLjA).



1. **TMP1117**







**REFERENCE**

<https://www.ti.com/lit/ds/symlink/tmp117.pdf?ts=1707296928379&ref_url=https%253A%252F%252Fwww.google.com%252F>

CUT OUT ZONE IN PCB

<https://www.sparkfun.com/products/retired/15413>

1. **ESP32-S3**

## Power Supply[ℑ](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#power-supply)

The general recommendations for power supply design are:

* When using a single power supply, the recommended power supply voltage is 3.3 V and the output current is no less than 500 mA.

### Digital Power Supply[ℑ](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#digital-power-supply)

ESP32-S3 has **pin46 VDD3P3\_CPU** as the digital power supply pin(s) working in a voltage range of 3.0 V ~ 3.6 V. It is recommended to add an extra 0.1 μF decoupling capacitor close to the pin(s).

Pin **VDD\_SPI** **can serve as the power supply for the external device at either 1.8 V or 3.3 V (default).** It is recommended to add extra 0.1 μF and 1 μF decoupling capacitors close to **VDD\_SPI.**

* When **VDD\_SPI** operates at 1.8 V, it is powered by ESP32-S3’s internal LDO. The typical current this LDO can offer is 40 mA.

**Attention**

When using VDD\_SPI as the power supply pin for in-package or off-package 3.3 V flash/PSRAM, the supply voltage should be 3.0 V or above, so as to meet the requirements of flash/PSRAM’s working voltage.

### Analog Power Supply[ℑ](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#analog-power-supply)

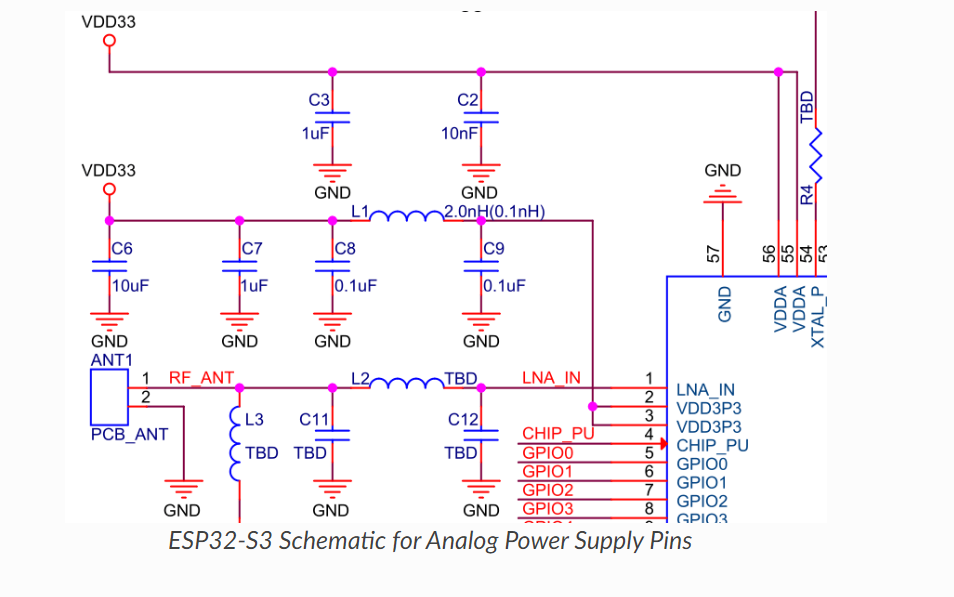
ESP32-S3’s VDDA and VDD3P3 pins are the analog power supply pins, working at 3.0 V ~ 3.6 V.

For VDD3P3, when ESP32-S3 is transmitting signals, there may be a sudden increase in the current draw, causing power rail collapse. Therefore, it is highly recommended to add a 10 μF capacitor to the power rail, which can work in conjunction with the 1 μF capacitor(s).

It is suggested to add an extra 10 μF capacitor at the power entrance. If the power entrance is close to VDD3P3, then two 10 μF capacitors can be merged into one.

Add a LC circuit on the VDD3P3 power rail to suppress high-frequency harmonics. The inductor’s rated current is preferably 500 mA and above.

Place appropriate decoupling capacitors near the other analog power pins according to Figure [ESP32-S3 Schematic for Analog Power Supply Pins](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#fig-chip-analog-power).

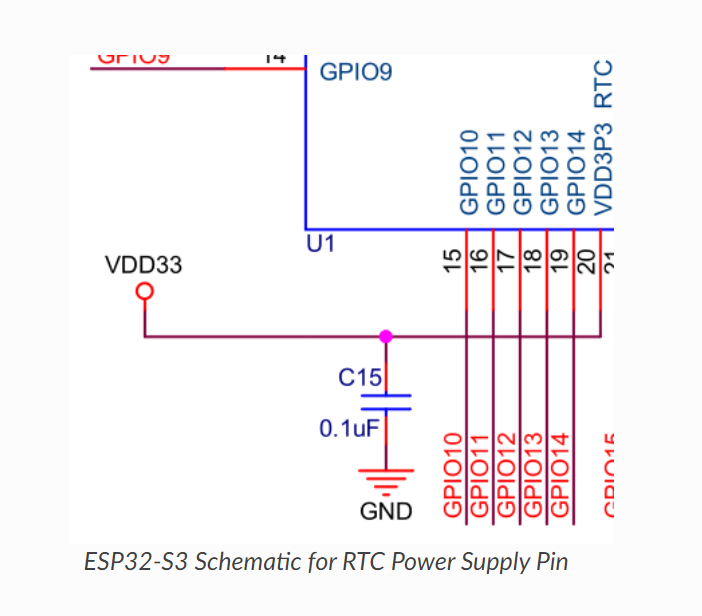


### **RTC Power Supply**[**ℑ**](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#rtc-power-supply)

ESP32-S3’s VDD3P3\_RTC pin is the RTC and analog power pin. It is recommended to place a 0.1 μF decoupling capacitor near this power pin in the circuit.

Note that this power supply cannot be used as a single backup power supply.

The schematic for the RTC power supply pin is shown in Figure [ESP32-S3 Schematic for RTC Power Supply Pin](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#fig-chip-rtc-power).



## **Chip Power-up and Reset Timing**[ℑ](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#chip-power-up-and-reset-timing)

ESP32-S3’s CHIP\_PU pin can enable the chip when it is high and reset the chip when it is low. **NOTED**

When ESP32-S3 uses a 3.3 V system power supply, the power rails need some time to stabilize before CHIP\_PU is pulled up and the chip is enabled. Therefore, CHIP\_PU needs to be asserted high after the 3.3 V rails have been brought up.

To reset the chip, keep the reset voltage VIL\_nRST in the range of (–0.3 ~ 0.25 × VDD) V. To avoid reboots caused by external interferences, make the CHIP\_PU trace as short as possible. **NOTED**

**Attention**

* CHIP\_PU must not be left floating.
* To ensure the correct power-up and reset timing, it is advised to add an RC delay circuit at the CHIP\_PU pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the characteristics of the actual power supply and the power-up and reset timing of the chip.

## **Flash and PSRAM**[ℑ](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#flash-and-psram)

ESP32-S3 requires in-package or off-package flash to store application firmware and data. In-package PSRAM or off-package RAM is optional. **NOTED**

### **In-Package Flash and PSRAM**[ℑ](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#in-package-flash-and-psram)

The tables list the pin-to-pin mapping between the chip and in-package flash/PSRAM. Please note that the following chip pins can connect at most one flash and one PSRAM. That is to say, when there is only flash in the package, the pin occupied by flash can only connect PSRAM and cannot be used for other functions; when there is only PSRAM, the pin occupied by PSRAM can only connect flash; when there are both flash and PSRAM, the pin occupied cannot connect any more flash or PSRAM.

| *Pin-to-Pin Mapping Between Chip and In-Package Quad SPI Flash*[*ℑ*](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#tab-chip-flash-pin-mapping) | | |
| --- | --- | --- |
| **ESP32-S3FN8/ESP32-S3FH4R2** | **In-Package Flash (Quad SPI)** | |
| SPICLK | CLK | |
| SPICS0 | CS# | |
| SPID | DI | |
| SPIQ | DO | |
| SPIWP | WP# | |
| SPIHD | HOLD# | |
| *Pin-to-Pin Mapping Between Chip and In-Package Quad SPI PSRAM* | |
|  | |

### **Off-Package Flash and PSRAM**[ℑ](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#off-package-flash-and-psram)

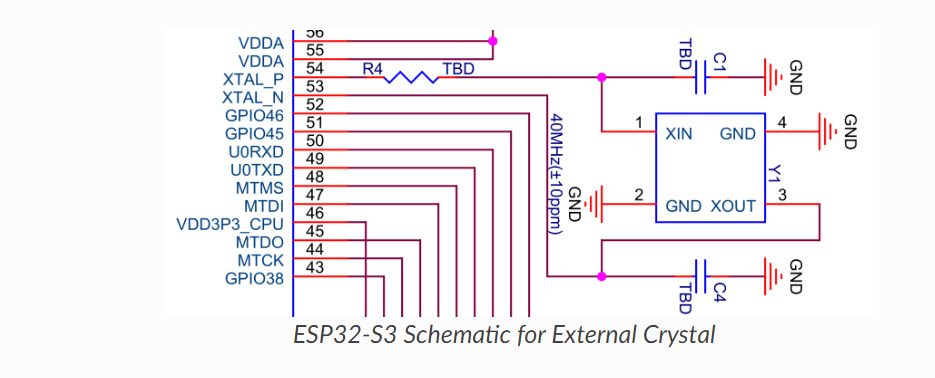
ESP32-S3 supports up to 1 GB off-package flash and 1 GB off-package RAM. If VDD\_SPI is used to supply power, make sure to select the appropriate off-package flash and RAM according to the power voltage on VDD\_SPI (1.8 V/3.3 V). It is recommended to add a zero-ohm series resistor on the SPI communication lines to lower the driving current, reduce interference to RF, adjust timing, and better shield from interference

## **Clock Source**[**ℑ**](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#clock-source)

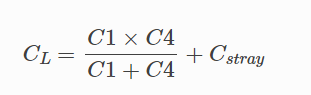
* [External crystal clock source (Compulsory)](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#external-crystal-clock-source-compulsory)
* [RTC clock source (Optional)](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#rtc-clock-source-optional)

### External Crystal Clock Source (Compulsory)[ℑ](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#external-crystal-clock-source-compulsory)

**The ESP32-S3 firmware only supports 40 MHz crystal. Noted**

The circuit for the crystal is shown in Figure [ESP32-S3 Schematic for External Crystal](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#fig-external-crystal-schematic). Note that the accuracy of the selected crystal should be within ±10 ppm. **Noted**

The initial values of external capacitors C1 and C4 can be determined according to the formula: **NOTED**



where the value of CL (load capacitance) can be found in the crystal’s datasheet, and the value of Cstray refers to the PCB’s stray capacitance. The values of C1 and C4 need to be further adjusted after an overall test as below

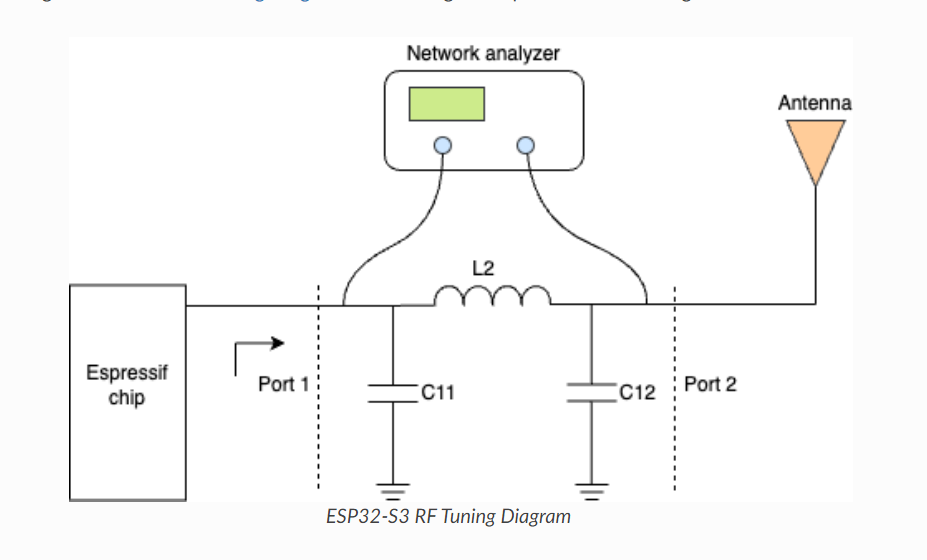
## RF[ℑ](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#rf)

### **RF Circuit**[**ℑ**](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#rf-circuit)

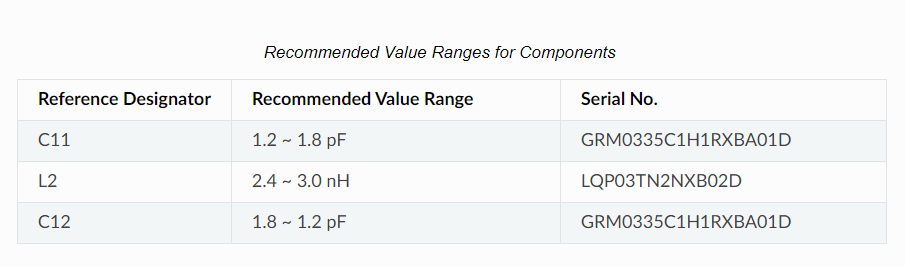
ESP32-S3’s RF circuit is mainly composed of three parts, the RF traces on the PCB board, the chip matching circuit, the antenna and the antenna matching circuit. Each part should meet the following requirements:

* For the RF traces on the PCB board, 50 Ω impedance control is required.
* For the chip matching circuit, it must be placed close to the chip. A CLC structure is preferred.
  + The CLC structure is mainly used to adjust the impedance point and suppress harmonics, and a set of LC can be added if space permits.
  + The RF matching circuit is shown in Figure [ESP32-S3 Schematic for RF Matching](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#fig-rf-matching-schematic).

The RF matching parameters vary with the board, so the ones used in Espressif modules could not be applied directly. Follow the instructions below to do RF tuning. **NOTED**



PCB design of the chip strictly follows the PCB design stated in Chapter [PCB Layout Design](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#pcb-layout-design), you can refer to the value ranges in Table [Recommended Value Ranges for Components](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#tab-recommended-value-ranges-components) to debug the matching circuit. **NOTED**



When using GPIOs, please:

* Pay attention to the states of strapping pins during power-up.**NOTED**
* Pay attention to the default configurations of the GPIOs after reset. The default configurations can be found in Table [IO MUX Pin Functions](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#io-mux-pin-functions). It is recommended to add a pull-up or pull-down resistor to pins in the high-impedance state or enable the pull-up and pull-down during software initialization to avoid extra power consumption. **NOTED**
* Avoid using the pins already occupied by flash/PSRAM. **NOTED**
* When USB-OTG Download Boot mode is enabled, some pins will have level output. Refer to Table [IO Pad Status After Chip Initialization in the USB-OTG Download Boot Mode](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#io-pad-status-after-chip-initialization-in-the-usb-otg-download-boot-mode) for details. **NOTED**
* SPICLK\_N, SPICLK\_P, and GPIO33 ~ GPIO37 work in the same power domain, so if octal 1.8 V flash/PSRAM is used, then SPICLK\_P and SPICLK\_N also work in the 1.8 V power domain. **NOTED**
* Only GPIOs in the VDD3P3\_RTC power domain can be controlled in Deep-sleep mode. **NOTED**

## USB

ESP32-S3 integrates a USB Serial/JTAG controller that supports USB 2.0 full-speed device.

GPIO19 and GPIO20 can be used as D- and D + of USB respectively. It is recommended to populate zero-ohm series resistors between the mentioned pins and the USB connector. Also, reserve a footprint for a capacitor to ground on each trace. Note that both components should be placed close to the chip. **NOTED**

# PCB Layout Design[ℑ](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#pcb-layout-design)

## General Principles of PCB Layout[ℑ](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#general-principles-of-pcb-layout) **NOTED**

It is recommended to use a four-layer PCB design:

* Layer 1 (TOP): Signal traces and components.
* Layer 2 (GND): No signal traces here to ensure a complete GND plane.
* Layer 3 (POWER): GND plane should be applied to better isolate the RF and crystal. Route power traces and a few signal traces on this layer, provided that there is a complete GND plane under the RF and crystal.
* Layer 4 (BOTTOM): Route a few signal traces here. It is not recommended to place any components on this layer.

Antenna design

If the PCB antenna cannot be placed outside the board, please ensure a clearance of at least 15 mm around the antenna area (no copper, routing, or components on it), and place the feed point of the antenna closest to the board. If there is a base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna. Figure [Keepout Zone for ESP32-S3 Module’s Antenna on the Base Board](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html" \l "fig-module-clearance) shows the suggested clearance for modules whose antenna feed point is on the right.

## Power Supply[ℑ](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#power-supply) **Layout**

Figure [ESP32-S3 Power Traces in a Four-layer PCB Design](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#fig-power-layout) shows the overview of the power traces in a four-layer PCB design.

### General Guidelines[ℑ](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#general-guidelines)

* Four-layer PCB design is preferred. **NOTED**
* The power traces should be routed on the inner third layer whenever possible.
* Vias are required for the power traces to go through the layers and get connected to the pins on the top layer. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces. **NOTED**
* The ground pad at the bottom of the chip should be connected to the ground plane through at least nine ground vias. **NOTED**
* If you need to add a thermal pad EPAD under the chip on the bottom of the module, it is recommended to employ a square grid on the EPAD, cover the gaps with solder paste, and place ground vias in the gaps, as shown in Figure [ESP32-S3 Power Traces in a Four-layer PCB Design](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#fig-power-layout). This can avoid chip displacement caused by tin leakage and bubbles when soldering the module EPAD to the substrate. **NOTED**

### **3.3 V Power Layout**[**ℑ**](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#v-power-layout)

* In Figure [ESP32-S3 Power Traces in a Four-layer PCB Design](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#fig-power-layout), the 10 µF capacitor is shared by the analog power supply VDD3P3, and the power entrance since the analog power is close to the chip power entrance. If the chip power entrance is not near VDD3P3, it is recommended to add a 10 µF capacitor to both the chip power entrance and VDD3P3. Also, reserve two 1 µF capacitors if space permits. **NOTED**
* The width of the main power traces should be no less than 25 mil. The width of VDD3P3 power traces should be no less than 20 mil. The recommended width of other power traces is 10 mil **NOTED**

## **Crystal Layout**

The layout of the crystal should follow the guidelines below:

* Ensure a complete GND plane for the RF, crystal, and chip. **NOTED**
* The crystal should be placed far from the clock pin to avoid interference on the chip. The gap should be at least 2.0 mm. It is good practice to add high-density ground vias stitching around the clock trace for better isolation. **NOTED**
* There should be no vias for the clock input and output traces, which means the traces cannot cross layers. The clock traces should not intersect with each other. **NOTED**
* Components in series to the crystal trace should be placed close to the chip side. **NOTED**
* The external matching capacitors should be placed on the two sides of the crystal, preferably at the end of the clock trace, but not connected directly to the series components. This is to make sure the ground pad of the capacitor is close to that of the crystal. **NOTED**
* Do not route high-frequency digital signal traces under the crystal. It is best not to route any signal trace under the crystal. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by grounding copper. **NOTED**
* As the crystal is a sensitive component, do not place any magnetic components nearby that may cause interference, for example large inductance component, and ensure that there is a clean large-area ground plane around the crystal **NOTED**

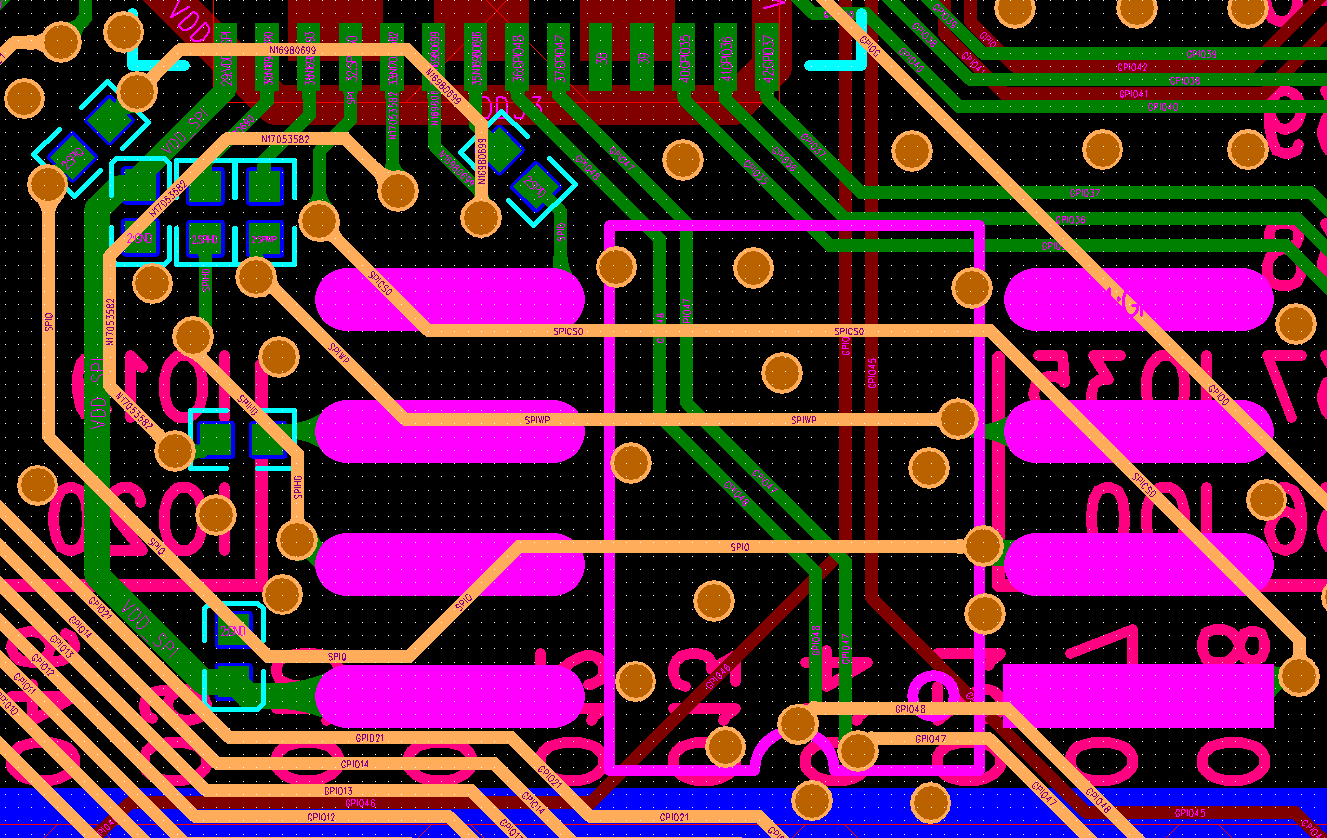
## **RF Layout**

* There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency components, such as crystals, DDR SDRAM, high-frequency clocks, etc. In addition, the USB port, USB-to-serial chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. The UART signal line should be surrounded by ground copper and ground vias **NOTED**

## **Flash and PSRAM**[**ℑ**](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#flash-and-psram)

The layout for flash and PSRAM should follow the guidelines below:

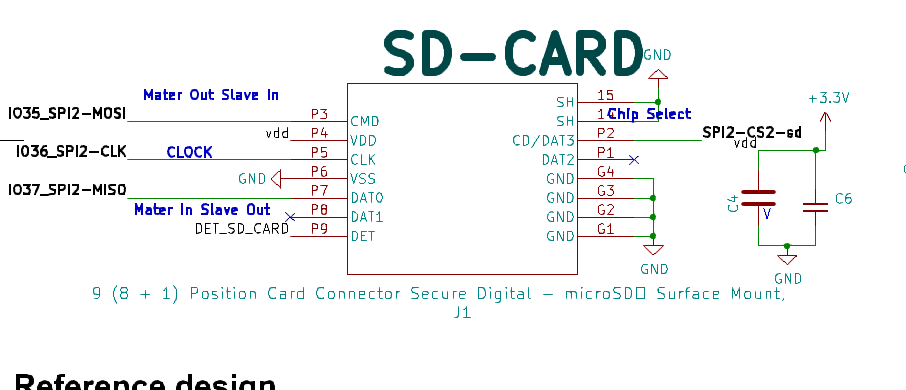
* Place the zero-ohm series resistors on the SPI lines close to the chip. **NOTED**
* Route the SPI traces on the inner layer (e.g., the third layer) whenever possible, and add ground copper and ground vias around the clock and data traces of SPI separately. **NOTED**
* Place the 0.1 μF capacitor to ground at the VDD\_SPI close to corresponding flash and PSRAM power pins. **NOTED**
* Octal SPI traces should have matching lengths. **NOTED**

Figure [ESP32-S3 Quad SPI Flash Layout](https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/pcb-layout-design.html#fig-flash-layout) shows the quad SPI flash layout.

References

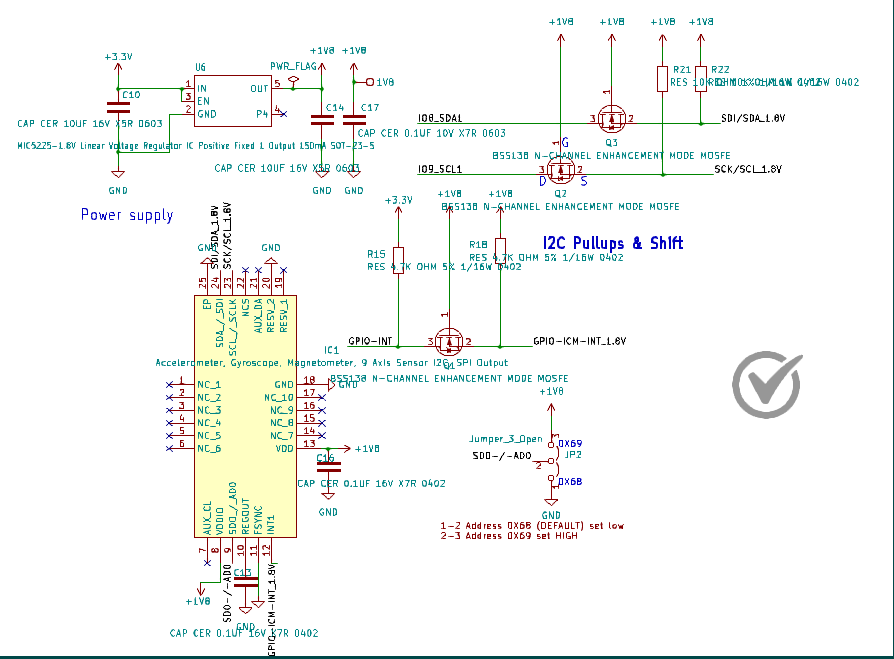
* 1. <https://docs.espressif.com/projects/esp-hardware-design-guidelines/en/latest/esp32s3/schematic-checklist.html#fig-rf-matching-schematic>
  2. <https://github.com/UnexpectedMaker/esp32s3/blob/main/schematics/schematic-feathers3_p7.pdf>

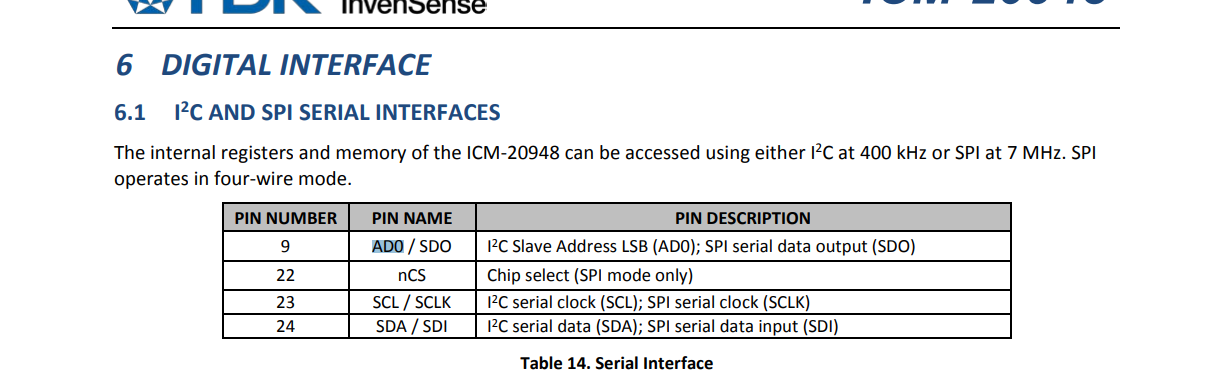
1. **SD-CARD**

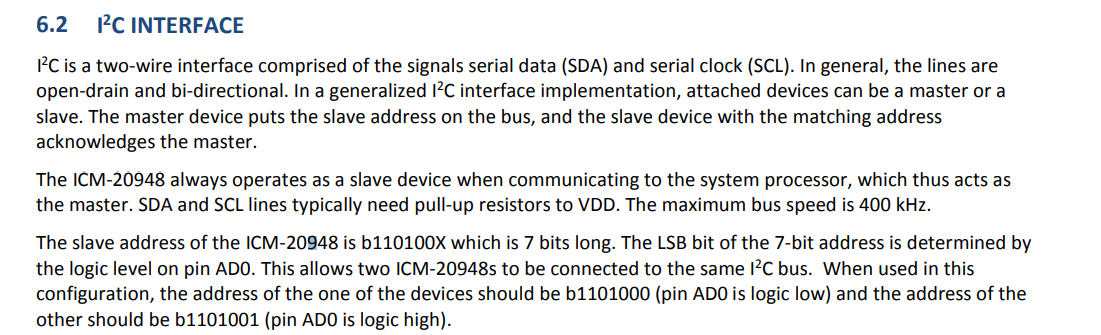


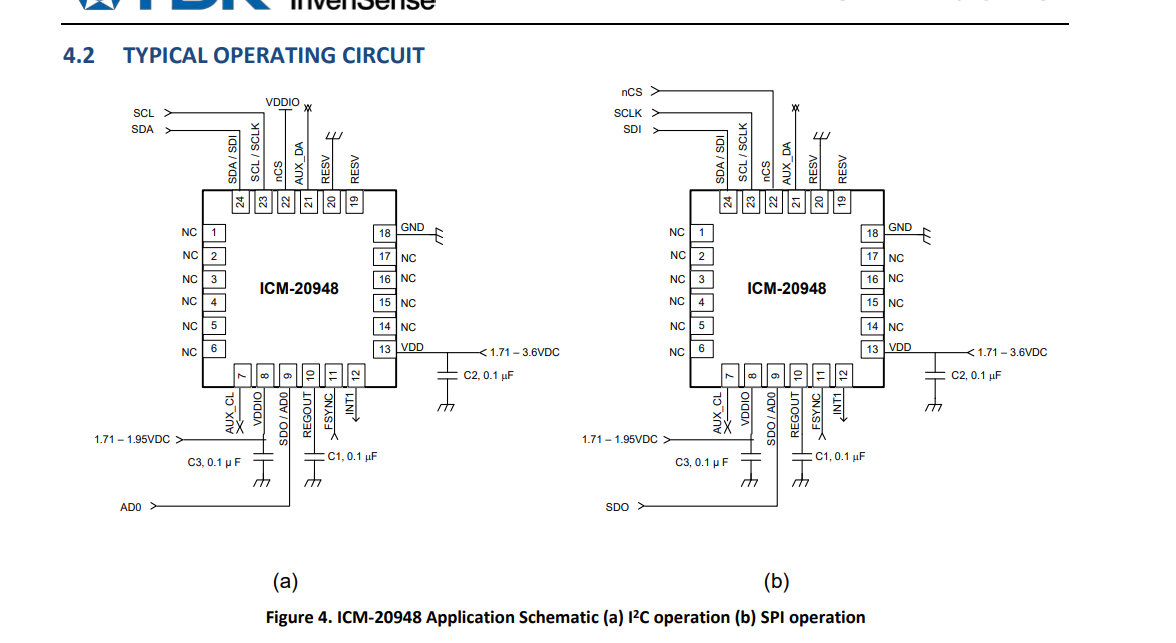
**Reference design**

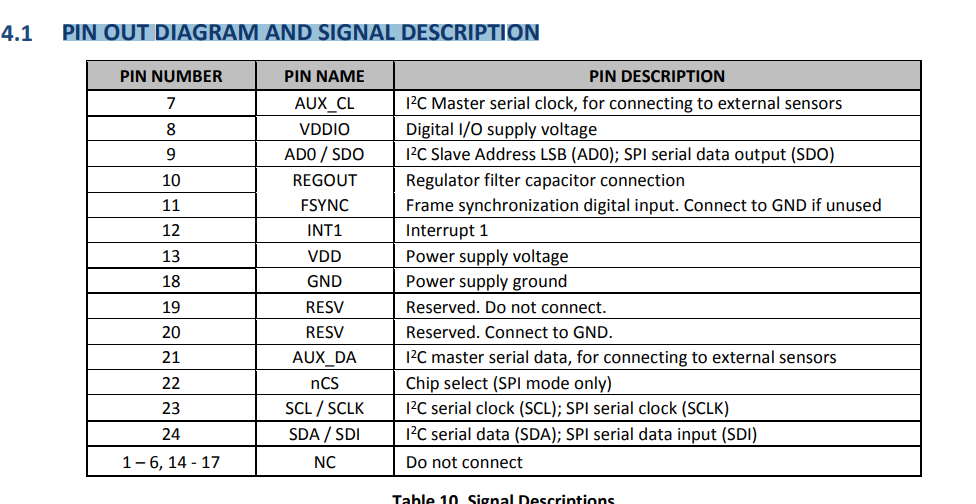
1. <https://github.com/adafruit/Adafruit-Metro-ESP32-S3-PCB>
2. [https://cdn.sparkfun.com/assets/5/9/7/4/1/SparkFun\_Thing\_Plus\_ESP32-WROOM\_C\_schematic2.pdf?\_gl=1\*1jd2j8a\*\_ga\*MTU5MTMwOTE0Ni4xNjk5NzIxMTY3\*\_ga\_T369JS7J9N\*MTcwNDYzODQ2MS41OS4wLjE3MDQ2Mzg0NjEuNjAuMC4w](https://cdn.sparkfun.com/assets/5/9/7/4/1/SparkFun_Thing_Plus_ESP32-WROOM_C_schematic2.pdf?_gl=1*1jd2j8a*_ga*MTU5MTMwOTE0Ni4xNjk5NzIxMTY3*_ga_T369JS7J9N*MTcwNDYzODQ2MS41OS4wLjE3MDQ2Mzg0NjEuNjAuMC4w)
3. **ICM-20948**







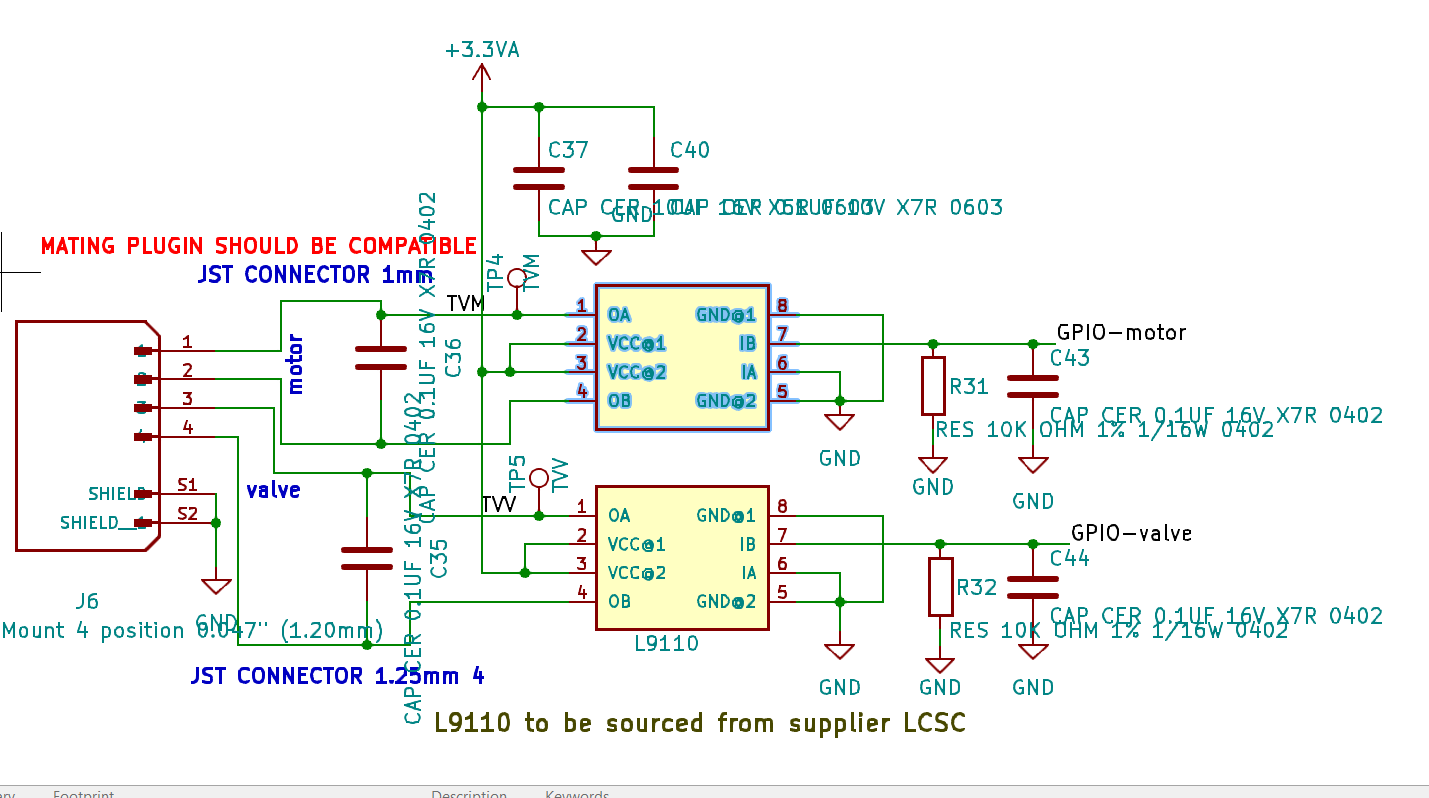




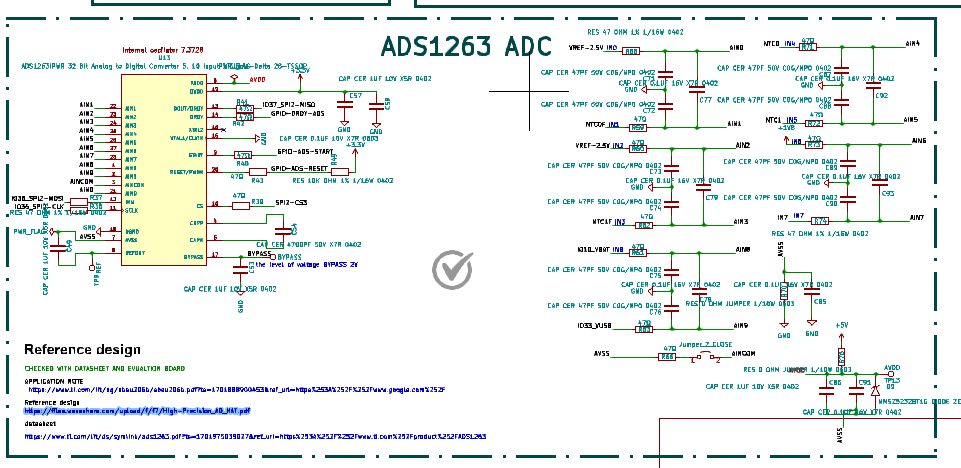
**Reference ADAFRUIT design**

<https://github.com/adafruit/Adafruit-ICM20948-PCB>

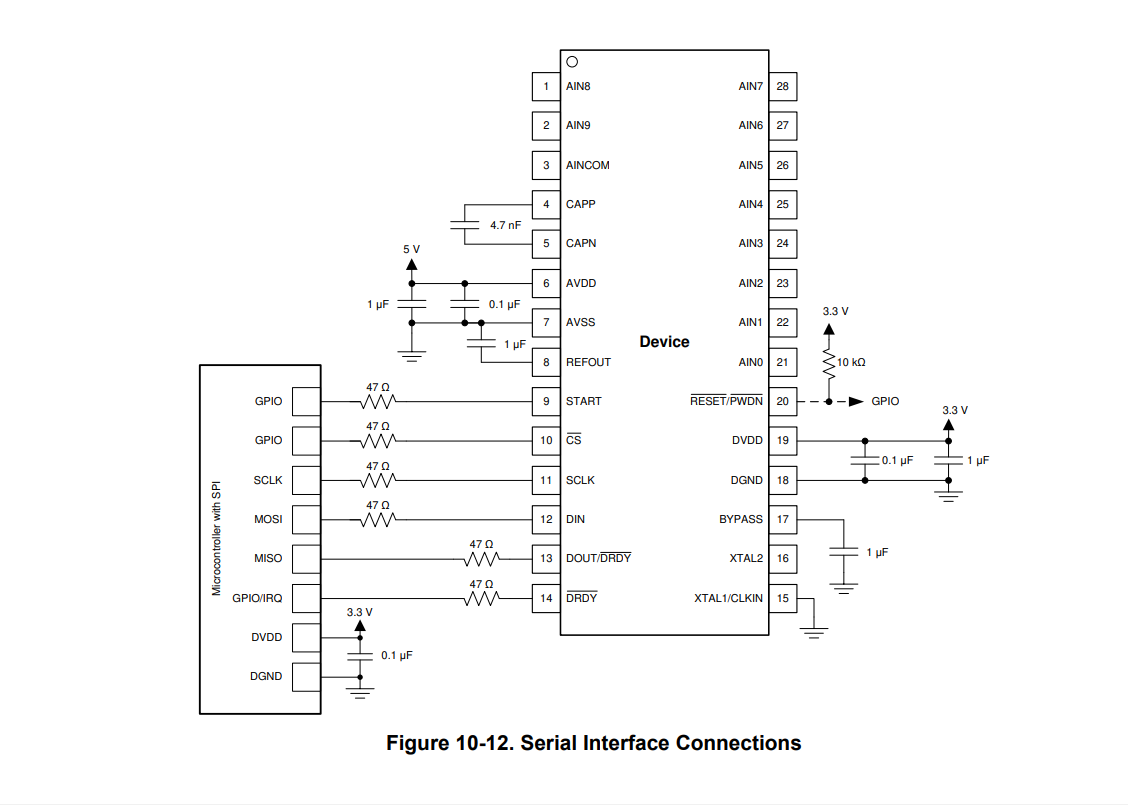
1. **L9110**



1. **ADS1263 ADC**

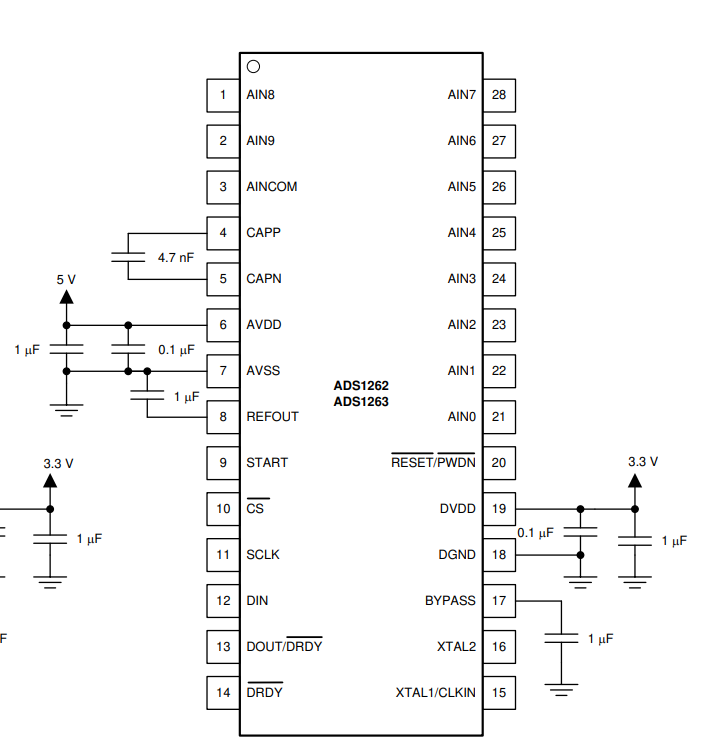


**Serial Interface Connections Noted**



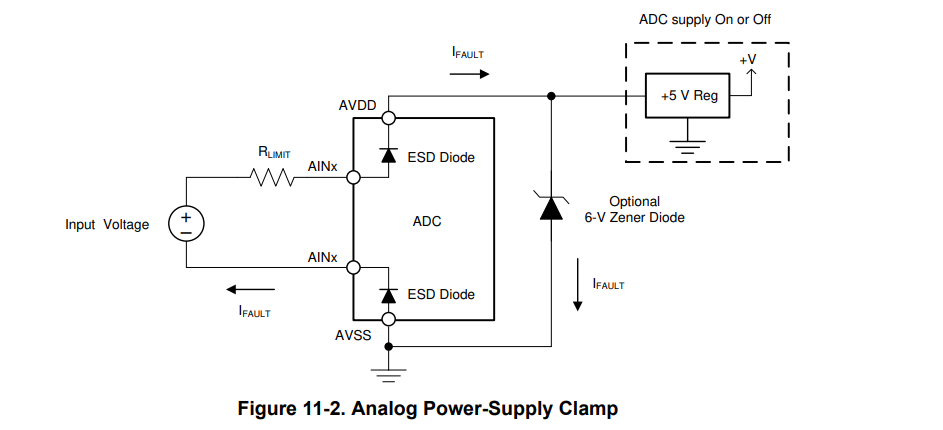
**11 Power Supply Recommendations**

The ADS1262 and ADS1263 require an analog power supply (VAVDD, VAVSS) and digital power supply (VDVDD). The analog power supply can be bipolar (for example, VAVDD = +2.5 V, VAVSS = –2.5 V) or unipolar (for example, VAVDD = 5 V, VAVSS = 0 V). The digital supply (VDVDD) range is 2.7 V to 5.25 V. The digital supply voltage determines the digital I/O logic levels. Keep in mind that the GPIO logic levels (AIN3-AINCOM) are referenced to the analog supply voltage and may be different from the digital I/O logic level. **Noted**



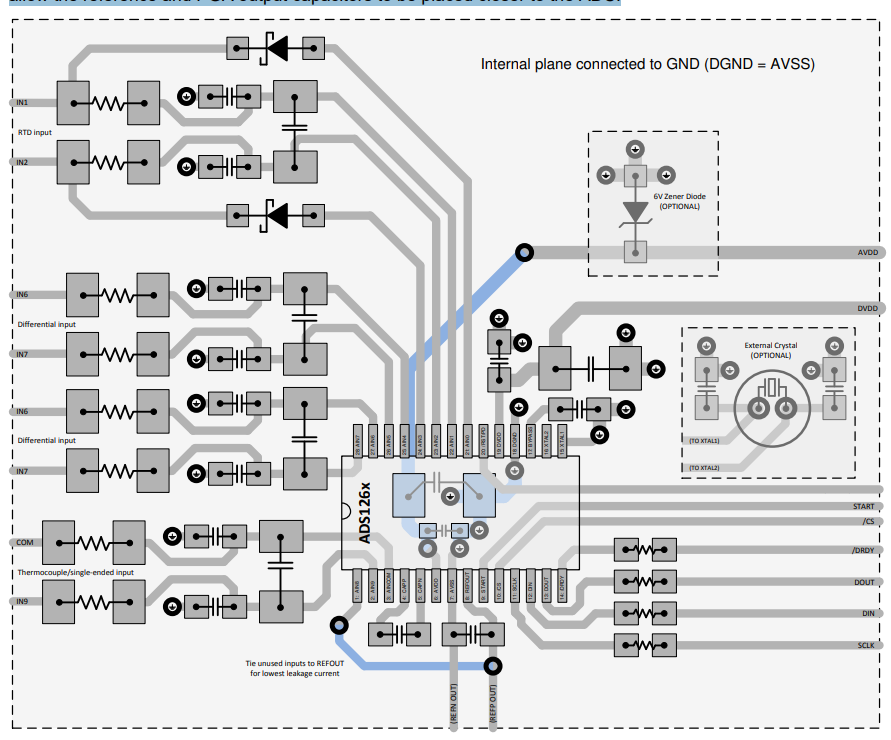
**11.2 Analog Power-Supply Clamp Noted**

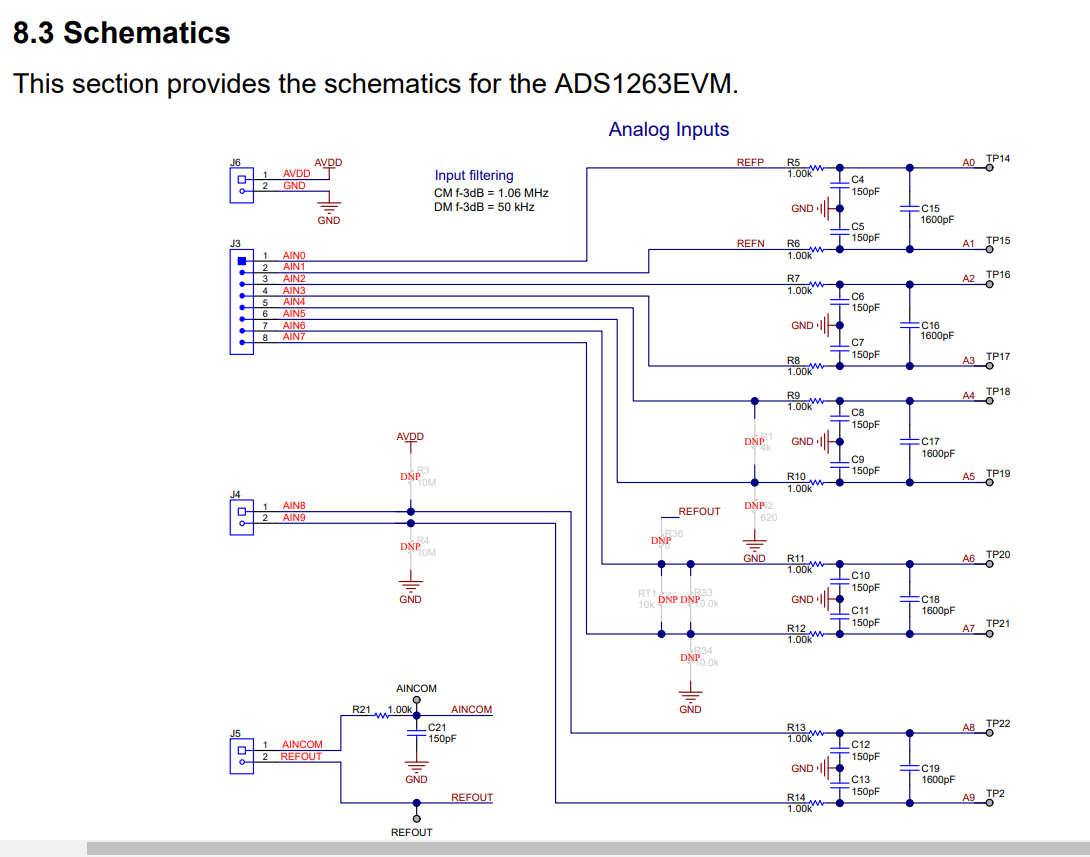
It is important to evaluate circumstances when an input signal is present while the ADC is powered and unpowered. When the input signal exceeds the power-supply voltage, it is possible to back drive the analog power-supply voltage with the input signal through a conduction path of the internal ESD diodes. Back driving the ADC power supply can also occur when the power-supply voltage is on.



**12.1 Layout Guidelines**

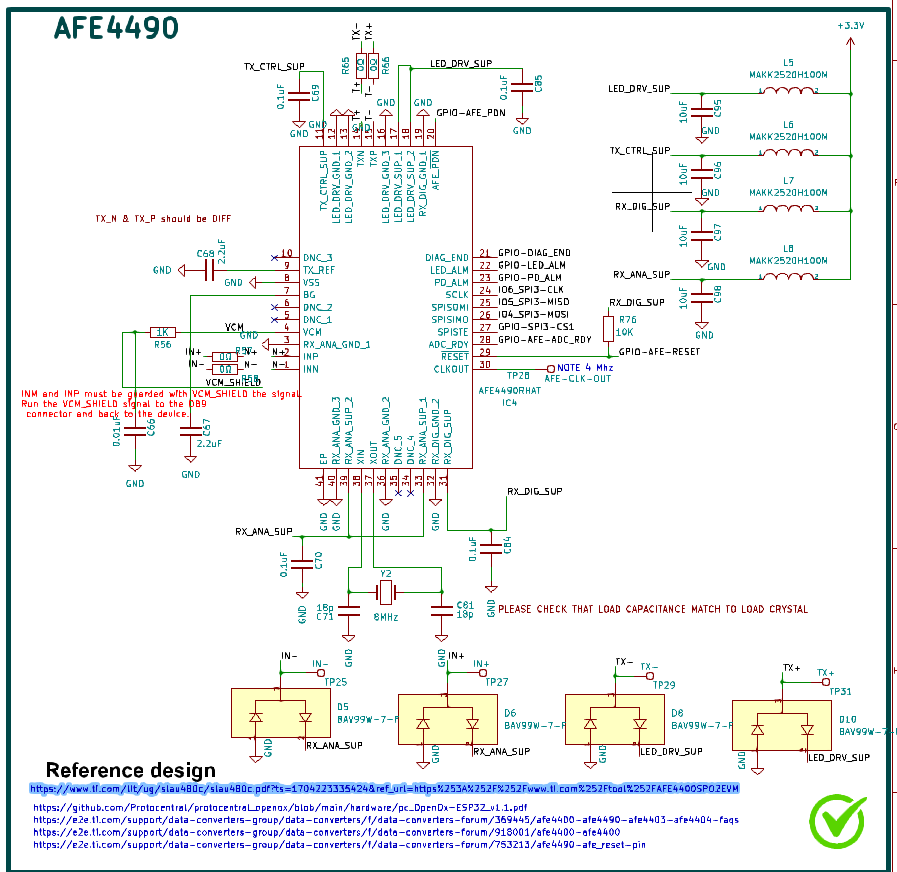
* 1. The ground must be a low impedance connection for return currents to flow undisturbed back to their respective sources. Keep connections to the ground plane as short and direct as possible. When using vias to connect to the ground layer, use multiple vias in parallel to reduce impedance to ground. **Noted**
  2. A mixed-signal layout sometimes incorporates separate analog and digital ground planes that are tied together at one location; however, separating the ground planes is not necessary when analog, digital, and power supply components are properly placed. Proper placement of components partitions the analog, digital, and power supply circuitry into different PCB regions to prevent digital return currents from coupling into sensitive analog circuitry. **Noted**
  3. Supply pins must be bypassed with a low-ESR ceramic capacitor. Place the bypass capacitors as close as possible to the supply pins using short, direct traces. For optimum performance, use low-impedance connections on the the ground-side connections of the bypass capacitors. **Noted**
  4. Flow the supply current through the bypass capacitor pin first and then to the supply pin to make the bypassing most effective (also known as a Kelvin connection). **Noted**
  5. If multiple ADCs are on the same PCB, use wide power supply traces or dedicated power-supply planes to minimize the potential of crosstalk between ADCs. **Noted**
  6. For the ADC CAPP and CAPN pins, place the 4.7-nF C0G capacitor close to the pins using short direct traces. **Noted**
  7. . Route digital circuit traces (such as clock signals) away from all analog pins. Note the internal reference output return shares the same pin as the AVSS power supply. To minimize coupling between the power-supply trace and reference-return trace, route the two traces separately; ideally, as a star connection at the AVSS pin. **Noted**
  8. If a four-layer PCB is used, dedicate the additional inner layers to route power traces. The ADC orientation is shown left to right to minimize crossover of the analog and digital signal traces. The PCB is partitioned with analog signals routed from the left, digital signals routed to the lower-right, and power routed from the upper-right. Analog supply bypass capacitors are placed opposite to the ADC on the bottom layer to allow the reference and PGA output capacitors to be placed closer to the ADC. **Noted**

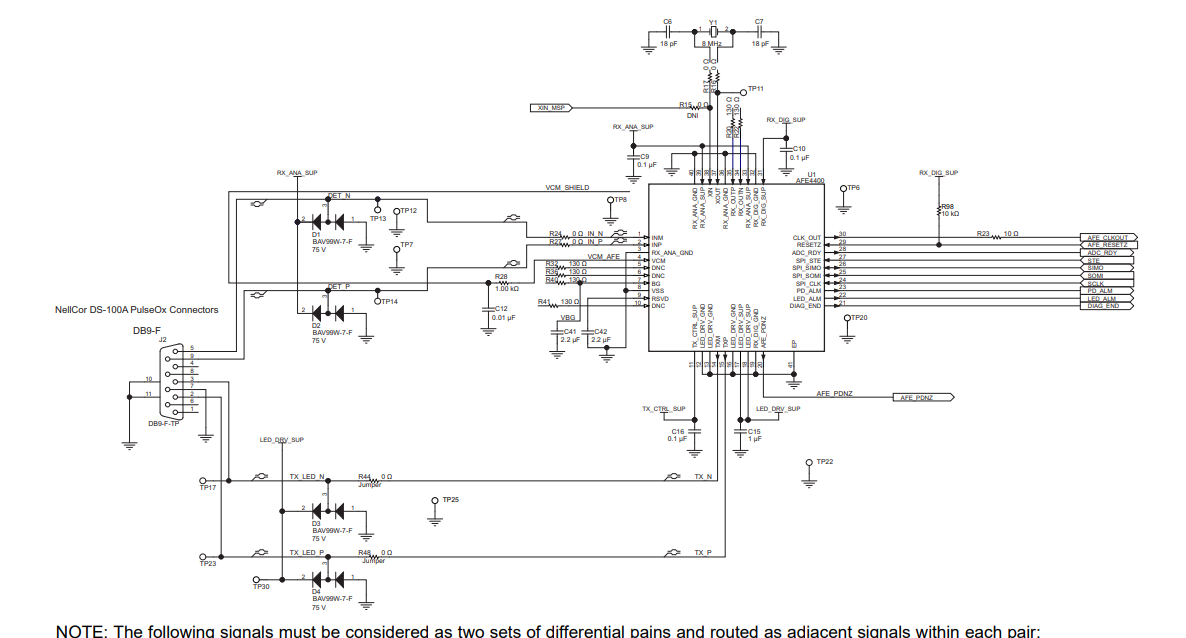




* 1. <https://www.ti.com/lit/ug/sbau206b/sbau206b.pdf?ts=1707293173812>
  2. <https://www.ti.com/lit/ds/sbas661c/sbas661c.pdf?ts=1707308577661&ref_url=https%253A%252F%252Fwww.ti.com%252Ftool%252FADS1263EVM-PDK>
  3. <https://files.waveshare.com/upload/f/f7/High-Precision_AD_HAT.pdf>

**AFE4490**





**Power-Supply Recommendations**

* 1. The AFE4490 has two sets of supplies: the receiver supplies (RX\_ANA\_SUP, RX\_DIG\_SUP) and the transmitter supplies (TX\_CTRL\_SUP, LED\_DRV\_SUP). The receiver supplies can be between 2.0 V to 3.6 V whereas the transmitter supplies can be between 3.0 V to 5.25 V. Another consideration that determines the minimum allowed value of the transmitter supplies is the forward voltage of the LEDs being driven. The current source and switches inside the AFE require voltage headroom that mandates the transmitter supply to be a few hundred millivolts higher than the LED forward voltage. TX\_REF is the voltage that governs the generation of the LED current from the internal reference voltage. Choosing the lowest allowed TX\_REF setting reduces the additional headroom required but results in higher transmitter noise. Other than for the highest end clinical SPO2 applications, this extra noise resulting from a lower TX\_REF setting might be acceptable. **Noted**
  2. The LED\_DRV\_SUP and TX\_CTRL\_SUP are recommended to be tied together to the same supply (between 3.0 V and 5.25 V). The external supply (connected to the common anode of the two LEDs) must be high enough to account for the forward drop of the LEDs as well as the voltage headroom required by the current source and switches inside the AFE. In most cases, this voltage is expected to fall below 5.25 V; thus the external supply can be the same as the LED\_DRV\_SUP. However, there might be cases (for instance when two LEDs are connected in series) where the voltage required on the external supply is higher than 5.25 V. Such a case must be handled with care to ensure that the voltage on the TXP and TXN pins stays less than 5.25 V and also never exceeds the supply voltage of LED\_DRV\_SUP, TX\_CTRL\_SUP by more than 0.3 V. **Noted**

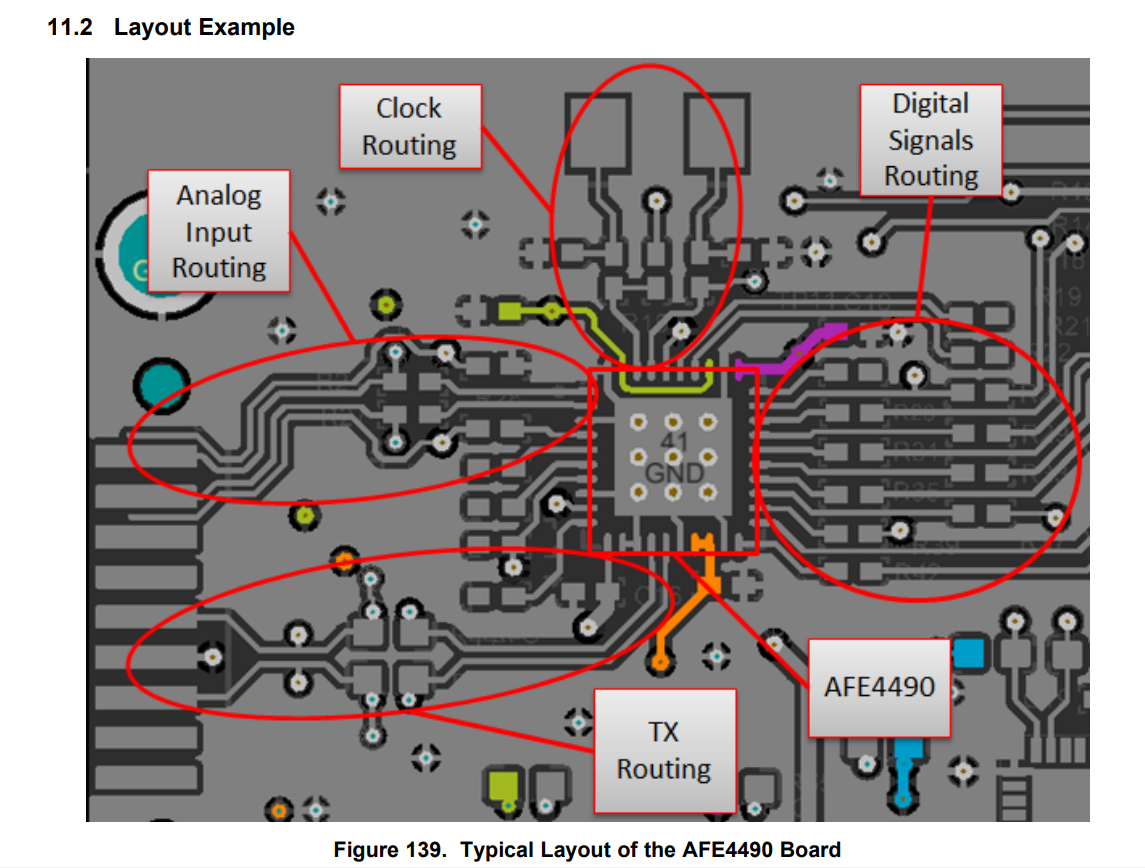
**Layout 1 Layout**

Guidelines Some key layout guidelines are:

**1. TXP, TXN are fast switching lines and must be routed away from sensitive reference lines as well as from the INP, INN inputs.**

**2. If required to route long, TI recommends that the VCM be used as a shield for the INP, INN lines.**

**3. The device can draw high switching currents from the LED\_DRV\_SUP pin. Therefore, having a decoupling capacitor electrically close to the pin is recommended**

* 1. <https://www.ti.com/lit/ug/slau480c/slau480c.pdf?ts=1704223335424&ref_url=https%253A%252F%252Fwww.ti.com%252Ftool%252FAFE4400SPO2EVM>
  2. <https://e2e.ti.com/support/data-converters-group/data-converters/f/data-converters-forum/753213/afe4490-afe_reset-pin>
  3. <https://github.com/Protocentral/protocentral_openox/blob/main/hardware/pc_OpenOx-ESP32_v1.1.pdf>

|  |  |  |
| --- | --- | --- |
| **ESP32-S3** | **PINS** | **DEVICES** |
| I2C-1 | (**MTCK**) – GPIO\_39- GPIO-ALERT-TMP117  (**IO8\_SDA1**) – GPIO\_8- SDA  (**IO8\_SCL1**) – GPIO\_9- SCL | CONNECTED TO **TMP117** |
| **SPI3** | (**IO35\_SPI2-MOSI`**)  - Pin  A0   TX  (**RX4**) - Pin   D0   RX  (**RTS4**) - Pin B14 RTS  (**CTS4**) - Pin B0   CTS  (**GPIO**) - Pin B1    Reset  (**GPIO**) - Pin F12   PWR\_CTR  (**GPIO**) - Pin F11    EN  (**GPIO**) - Pin E6    ON/OFF  (**GPIO**) - Pin A6    status | CONNECTED TO **ADS1263** |
| USART**5** | (**TX5**) - Pin  B6   TX  (**RX5**) - Pin  B5   RX | CONNECTED TO **AFE4490** |
| USART3 | (**TX3**)   - Pin B10 TX  (**RX3**)   - Pin D9   RX  (**GPIO**) - Pin D14 M0  (**GPIO**) - Pin D15 M1  (**GPIO**) - Pin F14  AUX | CONNECTED TO VALE&MOTOR |
| USART**5** | (**TX5**) - Pin  B6   TX  (**RX5**) - Pin  B5   RX | CONNECTED TO **ICM20948** |
| USART**5** | (**TX5**) - Pin  B6   TX  (**RX5**) - Pin  B5   RX | CONNECTED TO **Pressure sensor** |
| USART**5** | (**TX5**) - Pin  B6   TX  (**RX5**) - Pin  B5   RX | CONNECTED TO **SD-CARD** |
|  |  | CONNECTED TO **SPI-CONNECTOR** |
|  |  | CONNECTED TO **RGB-LED** |
|  |  | CONNECTED TO **Fuel Gauge** |
|  |  | CONNECTED TO **I2C-connectors** |

