Design of Area Efficient Low Latency 5G Compliant LDPC Decoder Architecture

***Abstract*—This paper proposes a low-complexity check node unit architecture for 5G new radio (5G-NR) compliant low-density parity-check (LDPC) decoder. The complexity of the check node unit architecture is reduced by computing the first minimum value in the conventional way and second minimum value by adding a small value alpha (α) to first minimum value. The bit error rate (BER) versus signal to noise ratio (SNR) performance analysis graph shows that this second minimum approximation (SMA) decoding method gives a reasonable error while comparing it with conventional min-sum and offset min-sum decoding methods. A novel architecture is presented and synthesized on Xilinx Artix-VII FPGA board. The synthesis results show that proposed design provides 45.5% reduction in number of LUTs along with 24.8% reduction in data path delay than state-of-the-art architectures. Thus, the proposed check node unit architecture with second minimum approximation decoding algorithm outperforms all the other existing architectures.**

***Index Terms*—Low-density Parity-Check (LDPC) codes, Check Node Unit (CNU) architecture, 5G new radio (5G-NR), Communication systems.**

I. Introduction

The information bits are encoded & modulated at the sending side, transmitted through the wireline or wireless channel, and demodulated & decoded at the receiving side. The noise may get added to the encoded information while transmitting and it will cause an error in the received signal. So, the system has to get rid of the error. For that, a better error correcting code is required to make the system resilient from misinformation. Low density parity check (LDPC) codes are considered to be a better error correcting code for the past several decades. They are introduced by R. Gallager [1] in 1962 which is not so prevalent at that time. Later, they are rediscovered by Mackay [2] in 1999 and reported that they have performance capacity near Shannon limit. Consequently, they have become one of the most efficient techniques for error correction. They have applications in wireless communication systems, 5G new radio (5G-NR), digital video broadcast (DVB), and space systems.

The LDPC codes have high degree of parallelism. They are represented with the help of $M \times N$ sparse parity check matrix (PCM) H as well as Tanner Graph. The example PCM with 4 rows and 6 columns; consists of 1's and 0's is shown in the Equation (1).

$$A = \begin{pmatrix} 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 \end{pmatrix} \tag{1}$$

The corresponding Tanner Graph representation is shown in Fig. 1. The columns which are also known as variable nodes (VN); are denoted by using the variables $C1, C2, \cdots C6$. The rows which are also known as check nodes (CN); are denoted by using the variables $R1, R2, \cdots R4$. The line connecting the VN and CN are termed as edges and these are based on the position of non-zero elements of parity check matrix (H). The number of lines (edges) connected to each node is known as node's degree. The decoding of the LDPC codes are performed by iteratively generating and exchanging messages between the variable nodes and check nodes, via the lines of the Tanner graph. There are different decoding algorithms and schedules to determine the specific operation of each node, the format of the messages and the order in which they are exchanged.

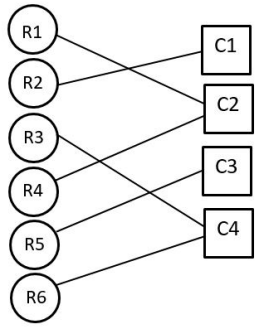

Fig. 1. Tanner Graph

In this research work, the focus is to design the novel check node unit (CNU) architecture and to replace the existing CNU architecture of LDPC decoder with it. This will improve the performance of the complete decoder with reduced area and latency. The conventional CNU architectures compute both the first & second minimum values and exchange it with the variable node unit (VNU) which requires more resources. In order to reduce the usage of resources, the novel architecture computes only the first minimum in the conventional way and the second minimum is computed by adding a small value alpha (α) to it.

Rest of this paper is organized as follows: Section II presents the related work. The proposed novel CNU architecture is discussed in Section III. The results are analyzed in Section IV. Finally, the conclusion of the paper is given in Section V.

II. Related Work

The LDPC decoder design requires the efficient way to compute the first and second minimum values from the given set of inputs. The computation of the first minimum value is easier; but the computation of the second minimum requires a better and efficient hardware architecture. There are two basic methods to find the first two minimums from the given inputs like sorting-based approach and tree-based approach [3]. Basically, the sorting based approach requires less number of comparisons and tree based approach achieves higher speed at lower hardware cost.

The sum-product decoding algorithm has high performance metrics and in turn it requires high hardware resources also than any other decoding algorithms. In order to achieve high throughput even with high hardware resource usage a multi-core architecture is proposed [4]. But the cost of the system will be high, if a multicore architecture is used. Therefore, to avoid it, the conventional min-sum decoding algorithm with reduced hardware complexity is introduced. These traditional decoding algorithms for LDPC codes generate and exchange messages between check node and variable node only based on loglikelihood ratio (LLR) of bits, and correlations introduced by modulation are not utilized. In [5], symbol based approach is used $i.e.$ the correlation factor introduced while modulating the signals are taken into account which results in an alternative low-cost way to better utilize available information. These symbol based sum product and min sum (S-SPA and S-MSA) achieve better error correcting performance than conventional decoding algorithm.

In order to reduce the cost and optimize the throughput, the generated messages are stored using a lower precision by truncating some bits [6]. The truncation happens only after the generated messages are updated by the processing units. The pipeline architectures are faster than the conventional architectures provided the data and control hazards are not there. But, all the pipeline architectures have these two hazards as bottlenecks. The conflicts occurred due to these bottlenecks are addressed in [7] by providing a flooding schedule.

Though the min-sum decoding algorithm has reduced hardware complexity, it also has reduced performance metrics. To overcome this, the offset min-sum [8] - [11] and normalized min-sum [12] decoding algorithms are introduced. The physical layer of the telecommunication systems are evolving rapidly, so the reprogrammable FPGA based implementation [9] of the 5G LDPC decoders are required. It will reduce the cost and time to implement such physical layers. Further, the length of the cycles is measured to change the number of iterations dynamically is proposed in [13] as reweighted offset min-sum algorithm (ROMS).

III. Proposed Check Node Unit Architecture

The architecture of the proposed CNU consists of three major building blocks such as minimum value computation unit (MVCU), sign computation unit (SU), and two's complement to sign magnitude/sign magnitude to two's complement unit (TCSM/SMTC) which are detailed in the following subsections.

A. Minimum Value Computation Unit

The basic building block of MVCU is 20-input minimum value unit (MVU-20). It is designed using 2-input minimum value unit (MVU) as shown in Fig. 2. It compares two 5-bit inputs and gives the minimum value and index as outputs.

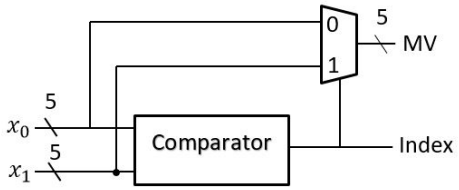

Fig. 2. Architecture of 2-input minimum value unit

The index value is computed by comparing two inputs using comparator and MV is computed based on the index value with the help of 2:1 multiplexer as shown in 2 and 3 respectively.

$$Index = \begin{cases} 0, & \text{if } x_0 < x_1. \\ 1, & \text{otherwise.} \end{cases} \tag{2}$$

$$mv = \begin{cases} x_0, & \text{if } Index = 0. \\ x_1, & \text{otherwise.} \end{cases} \tag{3}$$

The 4-input minimum value unit is shown in Fig. 3. It consists of three 2-input MVUs and an adder. The two 2-input MVUs which are named as A and B are used to compute the minimum values from the given inputs and the third MVU is used to compute the minimum of mv_A and mv_B. The output of the third MVU is considered as first minimum min_1. The second minimum value min_2 is computed by adding a small value alpha (α) to the first minimum.

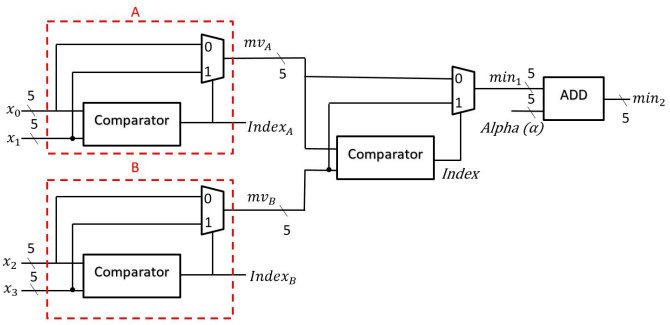

Fig. 3. Architecture of 4-input minimum value unit

Similarly, the 8-input MVU is constructed by using seven 2-input MVUs and an adder. The 16-input MVU is constructed

by using fifteen 2-input MVUs and an adder. In general, the K-input MVU requires (K-1) number of 2-input MVUs and an adder.

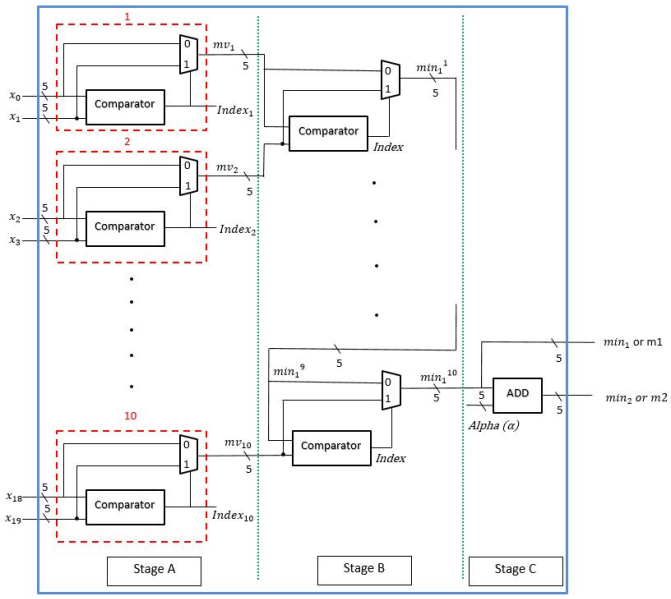

Fig. 4. Architecture of 20-input minimum value unit

Since our design requires 20-input MVU (MVU-20), it can be constructed by nineteen 2-input MVUs and an adder as shown in Fig. 4. The ten 2-input MVUs are considered as stage A where it takes primary inputs and computes the minimum value. The remaining nine 2-input MVUs are considered as Stage B where it takes the intermediate minimum values and computes the first minimum value min_1. The 5-bit adder is considered as stage C where it adds Alpha (α) to first minimum value to compute second minimum value min_2.

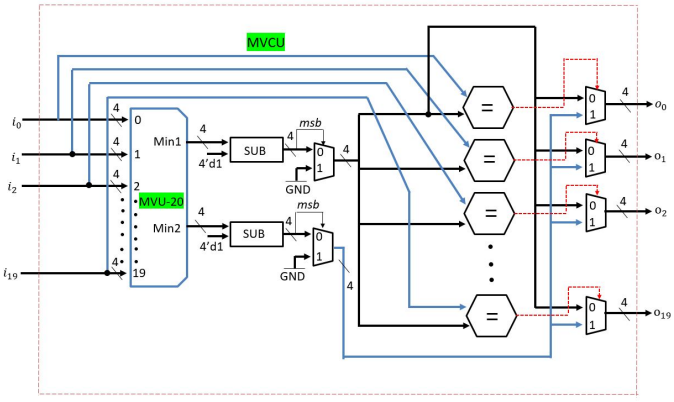

Fig. 5. Minimum value computation unit architecture

Now, the MVU-20 is connected in a manner to construct the MVCU as shown in Fig. 5. It computes first minimum min_1 and second minimum min_2 using the MVU-20 module. It subtracts the offset value $4'b1$ from min_1 and min_2. Then the most significant bit (MSB) is checked to find whether the subtracted value is positive or negative. If the subtracted value is negative, then the output of 2:1 Mux is zero otherwise it is the actual subtracted value. Now, all the output of the MVCU is replaced with min_1 expect the index of min_1; this magnitude of min_1 is replaced by min_2. This is done by using 20 equalizers and 2:1 multiplexers.

B. Sign Unit

The sign unit takes all the MSB of the given inputs and EX-OR those bits to compute a product bit. Then, the product bit is EX-ORed with each MSB to obtain the sign processed outputs as shown in Fig. 6. These sign processed outputs are concatenated with the outputs of MVCU in the MSB position.

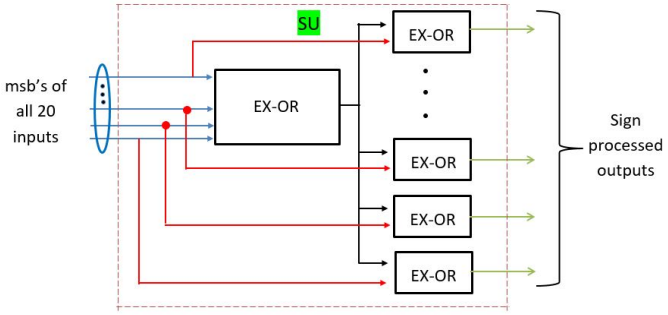

Fig. 6. Sign computation unit architecture

C. TCSM/SMTC

TCSM/SMTC module is used at both the sides of CNU architecture. It takes 5 bits as input and processes the lower 4 bits with the help of a conversion unit (ConU). The simplified Boolean expressions for ConU are given in Eq. 4, Eq. 5, Eq. 6 and Eq. 7 respectively.

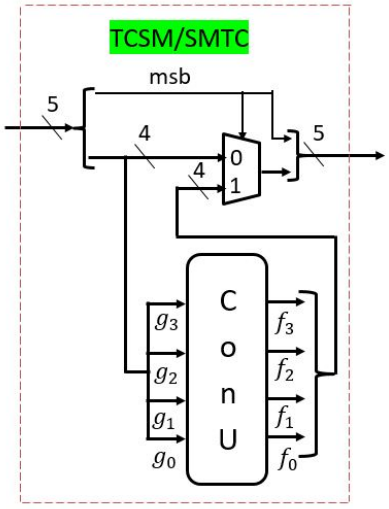

Fig. 7. Architecture of magnitude conversion unit

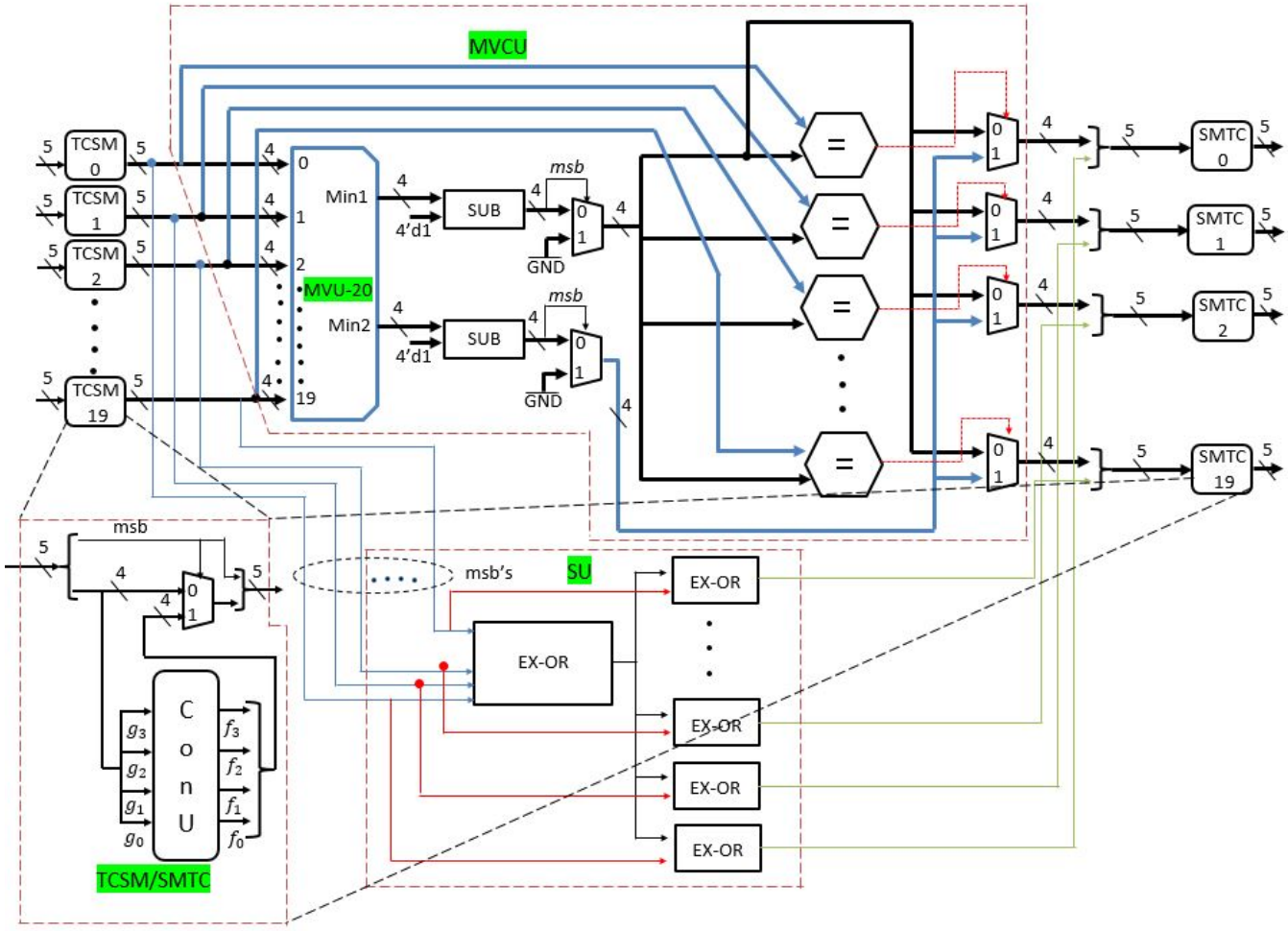

Fig. 8. Proposed novel check node unit architecture

$$f_3 = \bar{g_3}|(\bar{g_2}.\bar{g_1}.\bar{g_0}) \tag{4}$$

$$f_2 = (\bar{g_3}.\bar{g_2})|(\bar{g_2}.g_1)|\bar{g_2}.\bar{g_0})|(g_2.\bar{g_1}.\bar{g_0}) \tag{5}$$

$$f_1 = g_1 \oplus g_0 \tag{6}$$

$$f_0 = g_0 \tag{7}$$

The output of this module is either actual value or converted value based on the value of MSB as shown in Fig. 7.

D. Complete CNU Architecture

All the major modules are interconnected as shown in Fig. 8 to achieve a novel CNU architecture.

IV. Result Analysis

The LDPC decoder behaviour is studied for two conventional decoding algorithms $i.e.$ min-sum (MS) & offset min-sum (OMS) and one proposed decoding algorithm $i.e.$ second minimum approximation (SMA). This study is carried out in MATLAB environment. First, the 5G-NR LDPC codes are encoded and binary phase-shift keying (BPSK) modulated at the sending end. It is transmitted through additive white Gaussian noise (AWGN) Channel. Then, it is BPSK demodulated and decoded at the receiving end. The bit error rate (BER) versus signal to noise ratio (SNR) graph is used to evaluate the performance of the decoder which is shown in Fig. 9. The following graph is plotted for all the above mentioned decoding algorithms for 10 iterations and 20 iterations for the SNR (E_b/N_0) value ranging from 0 to 3 dB.

It is clear from the graph that the BER of conventional MS decoding algorithm is higher than SMA than OMS. It is also to be noted that; as the number of iterations increase, the BER decreases.

The proposed CNU architecture based on SMA decod-

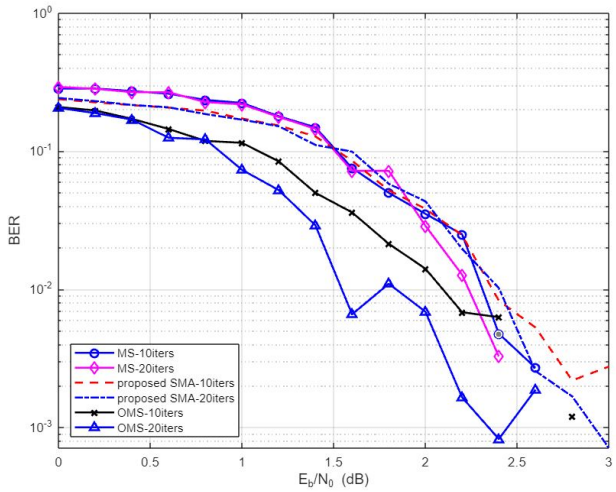

Fig. 9. BER Performance Analysis of LDPC Decoder

ing algorithm is written in Verilog Hardware-Description-Language (HDL) and it is synthesized in Xilinx Artix-VII series of FPGA Board. Table I shows the comparison results of our implementation with the existing CNU architectures. Our proposed design has 45.5% and 22.02% reduction in number of LUTs than [8] & [11] and [10] respectively. It also has 24.8% and 16.7% reduction in data path delay than [8] & [11] and [10] respectively.

TABLE I
HARDWARE UTILIZATION COMPARISON REPORT

Metrics	[8] & [11]	[10]	Proposed Work
No. of word length (bits)	5	5	5
Core Area (No. of LUTs used)	493	345	269
Data Path Delay (ns)	20.12	18.17	15.13

Thus, the proposed CNU architecture with SMA decoding algorithm outperforms all the other existing architectures.

V. CONCLUSION

In this paper, an area efficient low latency check node unit architecture for 5G new radio (5G-NR) compliant LDPC decoder is proposed. This can be achieved by computing only the first minimum value in a conventional way. The second minimum value is approximately computed. The bit error rate graph is also simulated in MATLAB to calculate the error occurred while approximating. But, the SMA decoding method gives a reasonable error while comparing it with conventional min sum and offset min sum decoding methods. The proposed architecture is synthesized on Xilinx Artix-VII series of FPGA board and the results are also compared with the existing architectures. It is clear from the table that our proposed work has used less area and consumed less time than the existing architectures.

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