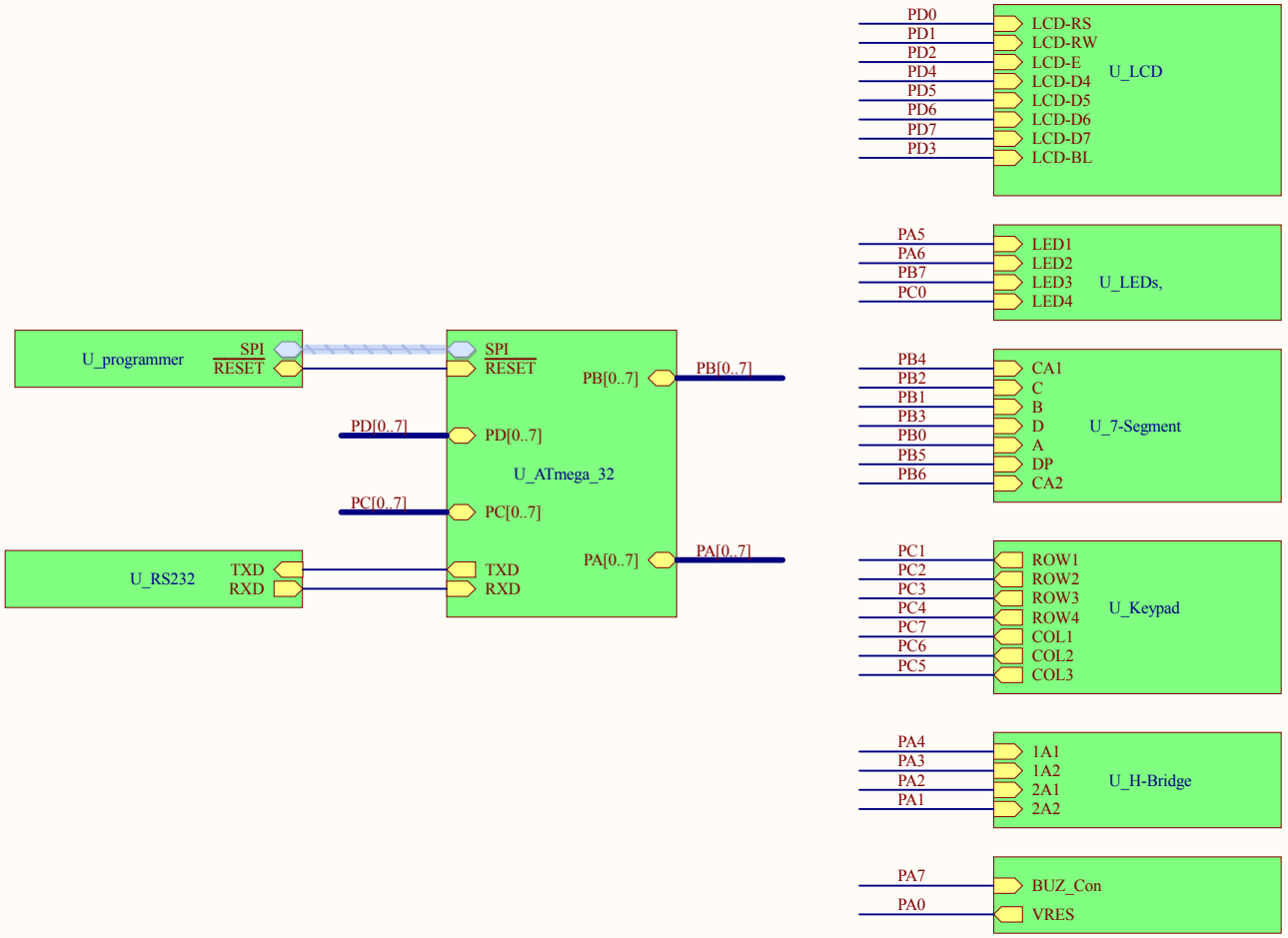
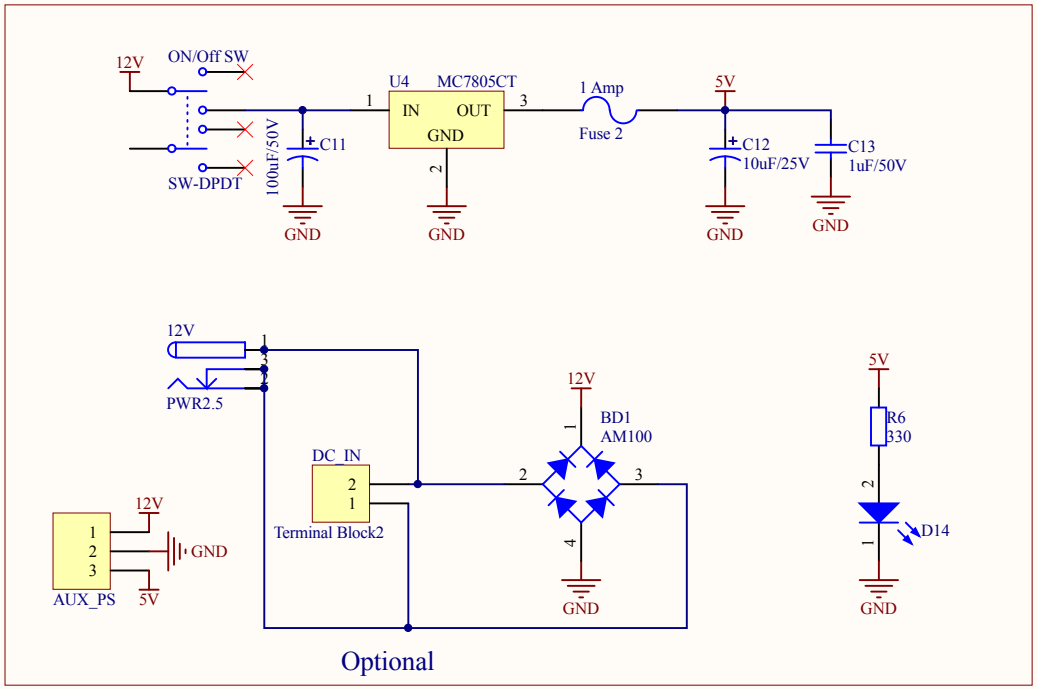
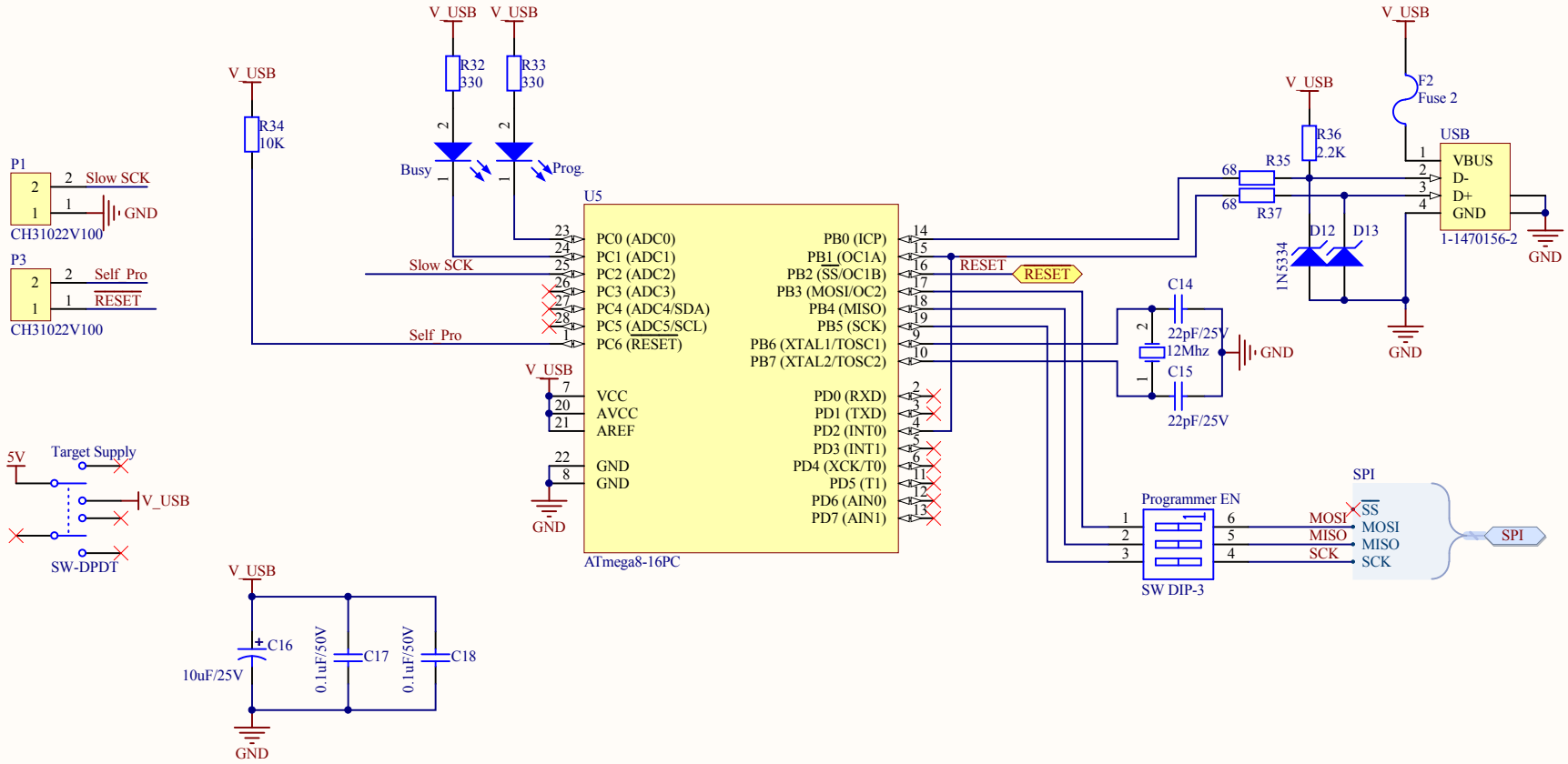


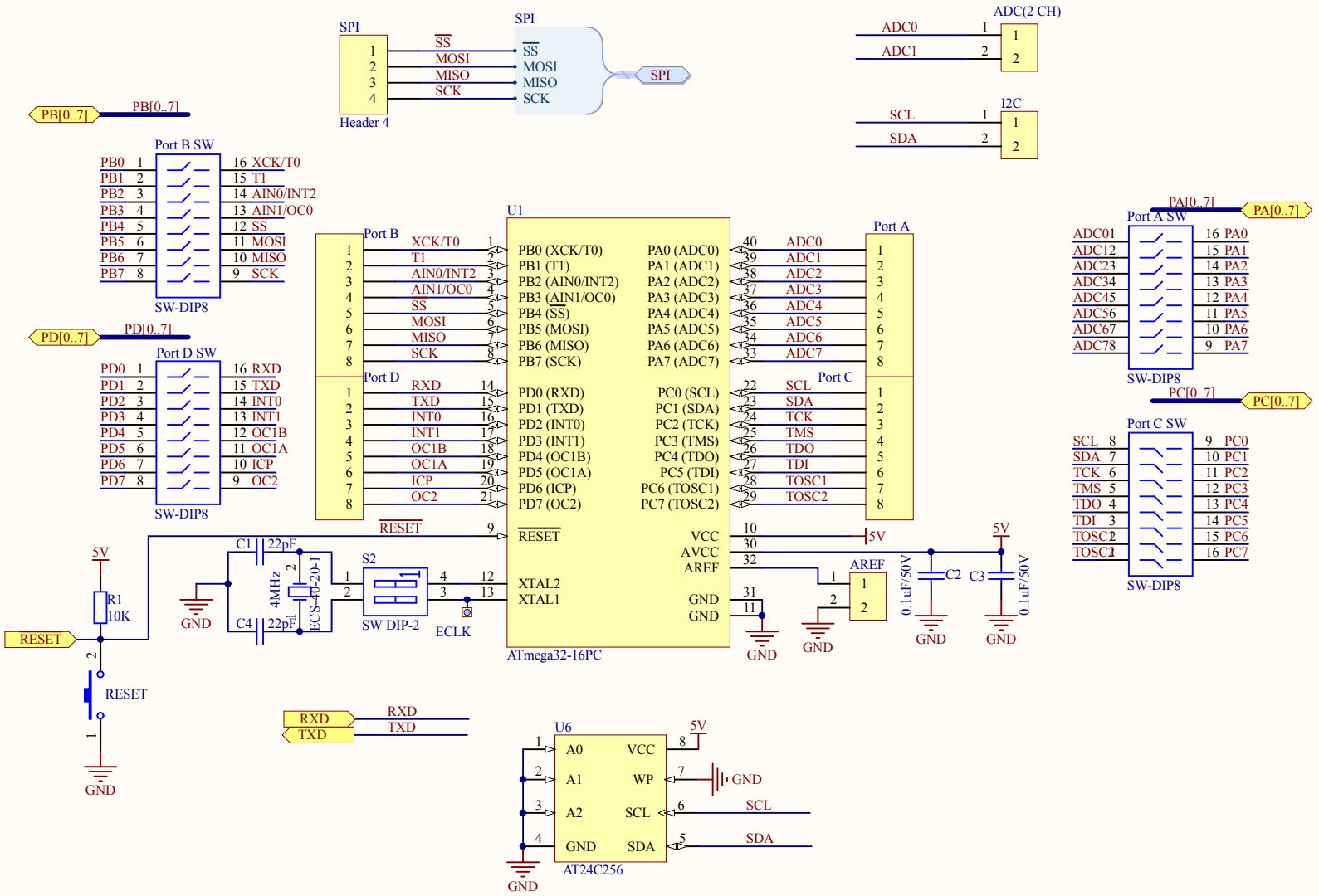
Task:	ATmega_32 Kit
Developer: *Eng. F. Elsisy*	Designer: *Eng. F. Elsisy*
Date: 29/11/2012 Time: 11:12:32 ص	Sheet 1 of 11
File: Master.SCHDOC	

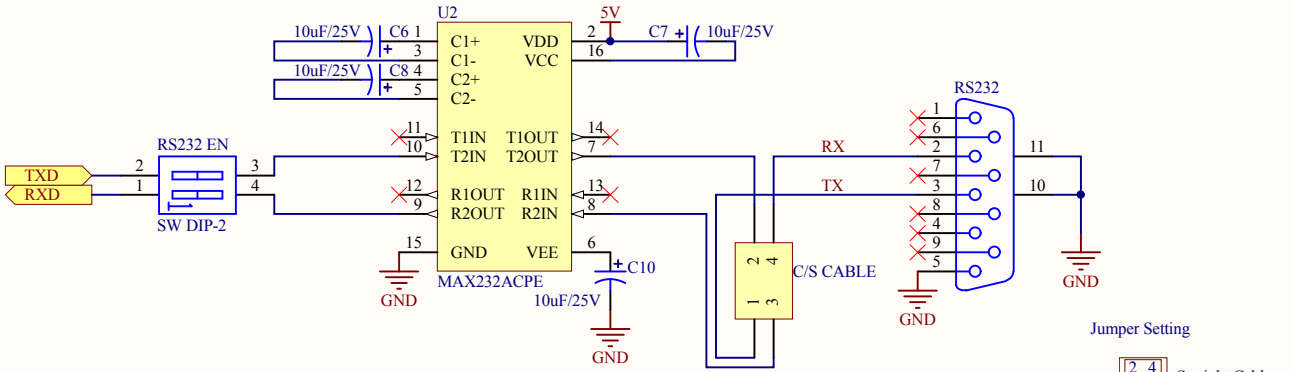


Task:	ATmega_32 Kit
Developer: *Eng. F. Elsisy*	Designer: *Eng. F. Elsisy*
Date: 29/11/2012 Time: 11:12:32 ص	Sheet 2 of 11
File: Power Supply.SCHDOC	



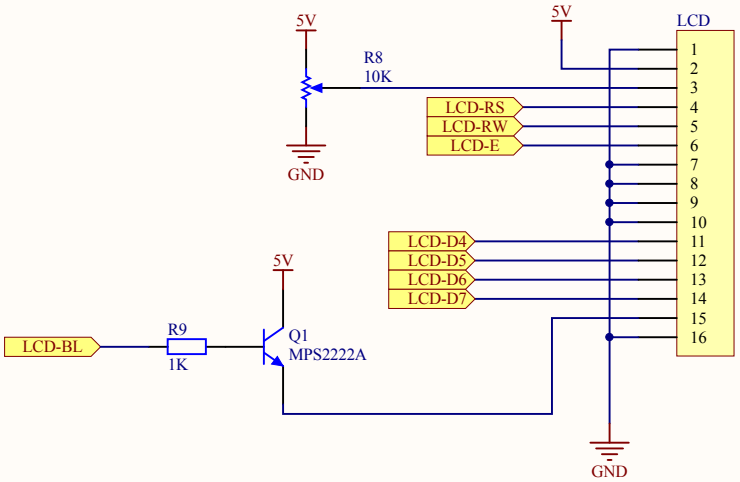
Task:	ATmega_32 Kit
Developer:	*Eng. F. Elsisy*
Designer:	*Eng. F. Elsisy*
Date:	29/11/2012
Time:	11:12:32 ص
Sheet	3 of 11
File:	programmer.SCHDOC


SPI
Header 4
SS
MOSI
MISO
SCK
SPI
ADC(2 CH)
ADC0
ADC1
I2C
SCL
SDA
PB[0..7]
Port B SW
SW-DIP8
PD[0..7]
Port D SW
U1
Port B
Port D
Port A
Port C
PA[0..7]
Port A SW
PC[0..7]
Port C SW
RESET
XTAL2
XTAL1
VCC
AVCC
AREF
GND
ATmega32-16PC
C1 22pF
C4 22pF
4MHz
ECS-40-20-1
S2
SW DIP-2
ECLK
R1 10K
C2
C3
0.1uF/50V
5V
RXD
TXD
U6
A0
A1
A2
GND
VCC
WP
SCL
SDA
AT24C256
Task: ATmega_32 Kit
Developer: Eng. F. Elsisy
Designer: Eng. F. Elsisy
Date: 29/11/2012 Time: 11:12:32 ص Sheet 4 of 11
File: ATmega_32.SCHDOC



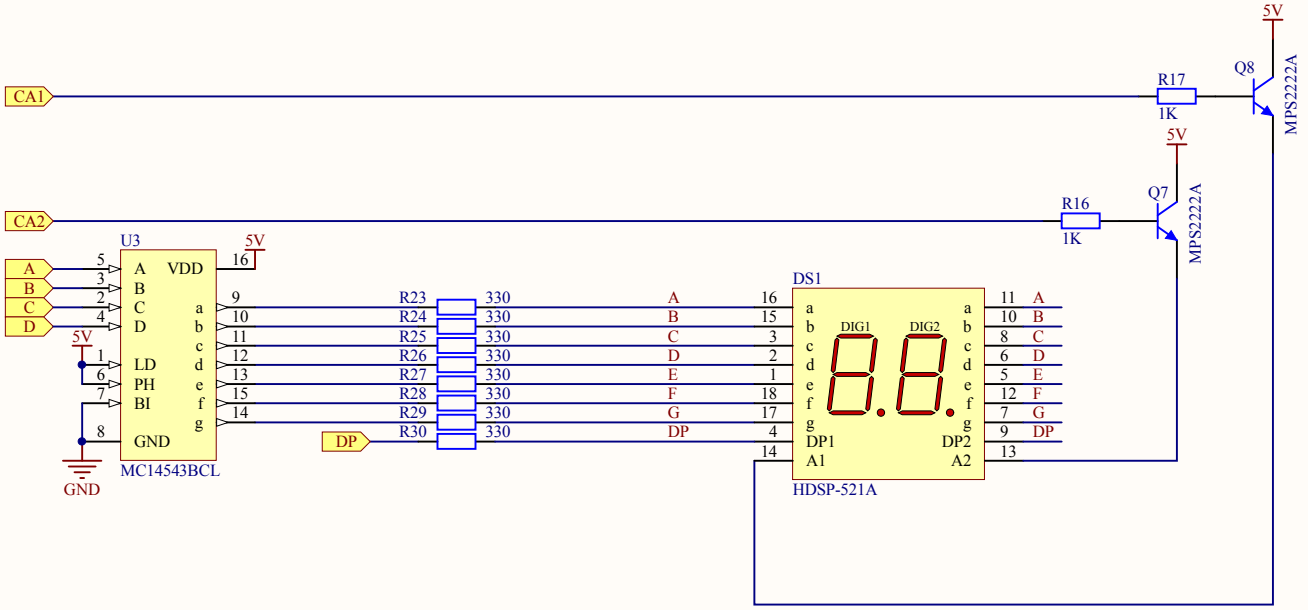
RS232

Task:	ATmega_32 Kit		
Developer:	*Eng. F. Elsisy*	Designer:	*Eng. F. Elsisy*
Date: 29/11/2012	Time: 11:12:33 ص	Sheet 5 of 11	
File: RS232.SCHDOC			

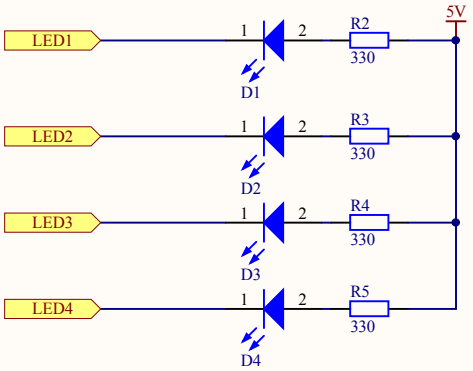


LCD 16x2

Task:	ATmega_32 Kit		
Developer:	*Eng. F. Elsisy*	Designer:	*Eng. F. Elsisy*
Date: 29/11/2012	Time: 11:12:33 ص	Sheet 6 of 11	
File: LCD.SCHDOC			

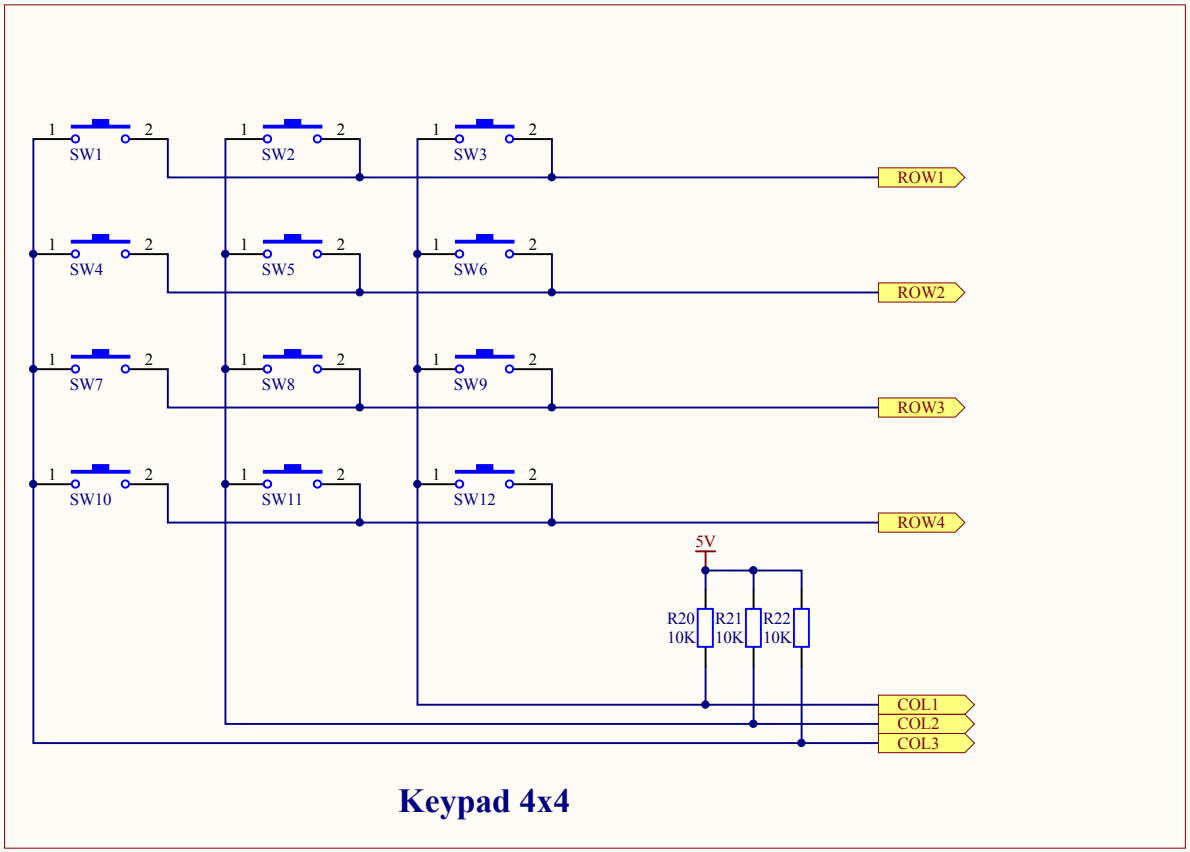


Task:	ATmega_32 Kit		
Developer:	*Eng. F. Elsisy*	Designer:	*Eng. F. Elsisy*
Date: 29/11/2012	Time: 11:12:33 ص	Sheet 7 of 11	
File: 7-Segment.SCHDOC			



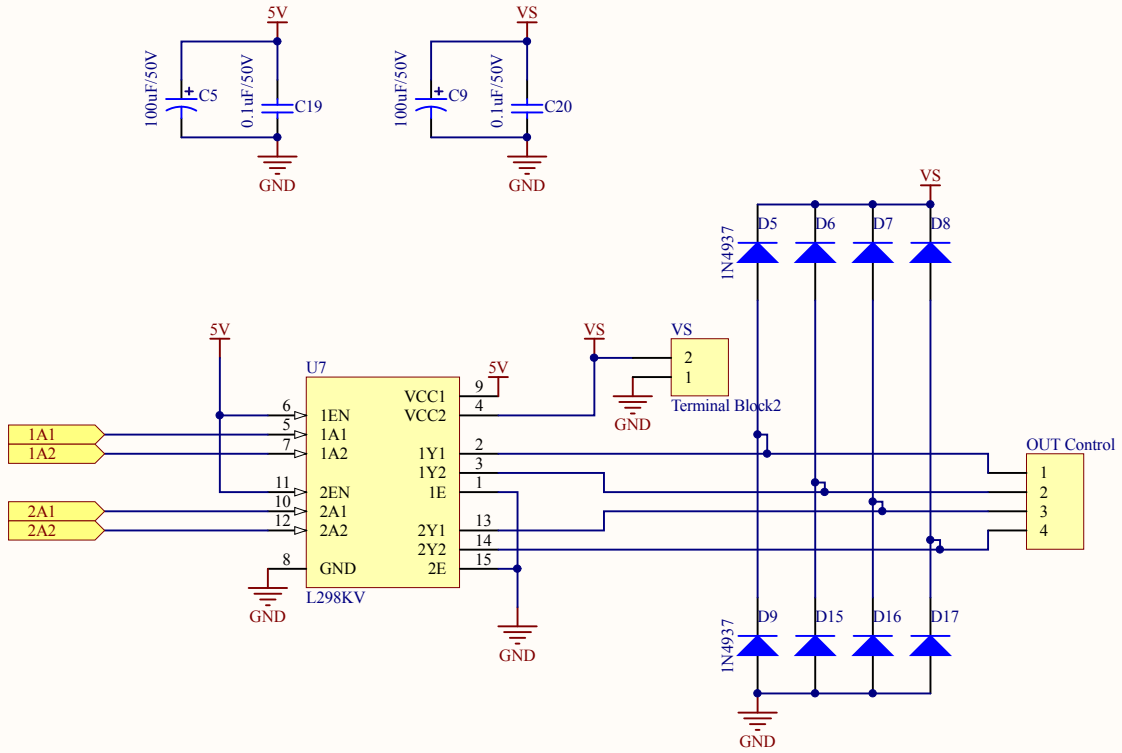
LEDs

Task:	ATmega_32 Kit		
Developer:	*Eng. F. Elsisy*	Designer:	*Eng. F. Elsisy*
Date: 29/11/2012	Time: 11:12:33 ص	Sheet 8 of 11	
File: LEDs,.SCHDOC			

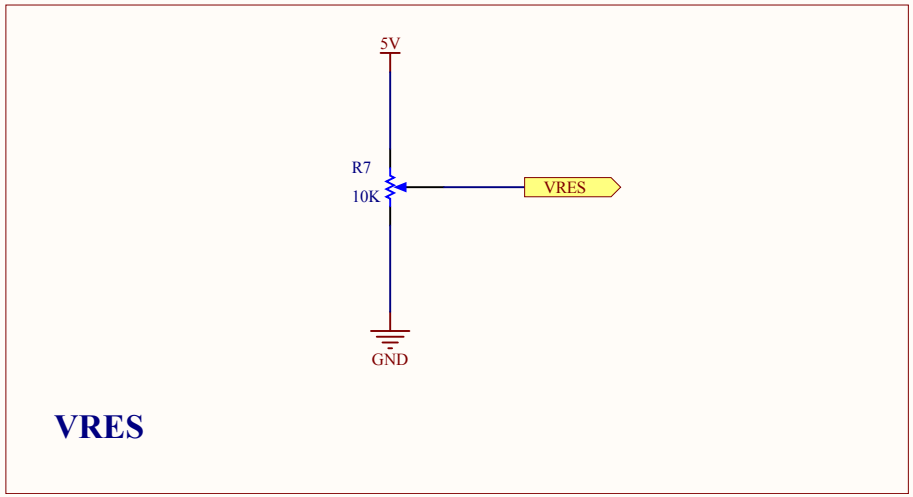


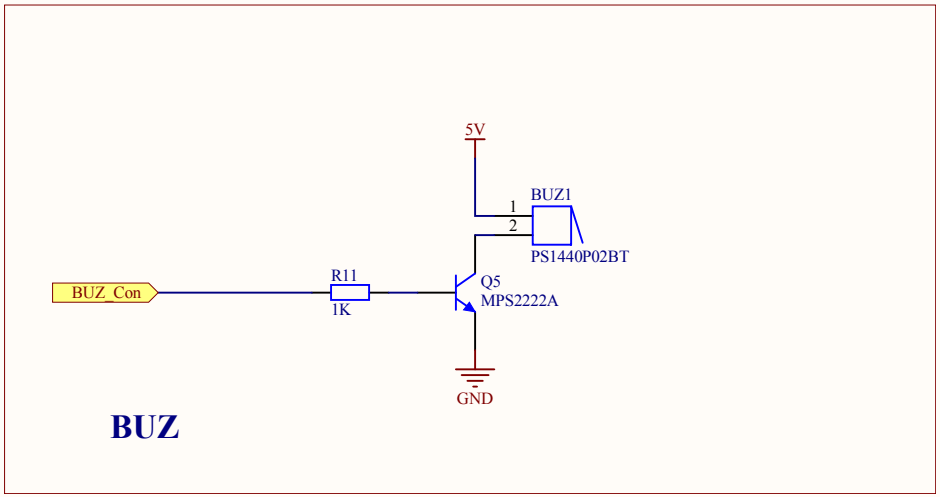
Keypad 4x4

Task:	ATmega_32 Kit
Developer: *Eng. F. Elsisy*	Designer: *Eng. F. Elsisy*
Date: 29/11/2012 Time: 11:12:33 ص	Sheet 9 of 11
File: Keypad.SCHDOC	



Task:	ATmega_32 Kit
Developer: *Eng. F. Elsisy*	Designer: *Eng. F. Elsisy*
Date: 29/11/2012 Time: 11:12:33 ص	Sheet 10 of 11
File: H-Bridge.SCHDOC	





Task:	ATmega_32 Kit		
Developer:	*Eng. F. Elsisy*	Designer:	*Eng. F. Elsisy*
Date: 29/11/2012	Time: 11:12:33 ص	Sheet 11 of 11	
File: VRES and Buzer.SCHDOC			