RCC Driver for STM32F103

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Chapter 1

File Index

1.1 File List

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Chapter 2

File Documentation

2.1 DRCC/DRCC.c File Reference

This file is the Implementation for RCC Driver for STM32F103.

```
#include "STD_TYPES.h"
#include "DRCC.h"
```

Macros

- #define DRCC_BASE_ADDRESS 0X40021000

  Base Address of RCC Peripheral

- #define **RCC_CR** ∗((uint_32t ∗)(DRCC_BASE_ADDRESS + 0X00))
- #define **RCC_CFGR** ∗((uint_32t ∗)(DRCC_BASE_ADDRESS + 0X04))
- #define **RCC_CIR** ∗((uint_32t ∗)(DRCC_BASE_ADDRESS + 0X08))
- #define **RCC_APB2RSTR** ∗((uint_32t ∗)(DRCC_BASE_ADDRESS + 0X0C))
- #define **RCC_APB1RSTR** ∗((uint_32t ∗)(DRCC_BASE_ADDRESS + 0X10))
- #define **RCC_AHBENR** ∗((uint_32t ∗)(DRCC_BASE_ADDRESS + 0X14))
- #define **RCC_APB2ENR** ∗((uint_32t ∗)(DRCC_BASE_ADDRESS + 0X18))
- #define **RCC_APB1ENR** ∗((uint_32t ∗)(DRCC_BASE_ADDRESS + 0X1C))
- #define **RCC_BDCR** ∗((uint_32t ∗)(DRCC_BASE_ADDRESS + 0X20))
- #define **RCC_CSR** ∗((uint_32t ∗)(DRCC_BASE_ADDRESS + 0X24))
- #define PLLRDY_MASK 0x02000000

  PLL Ready Mask

- #define HSERDY_MASK 0x00020000

  HSE Ready Mask

- #define HSIRDY_MASK 0x00000002

  HSI Ready Mask

- #define HSI_SRC_MASK 0x00000000

  HSI Source Mask

- #define HSE_SRC_MASK 0x00000004

HSE Source Mask

- #define PLL_SRC_MASK 0x00000008

  HSE_PLLSRC_MASK Mask

- #define HSE_PLLSRC_MASK 0x00010000

  HSE_PLL Source Mask

- #define HSE_PLLSRC_DIV_TWO_MASK 0x00030000

  HSE_PLL Source Mask divided by Two

- #define HSI_PLLSRC_DIV_TWO_MASK 0x00000000

  HSI_PLL Source Mask divided by Two

- #define **PLLMUL_2** 0x00000000
- #define **PLLMUL_3** 0x00040000
- #define **PLLMUL_4** 0x00080000
- #define **PLLMUL_5** 0x000C0000
- #define **PLLMUL_6** 0x00100000
- #define **PLLMUL_7** 0x00140000
- #define **PLLMUL_8** 0x00180000
- #define **PLLMUL_9** 0x001C0000
- #define **PLLMUL_10** 0x00200000
- #define **PLLMUL_11** 0x00240000
- #define **PLLMUL_12** 0x00280000
- #define **PLLMUL_13** 0x002C0000
- #define **PLLMUL_14** 0x00300000
- #define **PLLMUL_15** 0x00340000
- #define **PLLMUL_16** 0x00380000
- #define AHB_PRESCALE_CLR 0xFFFFFF0F

  AHB Prescale Clear Mask

- #define APB1_PRESCALE_CLR 0xFFFFF8FF

  APB1 Prescale Clear Mask

- #define APB2_PRESCALE_CLR 0xFFFFC7FF

  APB2 Prescale Clear Mask

- #define PLL_CONFIG_CLR 0xFFC0FFFF

  PLL Clear Mask

- #define SYS_CLK_CLR 0xfffffffc

  System Clock Clear Mask

- #define SW_MASK 0x0000000C

  System Clock Switch Mask.
- #define PLL_SOURCE_MASK 0x00030000

  PLL Clock Source Switch Mask.
- #define PLL_MUL_MASK (uint_32t)0x003C0000

  PLL Multiplayer Mask.
- #define **APB2_MASK** 0x00003800
- #define **APB1_MASK** 0x00000700
- #define AHB_MASK 0x000000F0
- #define **APB2_PRESCALER_NOT_DIVIDED_MASK** 0x00000000

- #define **APB2_PRESCALER_DIV_2_MASK** 0x00002000
- #define **APB2_PRESCALER_DIV_4_MASK** 0x00002800
- #define **APB2_PRESCALER_DIV_8_MASK** 0x00003000
- #define **APB2_PRESCALER_DIV_16_MASK** 0x00003800
- #define **APB1_PRESCALER_NOT_DIVIDED_MASK** 0x00000000
- #define **APB1_PRESCALER_DIV_2_MASK** 0x00000400
- #define **APB1_PRESCALER_DIV_4_MASK** 0x00000500
- #define **APB1_PRESCALER_DIV_8_MASK** 0x00000600
- #define **APB1_PRESCALER_DIV_16_MASK** 0x00000700
- #define **AHB_PRESCALER_NOT_DIVIDED_MASK** 0x00000000
- #define **AHB_PRESCALER_DIV_2_MASK** 0x00000080
- #define **AHB_PRESCALER_DIV_4_MASK** 0x00000090
- #define **AHB_PRESCALER_DIV_8_MASK** 0x000000A0
- #define **AHB_PRESCALER_DIV_16_MASK** 0x000000B0
- #define **AHB_PRESCALER_DIV_64_MASK** 0x000000C0
- #define **AHB_PRESCALER_DIV_128_MASK** 0x000000D0
- #define **AHB_PRESCALER_DIV_256_MASK** 0x000000E0
- #define **AHB_PRESCALER_DIV_512_MASK** 0x000000F0

Functions

- uint_8t DRCC_SetClkStatus (uint_32t clk, uint_8t status)

  Function to set the Clock State.
- uint_8t DRCC_SetSystemClk (uint_32t clk)

  Function to set the System Clock.
- uint_8t DRCC_SetPLLConfig (uint_32t src, uint_8t MULL)

  Function to Configure Clock Source of PLL and it's Multiplication Factor.
- uint_8t DRCC_SetPriephralStatus (uint_32t priephral, uint_8t Status)

  Function to Enable/Disable Clock to peripheral.
- uint_8t DRCC_SetBusPrescale (uint_32t Bus, uint_8t Prescale)

  Function to set Bus Prescaler.
- uint_8t DRCC_GetBusClock (uint_32t Bus, uint_32t *CLK)

  Function to get bus Clock.

2.1.1 Detailed Description

This file is the Implementation for RCC Driver for STM32F103.

Author

Mostafa (mnader96@gmail.com)

Version

0.1

Date

2020-06-05

Copyright

2.1.2 Macro Definition Documentation

2.1.2.1 AHB_MASK

```
#define AHB_MASK 0x000000F0
```

2.1.2.2 AHB_PRESCALE_CLR

```
#define AHB_PRESCALE_CLR 0xFFFFFF0F
```

AHB Prescale Clear Mask

2.1.2.3 APB1_PRESCALE_CLR

```
#define APB1_PRESCALE_CLR 0xFFFFF8FF
```

APB1 Prescale Clear Mask

2.1.2.4 APB2_PRESCALE_CLR

```
#define APB2_PRESCALE_CLR 0xFFFFC7FF
```

APB2 Prescale Clear Mask

2.1.2.5 DRCC_BASE_ADDRESS

```
#define DRCC_BASE_ADDRESS 0X40021000
```

Base Address of RCC Peripheral

2.1.2.6 HSE_PLLSRC_DIV_TWO_MASK

```
#define HSE_PLLSRC_DIV_TWO_MASK 0x00030000
```

HSE_PLL Source Mask divided by Two

2.1.2.7 HSE_PLLSRC_MASK

```
#define HSE_PLLSRC_MASK 0x00010000
```

HSE_PLL Source Mask

2.1.2.8 HSE_SRC_MASK

```
#define HSE_SRC_MASK 0x00000004
```

HSE Source Mask

2.1.2.9 HSERDY_MASK

```
#define HSERDY_MASK 0x00020000
```

HSE Ready Mask

2.1.2.10 HSI_PLLSRC_DIV_TWO_MASK

```
#define HSI_PLLSRC_DIV_TWO_MASK 0x00000000
```

HSI_PLL Source Mask divided by Two

2.1.2.11 HSI_SRC_MASK

```
#define HSI_SRC_MASK 0x00000000
```

HSI Source Mask

2.1.2.12 HSIRDY_MASK

```
#define HSIRDY_MASK 0x00000002
```

HSI Ready Mask

2.1.2.13 PLL_CONFIG_CLR

```
#define PLL_CONFIG_CLR 0xFFC0FFFF
```

PLL Clear Mask

2.1.2.14 PLL_MUL_MASK

```
#define PLL_MUL_MASK (uint_32t)0x003C0000
```

PLL Multiplayer Mask.

2.1.2.15 PLL_SOURCE_MASK

```
#define PLL_SOURCE_MASK 0x00030000
```

PLL Clock Source Switch Mask.

2.1.2.16 PLL_SRC_MASK

```
#define PLL_SRC_MASK 0x00000008
```

HSE_PLLSRC_MASK Mask

2.1.2.17 PLLRDY_MASK

```
#define PLLRDY_MASK 0x02000000
```

PLL Ready Mask

2.1.2.18 SYS_CLK_CLR

```
#define SYS_CLK_CLR 0xfffffffc
```

System Clock Clear Mask

2.1.3 Function Documentation

2.1.3.1 DRCC_GetBusClock()

```
uint_8t DRCC_GetBusClock (
            uint_32t Bus,
            uint_32t * CLK )
```

Function to get bus Clock.

Parameters

Bus	Variable of uint_32t describe Bus Number (AHB_PRESCALER, APB1_PRESCALER, APB2_PRESCALER)
CLK	pointer to uint_32t Clock which to be read

Returns

uint_8t : OK | NOK

2.1.3.2 DRCC_SetBusPrescale()

```
uint_8t DRCC_SetBusPrescale (
            uint_32t Bus,
            uint_8t Prescale )
```

Function to set Bus Prescaler.

Parameters

Bus	Variable of uint_32t describe Bus Number (AHB_PRESCALER, APB1_PRESCALER, APB2_PRESCALER)
Prescale	Variable of uint_8t describe Bus Prescaler ex (APB2_PRESCALER_NOT_DIVIDED,APB1_PRESCALER_DIV_8,AHB_PRESCALER_DIV_256)

Returns

uint_8t : OK | NOK

2.1.3.3 DRCC_SetClkStatus()

```
uint_8t DRCC_SetClkStatus (
            uint_32t clk,
            uint_8t status )
```

Function to set the Clock State.

Parameters

clk	Variable of uint_32t describe Clock Type
status	Variable of uint_8t describe Clock Status (ON,OFF)

Returns

uint_8t : OK | NOK

2.1.3.4 DRCC_SetPLLConfig()

```
uint_8t DRCC_SetPLLConfig (
            uint_32t src,
            uint_8t MULL )
```

Function to Configure Clock Source of PLL and it's Multiplication Factor.

Parameters

src	Variable of uint_32t describe Clock Source to PLL (HSE_SRC,HSE_SRC_DIV_TWO,HSI_SRC_DIV_TWO)
MULL	Variable of uint_8t describe Miltiplication Factor (PLL_input_clock_x_2 up to PLL_input_clock_x_16)

Returns

uint_8t : OK | NOK

2.1.3.5 DRCC_SetPriephralStatus()

```
uint_8t DRCC_SetPriephralStatus (
            uint_32t priephral,
            uint_8t Status )
```

Function to Enable/Disable Clock to peripheral.

Parameters

priephral	Variable of uint_32t describe Peripheral ex (GPIO_A_ENABLE,DMA_1_ENABLE)
Status	Variable of uint_8t describe Clock Status of Peripheral (ON,OFF)

Returns

uint_8t : OK | NOK

2.1.3.6 DRCC_SetSystemClk()

```
uint_8t DRCC_SetSystemClk (
            uint_32t clk )
```

Function to set the System Clock.

Parameters

clk	Variable of uint_32t describe Clock Type to be System Clock(HSI_SYS,HSE_SYS,PLL_SYS)

Returns

uint_8t : OK | NOK

2.2 DRCC/DRCC.h File Reference

This file is a user interface for RCC Driver for STM32F103.

Macros

- #define HSI_ENABLE 0x10000001

  Used to Enable HSI.
- #define HSE_ENABLE 0x10010000

  Used to Enable HSE.
- #define PLL_ENABLE 0x11000000

  Used to Enable PLL.
- #define HSI_SYS 0x20000000

  used to make HSI Clock the System Clock
- #define HSE_SYS 0x20000001

  used to make HSE Clock the System Clock
- #define PLL_SYS 0x20000002

  used to make PLL Clock the System Clock
- #define HSE_SRC 0x40010000

  HSE Clock without Division.
- #define HSE_SRC_DIV_TWO 0x40030000

  HSE Clock divide by Two.
- #define HSI_SRC_DIV_TWO 0x40000000

  HSI Clock divide by Two.
- #define **PLL_input_clock_x_2** 0
- #define **PLL_input_clock_x_3** 1
- #define **PLL_input_clock_x_4** 2
- #define **PLL_input_clock_x_5** 3
- #define **PLL_input_clock_x_6** 4
- #define **PLL_input_clock_x_7** 5
- #define **PLL_input_clock_x_8** 6
- #define **PLL_input_clock_x_9** 7
- #define **PLL_input_clock_x_10** 8
- #define **PLL_input_clock_x_11** 9
- #define **PLL_input_clock_x_12** 10
- #define **PLL_input_clock_x_13** 11
- #define **PLL_input_clock_x_14** 12
- #define **PLL_input_clock_x_15** 13
- #define **PLL_input_clock_x_16** 14
- #define **GPIO_A_ENABLE** 0x20000004
- #define **GPIO_B_ENABLE** 0x20000008
- #define **GPIO_C_ENABLE** 0x20000010
- #define **GPIO_D_ENABLE** 0x20000020
- #define **GPIO_E_ENABLE** 0x20000040
- #define **GPIO_F_ENABLE** 0x20000080
- #define **GPIO_G_ENABLE** 0x20000100
- #define **USART_1_ENABLE** 0x20004000
- #define **DMA_1_ENABLE** 0x80000001
- #define AHB_PRESCALER 0x08000000

  used to select AHB Bus
- #define APB1_PRESCALER 0x08000001

used to select APB1 Bus

- #define APB2_PRESCALER 0x08000002

  used to select APB2 Bus
- #define **APB2_PRESCALER_NOT_DIVIDED** 0
- #define **APB2_PRESCALER_DIV_2** 4
- #define **APB2_PRESCALER_DIV_4** 5
- #define **APB2_PRESCALER_DIV_8** 6
- #define **APB2_PRESCALER_DIV_16** 7
- #define **APB1_PRESCALER_NOT_DIVIDED** 0
- #define **APB1_PRESCALER_DIV_2** 4
- #define **APB1_PRESCALER_DIV_4** 5
- #define **APB1_PRESCALER_DIV_8** 6
- #define **APB1_PRESCALER_DIV_16** 7
- #define **AHB_PRESCALER_NOT_DIVIDED** 0
- #define **AHB_PRESCALER_DIV_2** 8
- #define **AHB_PRESCALER_DIV_4** 9
- #define **AHB_PRESCALER_DIV_8** 10
- #define **AHB_PRESCALER_DIV_16** 11
- #define **AHB_PRESCALER_DIV_64** 12
- #define **AHB_PRESCALER_DIV_128** 13
- #define **AHB_PRESCALER_DIV_256** 14
- #define **AHB_PRESCALER_DIV_512** 15
- #define HSI_FREQ 8000000

  describe HSI Frequency

- #define HSE_FREQ 8000000

  describe HSE Frequency

- #define AHB_BUS 77

  used to check AHB Bus
- #define APB1_BUS 78

  used to check APB1 Bus
- #define APB2_BUS 79

  used to check APB2 Bus

Functions

- uint_8t DRCC_SetClkStatus (uint_32t clk, uint_8t status)

  Function to set the Clock State.
- uint_8t DRCC_SetSystemClk (uint_32t clk)

  Function to set the System Clock.
- uint_8t DRCC_SetPLLConfig (uint_32t src, uint_8t MULL)

  Function to Configure Clock Source of PLL and it's Multiplication Factor.
- uint_8t DRCC_SetPriephralStatus (uint_32t priephral, uint_8t Status)

  Function to Enable/Disable Clock to peripheral.
- uint_8t DRCC_SetBusPrescale (uint_32t Bus, uint_8t Prescale)

  Function to set Bus Prescaler.
- uint_8t DRCC_GetBusClock (uint_32t Bus, uint_32t *CLK)

  Function to get bus Clock.

2.2.1 Detailed Description

This file is a user interface for RCC Driver for STM32F103.

Author

Mostafa (mnader96@gmail.com)

Version

0.1

Date

2020-06-05

Copyright

2.2.2 Macro Definition Documentation

2.2.2.1 HSE_SRC_DIV_TWO

```
#define HSE_SRC_DIV_TWO 0x40030000
```

HSE Clock divide by Two.

2.2.2.2 HSI_SRC_DIV_TWO

```
#define HSI_SRC_DIV_TWO 0x40000000
```

HSI Clock divide by Two.

2.2.3 Function Documentation

2.2.3.1 DRCC_GetBusClock()

```
uint_8t DRCC_GetBusClock (
            uint_32t Bus,
            uint_32t * CLK )
```

Function to get bus Clock.

Parameters

Bus	Variable of uint_32t describe Bus Number (AHB_PRESCALER, APB1_PRESCALER, APB2_PRESCALER)
CLK	pointer to uint_32t Clock which to be read

Returns

uint_8t : OK | NOK

2.2.3.2 DRCC_SetBusPrescale()

```
uint_8t DRCC_SetBusPrescale (
            uint_32t Bus,
            uint_8t Prescale )
```

Function to set Bus Prescaler.

Parameters

Bus	Variable of uint_32t describe Bus Number (AHB_PRESCALER, APB1_PRESCALER, APB2_PRESCALER)
Prescale	Variable of uint_8t describe Bus Prescaler ex (APB2_PRESCALER_NOT_DIVIDED,APB1_PRESCALER_DIV_8,AHB_PRESCALER_DIV_256)

Returns

uint_8t : OK | NOK

2.2.3.3 DRCC_SetClkStatus()

```
uint_8t DRCC_SetClkStatus (
            uint_32t clk,
            uint_8t status )
```

Function to set the Clock State.

Parameters

clk	Variable of uint_32t describe Clock Type
status	Variable of uint_8t describe Clock Status (ON,OFF)

Returns

uint_8t : OK | NOK

2.2.3.4 DRCC_SetPLLConfig()

```
uint_8t DRCC_SetPLLConfig (
            uint_32t src,
            uint_8t MULL )
```

Function to Configure Clock Source of PLL and it's Multiplication Factor.

Parameters

src	Variable of uint_32t describe Clock Source to PLL (HSE_SRC,HSE_SRC_DIV_TWO,HSI_SRC_DIV_TWO)
MULL	Variable of uint_8t describe Miltiplication Factor (PLL_input_clock_x_2 up to PLL_input_clock_x_16)

Returns

uint_8t : OK | NOK

2.2.3.5 DRCC_SetPriephralStatus()

```
uint_8t DRCC_SetPriephralStatus (
            uint_32t priephral,
            uint_8t Status )
```

Function to Enable/Disable Clock to peripheral.

Parameters

priephral	Variable of uint_32t describe Peripheral ex (GPIO_A_ENABLE,DMA_1_ENABLE)
Status	Variable of uint_8t describe Clock Status of Peripheral (ON,OFF)

Returns

uint_8t : OK | NOK

2.2.3.6 DRCC_SetSystemClk()

```
uint_8t DRCC_SetSystemClk (
            uint_32t clk )
```

Function to set the System Clock.

Parameters

clk	Variable of uint_32t describe Clock Type to be System Clock(HSI_SYS,HSE_SYS,PLL_SYS)

Returns

uint_8t : OK | NOK

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