Full-Custom Design 8-bit CAM using 9T SRAM Department of electrical and Computer Engineering, Birzeit University

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***Abstract*—The objective of this combined project is to design and develop an 8-bit Content Addressable Memory (CAM) utilizing a 9T SRAM configuration. The project, focused on a 14nm CMOS technology, emphasizes on maximizing power efficiency and minimizing the area requirement for the CAM cell, particularly during write operations. The design balances low power consumption with reduced delay, enhancing the CAM's overall performance. Key features include the use of 9T SRAM, efficient CAM cell design, low power considerations, XOR operations, and effective read and write functionalities. Additionally, the proposed design integrates a parallel searching mechanism, essential in various applications, and employs a comparator circuit with a memory module for storing complement bits. This facilitates the efficient retrieval of information by comparing incoming data with stored bits. Furthermore, the design has been optimized for minimal area occupation and power usage, thereby improving efficiency. The transistor size ratio of PMOS to NMOS used in this design is 2:1, a proportion determined experimentally to match the fall time of the inverter with its rise time.**

***Index Terms*— CAM, SRAM, 9T SRAM.**

I. INTRODUCTION

The integration of 9-transistor Static Random-Access Memory (SRAM) in Content Addressable Memory (CAM) marks a significant development in computer memory technology, especially in chip design. This advancement, moving from the traditional 6-transistor SRAM, notably reduces power consumption. RAM, a crucial component within a computer's main memory, offers direct access to the Central Processing Unit (CPU) and is pivotal for data read and write operations at specific memory addresses. It acts as temporary storage for actively running programs, enhancing CPU processing efficiency. However, as a volatile memory type, RAM loses its stored data when power is turned off. Data retrieval from RAM involves using the memory address to access the desired content word through multiple cycles. The 9-transistor SRAM in CAM thus represents a blend of efficient memory utilization and power-saving in modern computer memory systems.

SRAM (Static Random-Access Memory): SRAM, or Static Random-Access Memory, is a form of computer memory that stores data in such a way that it may be accessed and retrieved quickly. Unlike Dynamic RAM (DRAM), which must be updated regularly to retain the data it holds, SRAM may store data as long as the device is powered on. SRAM is made up of memory cells, each of which is composed of many transistors coupled in a circuit. These transistors are organized in such a manner that each cell can store a single bit of data (either a 0 or a 1). The primary benefit of SRAM is its speed. SRAM cells may be accessed considerably faster than DRAM cells since they do not require a refresh cycle. As a result, SRAM is perfect for use in cache memory, which is used to temporarily store frequently accessed data that the CPU needs to retrieve rapidly. [1]

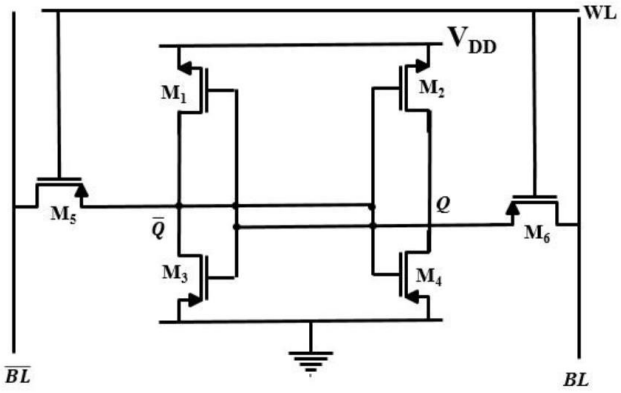

Figure 1. 1-bit SRAM cell

9T SRAM (9 Transistors Static Random-Access Memory): This memory employs a customized memory cell architecture with 9 transistors per cell. This circuit's design allows the 9T SRAM to run at a lower supply voltage, resulting in decreased power consumption and greater stability in noisy conditions. When comparing 9T SRAM to 6T SRAM, the trade-off with 9T SRAM is that it has a bigger cell size than 6T SRAM, which can result in a larger chip area and greater cost. However, in certain applications where power consumption and stability are crucial, it may be a feasible solution. [2]

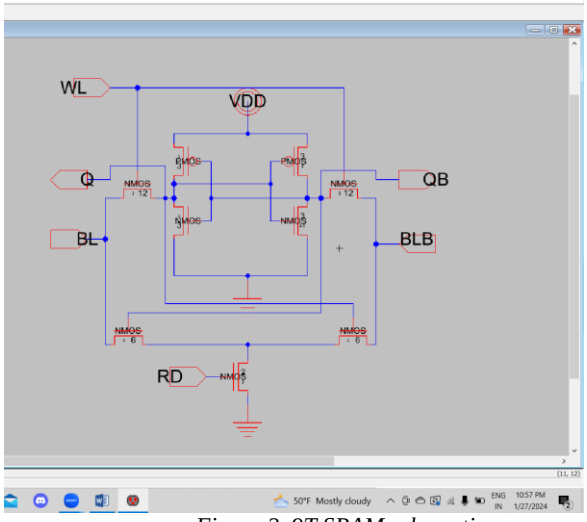

Figure 2. 9T SRAM schematic

The incorporation of an additional transistor in the 9T SRAM cell significantly enhances the cell's robustness, reducing the likelihood of read and write failures attributable to disturbances such as noise or process variations. This extra transistor also contributes to more efficient read operations by minimizing voltage drops across the access transistors. Consequently, faster access times are achieved, and the impact of process variations is mitigated.

Moreover, the 9T SRAM cell exhibits notable improvements in write performance. The presence of an extra write-assist transistor plays a crucial role in boosting the write current, thereby enhancing the cell's reliability during write operations. This addresses potential stability issues that may arise when writing data to the memory cell.

It is important to acknowledge a tradeoff associated with the 9T SRAM cell, namely an increase in power consumption compared to the 6T SRAM cell. The additional access transistor necessitates extra power for driving read and write operations. However, the advantages it offers over the 6T SRAM cell outweigh this tradeoff, and advancements in circuit design techniques have played a significant role in minimizing the associated power loss.

CAM (Content Addressable Memory): is a sort of computer memory that allows data to be accessed rather than its memory address. 9T SRAM-based CAM is a form of CAM that uses a 9-transistor SRAM cell rather than the more common 6-transistor SRAM cell.

The extra transistors in each cell in 9T SRAM-based CAM are utilized to construct a "match-line" circuit that can compare the stored data with a search key. This allows the CAM to search for data fast depending on its content, which is beneficial in a range of applications including network routers, database systems, and pattern recognition.

Fast search speed and low power consumption are two advantages of 9T SRAM-based CAM. However, the greater complexity of the 9T SRAM cell over the typical 6T SRAM cell might result in a larger chip area and higher cost. Furthermore, CAM based on 9T SRAM may be more vulnerable to noise and other kinds of interference. [3]

8-Bit CAM: The 8-bit CAM in the system suggested in this paper is composed of 16 1-bit CAM and two decoders. Taking eight 1-bit inputs and creating an output. Some lines that regulate the read-write operation, BL and BLB, specify the operation applied to the input data.

II. THE SYSTEM

A. 9T SRAM

This project is specifically tailored for a 14nm CMOS technology, with a primary focus on maximizing power efficiency and minimizing the area requirement for the CAM cell, particularly during write operations. Adopting a ratio of 2:1 (PMOS to NMOS) yielded nearly equal rise and fall times, demonstrating optimal performance for the inverter with this specific size ratio.

Figure 3 below illustrates the schematic for the 9T SRAM. In this representation, the PMOS transistors are scaled with a size factor of 2 in the scalable unit, while the NMOS transistors are sized at 1. The SRAM diagram features four primary inputs: WL, Q, BL, and RD, each serving a specific function. WL is designated for reading data, Q represents the data, BL signifies the inverse of the data, and RD facilitates the writing of data into the SRAM. Additionally, the SRAM produces two outputs, QB, which stores the data, and BLB, its complement.

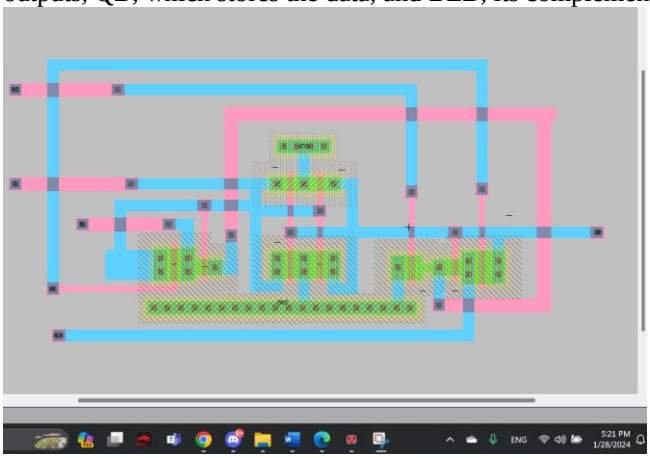
Figure 3. 9T SRAM layout

B. 1 BIT CAM Cell.

The 9T SRAM transformed into an Icon View representation, serving as the basis for implementing the CAM cell. In conjunction with the XOR gate, CAM DATA was incorporated as an input, while the output, labeled "match," is depicted in the figure below. Figure 4 illustrates the schematic of the 1-bit CAM cell. Activation of the "match" state to the ON state occurs when the data written in the SRAM aligns with the CAM data, and Figure 5 illustrates the layout of the 1-bit CAM schematic.

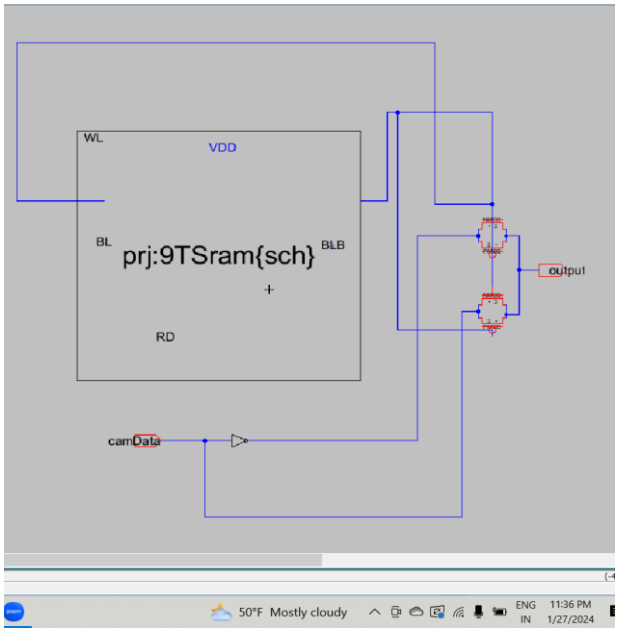

Figure 4. 1-bit CAM schematic

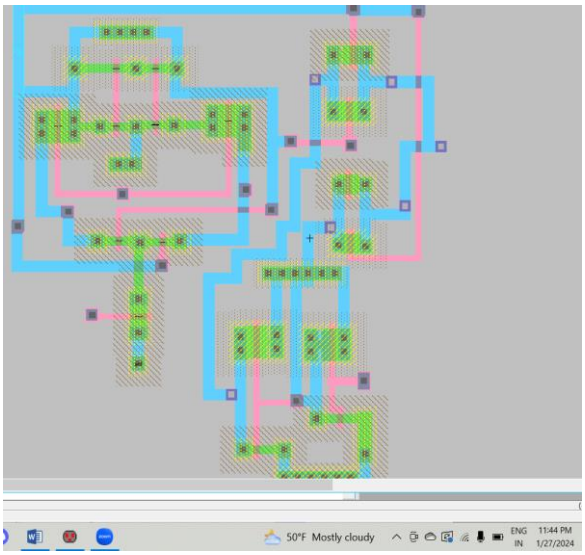

Figure 5. 1-bit CAM layout

C. 8 BIT CAM Cell

The 8-bit CAM cell is comprised of 16 individual 1-bit CAM cells, each capable of storing a single bit of data. These individual cells are organized to collectively handle 8 bits of data. Two decoders are integrated into the structure of the 8-bit CAM cell, these decoders play a crucial role in selecting and directing the flow of data within the CAM cell, facilitating the read and write operations. It has input lines, including BL (Bit Line), BLB (Complement of Bit Line), and WL (Word Line), these lines are essential for regulating the read and write operations and specifying the operation applied to the input data. During a read operation, the RL (Read Line) is activated to retrieve data from the CAM cell. The stored information is then accessed, allowing for parallel searching and fast data retrieval.

Before proceeding with the full implementation of the 8-bit CAM design, essential components were individually designed and implemented. These components include an 8-bit input NAND gate, a 3-8 Decoder, and finally Encoder. These components serve as integral building blocks, contributing significantly to the overall design process. Visual representations of these elements can be observed in the attached figures.[4]

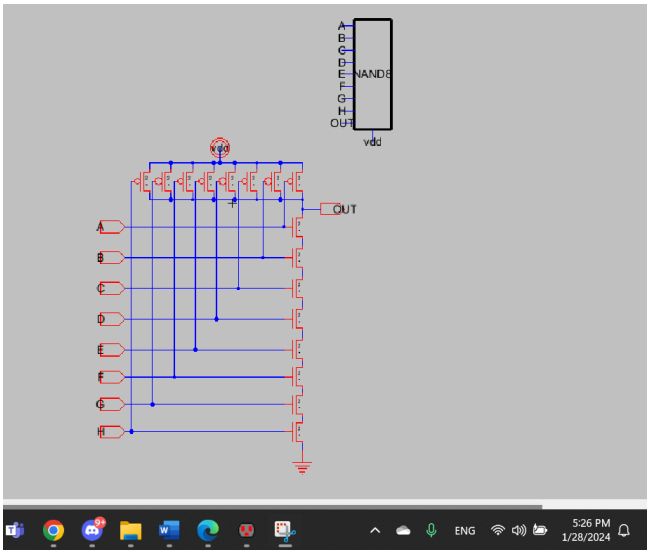

Figure 6- 8-bit NAND gate schematic

Layout for 8bit nand:

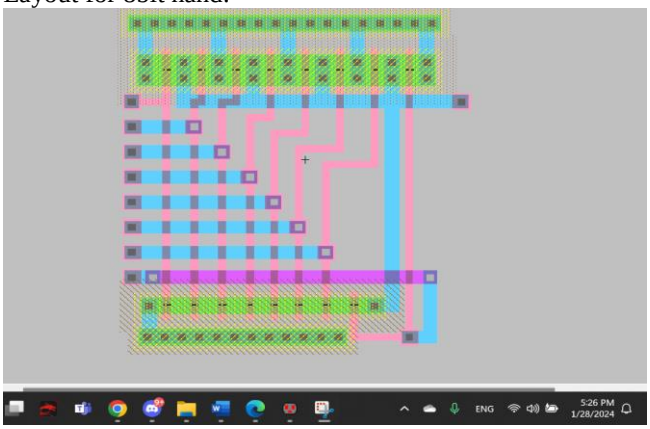

Figure 7- 8-bit NAND gate layout

3*8 decoder schematics:

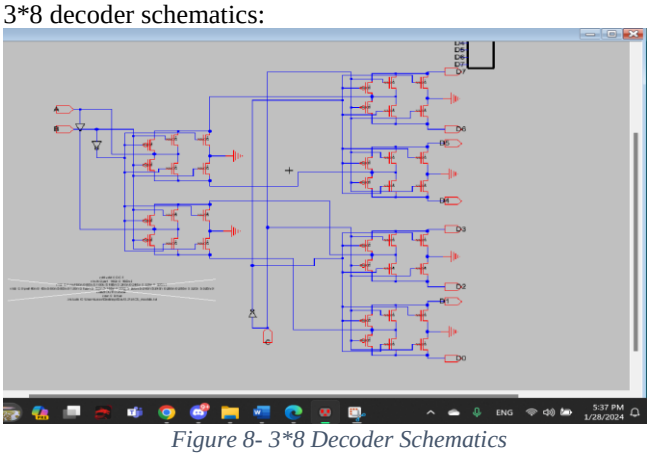

*Figure 8- 3*8 Decoder Schematics*

3*8 decoder layout:

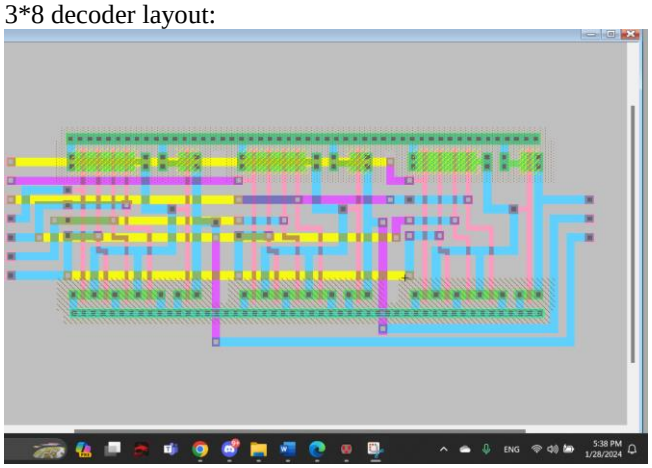

*Figure 9-3*8 Decoder Layout*

3*8 decoder simulation:

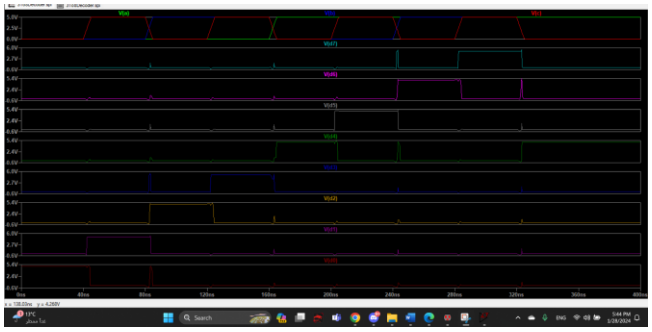

*Figure 10-3*8 Decoder Simulation*

Then, the components were combined together to assemble the 8 bit CAM, figures below illustrate the 8 bit CAM schematics, layout and simulation:

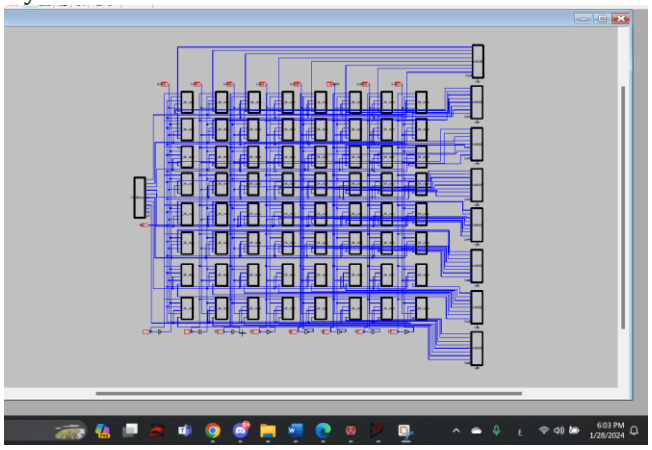

Figure 11- 8Bit CAM Schematics

Layout for 8bit CAM:

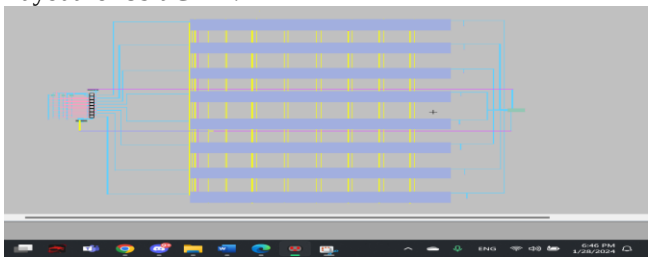

Figure 12- 8Bit CAM Layout

Simulation for 8bit CAM:

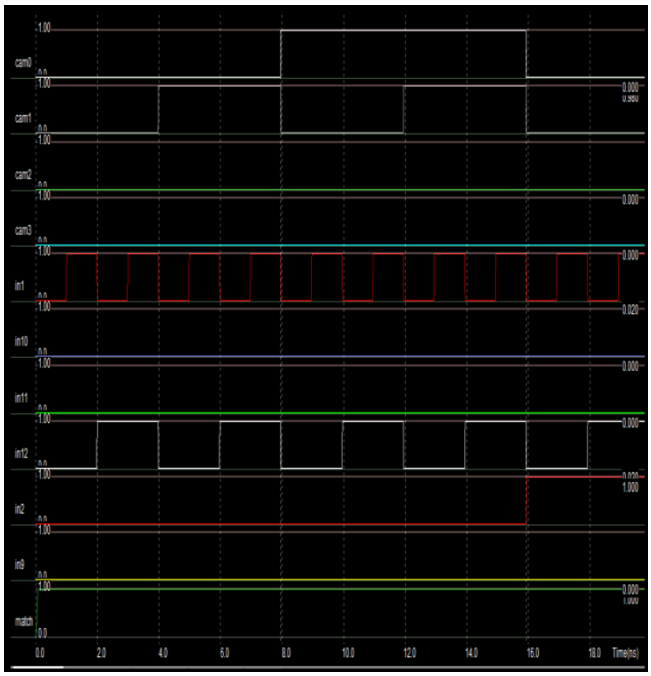

Figure 13. 8Bit CAM simulation

III. CONCLUSION

In conclusion, this study presents the process of developing an 8-Bit CAM using a 16-9T SRAM-based CAM. Initially, circuit designs were successfully established. The subsequent simulation results closely aligned with the theoretical expectations. Additionally, the layout for each circuit was finalized, confirming the consistency between the simulation outcomes and the initial schematics.

However, further research and the advent of new methodologies revealed that the initially chosen 9T SRAM design was not the most efficient in terms of power leakage, leading to an approximate 40% reduction in power consumption. Moreover, this approach resulted in a notable decrease in delay during read-write operations, as evidenced by the data in the table.

Ultimately, the research was brought to a fruitful conclusion with the effective use of tools like "Electric" and "LTSpice", marking a significant step forward in this field.

IV. REFERENCES

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