Q. The definitions;

of Micro-Processor on Integrated Circuiting which

of Performent The afth metic and logic ofer orthans

12-micro-controller or Ic whith has micro-Processor

nond another pereprence like RAM & ROM, IzC, ---
3-Embedded Systems: Computer System.

15 Combination of micro Processor-compination 15 F memory and peripheral devices to 15 do Specific Function.

W-mechationic Systems: System in which in michanecal hardware age integrated with

105- N-bit Processor

-Processor Con work only on n bit of data at time of the data torget than n bit it will broken into nebit Pieces.

SUN MON TUE WED THU FRI SAT

1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13. 14. 15. 16. 17. 18. 19. 20. 21. 22. 23. 24. 25. 26. 27. 28. 29. 30. 31

| Comparation Comparation Comparation Comparation Comparation Comparation ALU CRU but Flash both at a ALU Registers MCU To Parts Unit MCU Registers Mcu |
|--|
| OB 2J CPU & MCU OB ALU TO CRU but Flash both 9 Te ALU To Pasts but Registers To Pasts but Registers |
| Ilo Posts but [Registers] |
| I/o Pasts but [Registers] |
| |
| MCII |
| CPU -> Alux CU + Registers Ebrain of computation |
| 15MCU - V CPU+ Flosh+RAM+ |
| 3] Von neuman & har vard |
| 18 FRAM |
| CPU RAM CPU 30 |
| Used one memory For instructure |
| instructures and dotat For used Two memory and |
| - Jus bus [inst; data] |
| - o Slover - o faster |
| SUN MON TUE WED THU FRI SAT 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13. 14. 15. 16. 17 18. 19. 20. 21. 22. 23. 24. 25. 26. 27. 28. 29. 30. 31 |

Date L Subject auj Rom [Read only memory] PROM & Programable Rom * & but The info or oglamed by the User by burner devices Programed only one tim [OTP] we con't write on it [Read only memory] mosk Rom - Read only memory programed only one time COTPJ - Programed during the monufacturing. EPROM - Elease Programable Rome - CON COR CATSE OR and Programed Thousand Times we can colle the information by Ultravoilet rays. - Non Volatile like PRom, Mask Rom 125 RAN LRandom access memory 7 SRAM - + Stotic RAM - doesn't need refreshing - Use 6 Transistor to Stare one with bit. - more expensive. Faster Than DRAM - Cash memoly one of its USES. -o com plex - Use high midum Pouel consumption DRAH -> Dynamic Rank need refreshing the onen Tr 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13. 14. 15. 16. 17. 18. 19. 20. 21. 22. 23. 24. 25. 26. 27. 28. 29. 30. 31

| F-11-4 | Date | | | |
|---------|------|--|--|--|
| Subject | | | | |
| | | | | |

when one Transistor and one capictor to store with white point of refreshing time about bums. [16 time in second] and during The refreshing use can't access it about Than SRAM- simple - chear.

Used in moin memory

26] The Qu doesn't have the capecity
"To write on it.

so con writer by external device

18

The state of the s

1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13. 14. 15. 16. 17. 18. 19. 20. 21. 22. 23. 24. 25. 26. 27 28 29 30 31

| Туре | Volatile? | Writeable? | Erase
size | Max Erase
cycles | Cost(per
Byte) | Speed | |
|-------------|-----------|------------|----------------|---------------------|-------------------|--|-----------------|
| SRAM | Yes | Yes | Byte | Unlimited | Expensive | Fast than
DRAM | RAM |
| DRAM | Yes | Yes | Byte | Unlimited | moderated | Moderated | Fast than ROM |
| MASK
ROM | No | No | | | Cheap | Fast | |
| PROM | No | once | | | moderated | Fast | ROM |
| EPROM | No | Yes | Entire
chip | Limited | moderated | Fasst | Slower than RAM |
| EEPROM | Yes | Yes | Byte | Limited | Expensive | Fast to read
slow to
earse / write | |
| FLASH | Yes | Yes | Sector | Limited | moderated | Fast to read
slow to
earse / write | Hybrid |
| NVRAM | Yes | Yes | Byte | Unlimited | Expensive | Fast | |