

1. Implement the MIPS register file that reads simultaneously from two registers and write into one register.

Main module should be called "RegisterFile".

RegisterFile RTL should match the desired RTL (refer to lab05). Entity should look as follows:

```
read_sel1 : in std_logic_vector(4 downto 0)
read_sel2 : in std_logic_vector(4 downto 0)
write_sel : in std_logic_vector(4 downto 0)
write_ena : in std_logic
clk: in std_logic

write_data: in std_logic_vector(31 downto 0) data1:
out std_logic_vector(31 downto 0)
data2: out std_logic_vector(31 downto 0)
```

Test before submit ([attached test case](#)).

2. Implement 32 bit full ALU.

Main module should be called "ALU" ALU functional specifications:

ALUOp	Function
0000	AND
0001	OR
0010	ADD
0110	SUB

ALU RTL should match the desired RTL (refer to lab05). Entity should look as follows:

```
data1 : in std_logic_vector(31 downto 0) data2 :
in std_logic_vector(31 downto 0) aluop : in
std_logic_vector(3 downto 0) cin : in std_logic

dataout: out std_logic_vector(31 downto 0) cflag:
out std_logic

zflag: out std_logic oflag:
out std_logic
```

Test before submit ([attached test case](#)).

Delivery method:

A dropbox folder named "Group#" will be shared with each team. Inside the shared folder, create new folder called "Milestone1".

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Milestone1 folder should include two zip files that includes the main modules and its dependencies (package, mux, decoder, and so on ...)

1. RegisterFile.zip
2. ALU.zip

Deadline: saturday, 02 April, 2016 23:59.

Good luck!