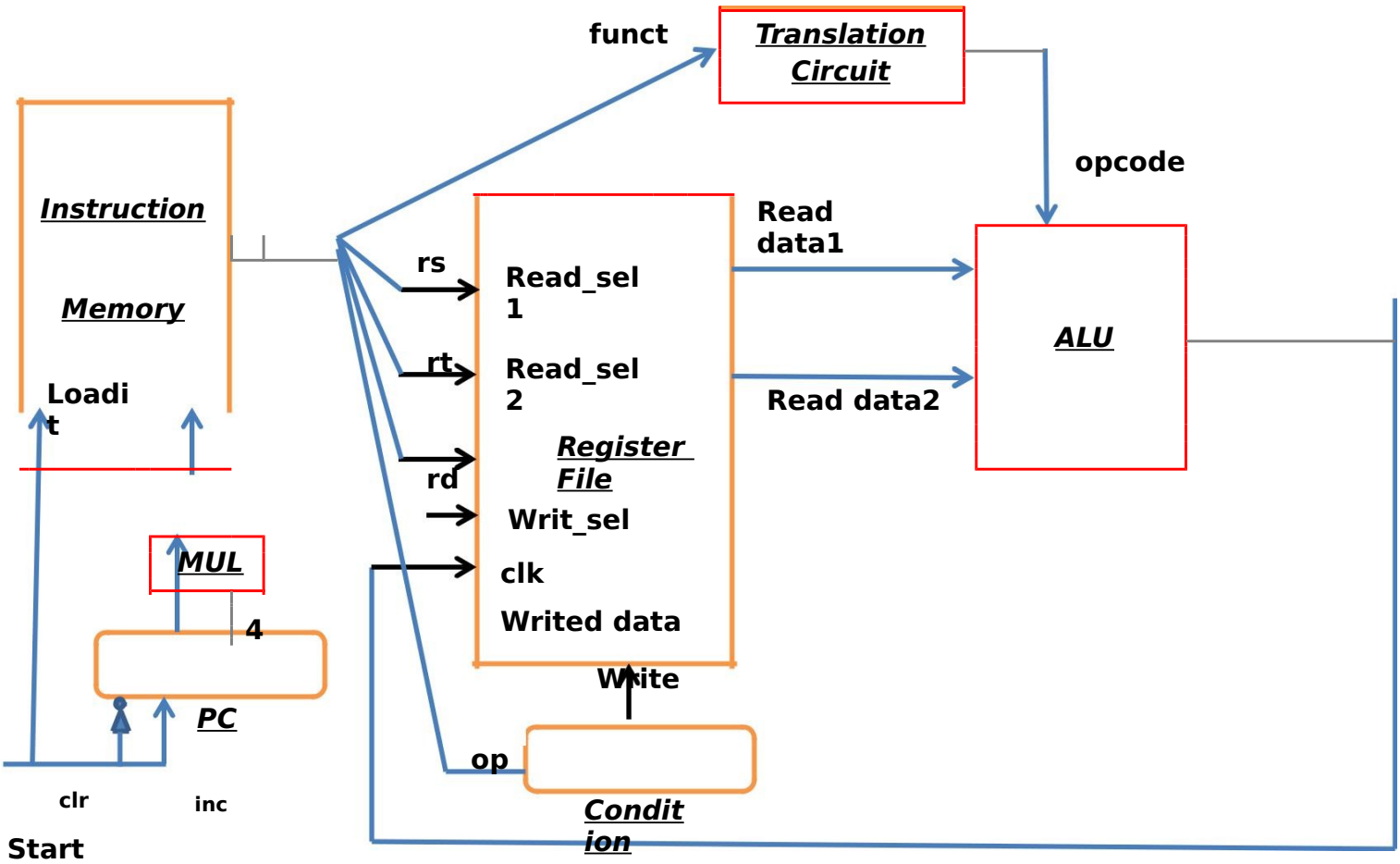
Computer Architectures 2016

Milestone 2:

In this milestone you have to design MIPS CPU Using VHDL. Your proposed CPU should be able to perform certain instructions. These instructions are R-type instructions and they only include AND, OR, ADD, SUB, SLT and finally NOR instructions.

You should use “register file” and “32bit ALU” that you have already implemented in milestone1. The main goal of this milestone is to connect the implemented modules in pervious milestone. An instruction memory module will be given to you. This given module contains some R-type instructions you should connect it to your CPU in such a way that your CPU performs them sequentially. You may refer to lab7.

The following diagram may help to understand the required design



Your implemented module should be named as MainModule. Its entity should be as following:

START: IN STD_LOGIC;

CLK: IN STD_LOGIC;

RegFileOut1: OUT STD_LOGIC_VECTOR(31 downto 0);

RegFileOut2: OUT STD_LOGIC_VECTOR(31 downto 0);

ALUOut: OUT STD_LOGIC_VECTOR(31 downto 0);

Note:

Please check the attached test cases before submission

Delivery method:

Same method as in milestone1

- A dropbox folder named "Group#" will be shared with each team. ○ Inside the shared folder, create new folder called "Milestone2".
- Milestone2 folder should include one zip files that includes the main modules and its dependencies (package, InstMem, mux, decoder, and so on …)

Deadline:

Friday, 22th April 2016 23:59:59

Good Luck!