16 BIT High Speed Comparator

Abdallah AboShoaib[1] and Malik Arqoup[2]

[1]1210211
[2]1211686

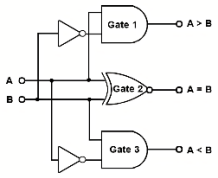
ABSTRACT

Showing the theory of comparators and why we need them. Then , how to implement 16 bit one using 4 bits And demonstrate the steps of Digital designing and then schematic and layout for the fabrication process. Finaly showing results and statistic .

1 | Theory And Workflow

Digital Desgin :

1- Bit Comparator :

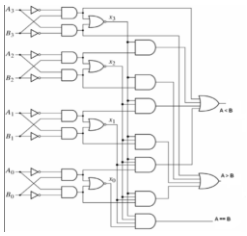


1 1-bit comparator block diagram

A > B : A.B' , A = B : A'.B' + A . B

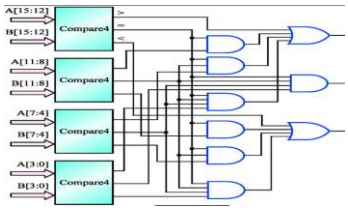
4- Bit Comparator :

We can use the one bit to make the 4 one .



2 4bit comparator using 1 bit

16 – bit Comparator :

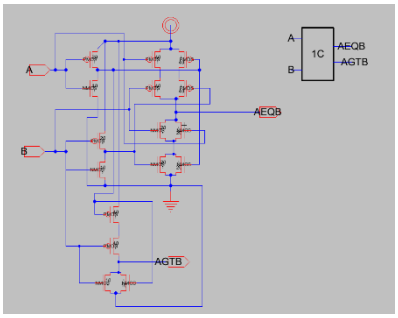


3 16 bit comparator using 4 bit

Schematic :

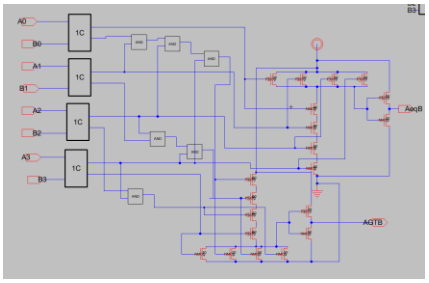
Using cmos technology and the roles of design aspects.

1-bit comparator :



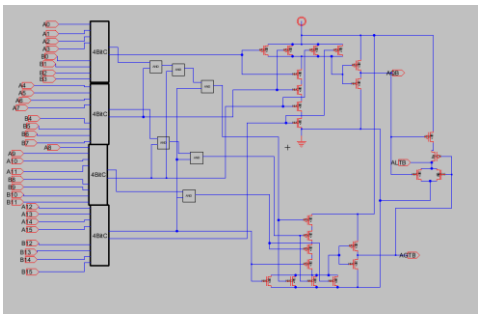
4 1bit Comparator cmos schematic

4 – bit Comparator :



5 4bit comparator coms schematic

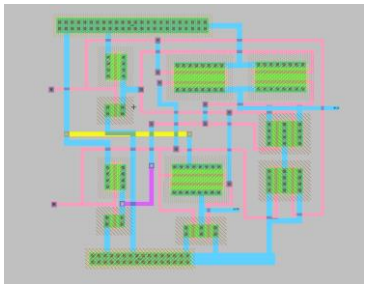
16-bit comparator :



6 16- bit comparator cmos schematic

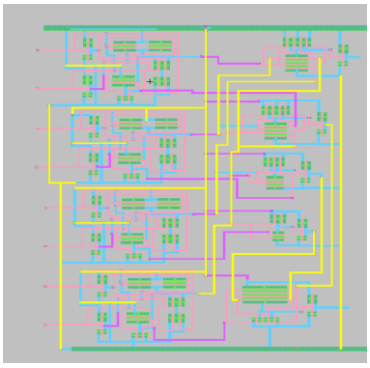
Layout :

1-bit :



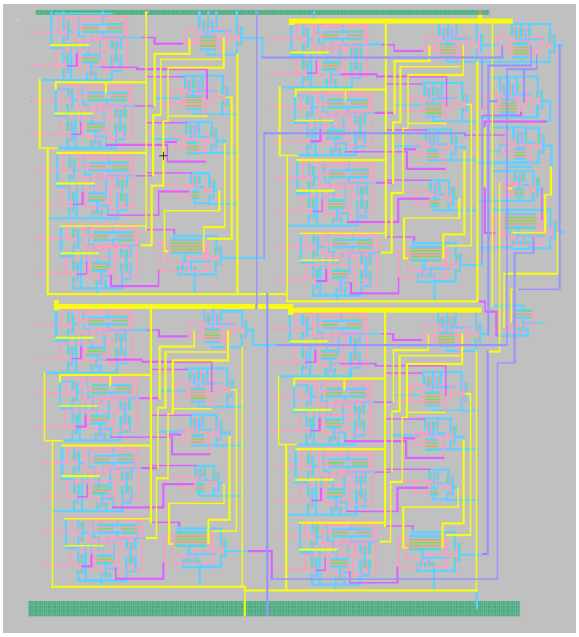
7 1 bit Layout

4-bit:



8 4-bit Layout

16- bit :



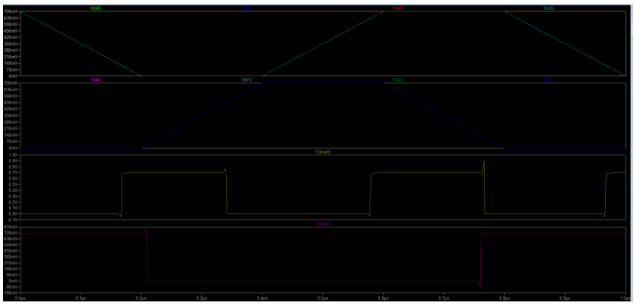
9 16- bit layout

Delay report :

```
vaeqb=7.08925e-009 FROM 1.74487e-007 TO 1.81576e-007
vaeqbt=7.06076e-009 FROM 3.80942e-007 TO 3.88003e-007
vagtb=5.46814e-009 FROM 3.78905e-007 TO 3.84373e-007
vagtbt=5.65048e-009 FROM 1.8459e-007 TO 1.90241e-007
```

4 bit :

schematic :



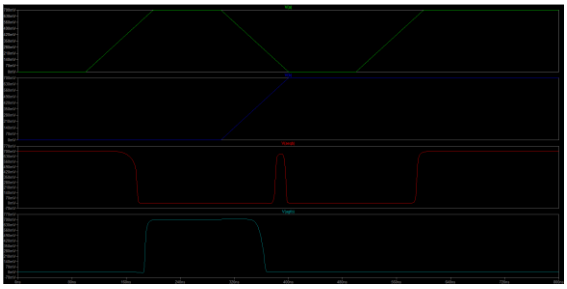
Delay and power report :

```
avg_power: AVG(i(vdd))=-2.30936e-007 FROM 0 TO 1e-006
peak_power: MAX(i(vdd))=-2.30935e-007 FROM 0 TO 1e-006
veqb=9.46711e-010 FROM 3.40423e-007 TO 3.4137e-007
veqbt=1.04156e-009 FROM 1.66971e-007 TO 1.68012e-007
vgtb=1.32564e-009 FROM 2.09545e-007 TO 2.10871e-007
vgb=6.97791e-010 FROM 7.60259e-007 TO 7.60956e-007
```

2 | Results and Statistic

1-bit comparator :

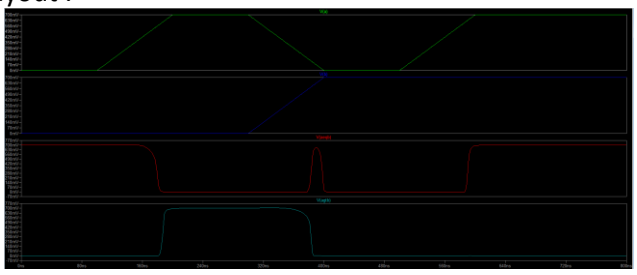
Schematic :



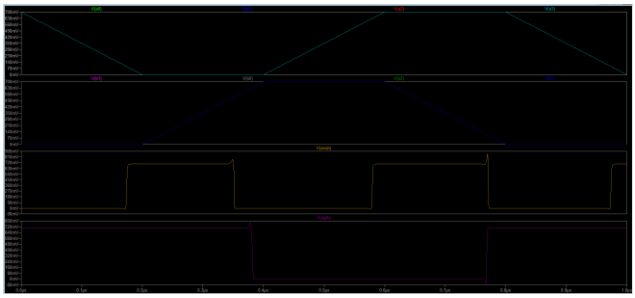
Delay report :

```
vaeqb=5.84739e-009 FROM 1.71227e-007 TO 1.77075e-007
vaeqbt=6.09705e-009 FROM 3.78882e-007 TO 3.84979e-007
vagtb=8.36888e-009 FROM 3.56919e-007 TO 3.65288e-007
vagtbt=5.46451e-009 FROM 1.87117e-007 TO 1.92582e-007
```

Layout :



Layout :

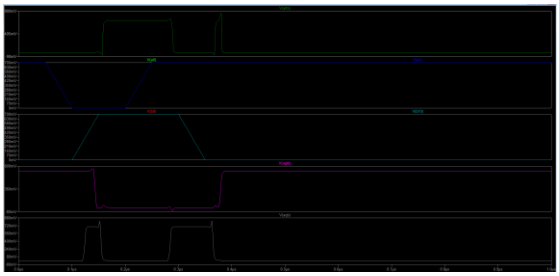


Delay report :

```
avg_power: AVG(i(vdd))=-7.92732e-006 FROM 0 TO 1e-006
peak_power: MAX(i(vdd))=8.44107e-006 FROM 0 TO 1e-006
veqb=1.07203e-009 FROM 3.50822e-007 TO 3.51894e-007
veqbt=1.53032e-009 FROM 1.73415e-007 TO 1.74946e-007
vgtb=1.81859e-009 FROM 3.80705e-007 TO 3.82524e-007
vgb=1.0047e-009 FROM 7.68181e-007 TO 7.69186e-007
```

16 – bit

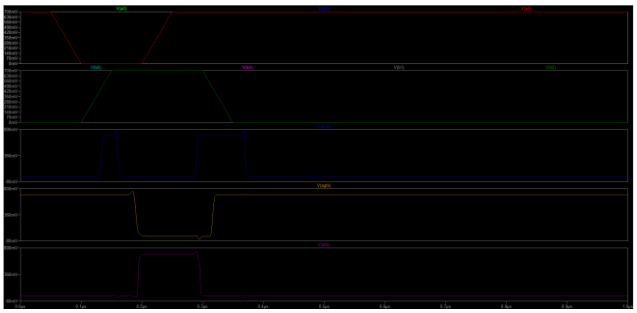
schematic :



Delay and power report :

```
avg_power: AVG(i(vdd))=-2.58342e-005 FROM 0 TO 1e-006
peak_power: MAX(i(vdd))=8.32356e-005 FROM 0 TO 1e-006
vaeqb=3.21783e-009 FROM 1.53314e-007 TO 1.56532e-007
vaeqbt=4.71587e-009 FROM 1.21639e-007 TO 1.26355e-007
vagb=3.99212e-009 FROM 1.41111e-007 TO 1.45103e-007
vagbt=5.27217e-009 FROM 3.76839e-007 TO 3.82111e-007
vltb=3.19297e-009 FROM 2.86701e-007 TO 2.89894e-007
vltbt=3.28306e-009 FROM 1.57499e-007 TO 1.60782e-007
```

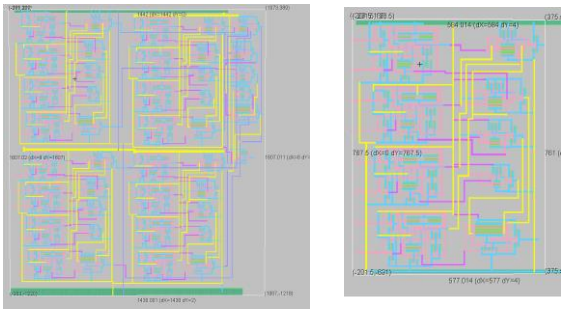
Layout :



Delay And power report :

```
avg_power: AVG(i(vdd))=-2.77042e-005 FROM 0 TO 1e-006
peak_power: MAX(i(vdd))=7.57739e-005 FROM 0 TO 1e-006
vaeqb=3.073e-009 FROM 1.59403e-007 TO 1.62476e-007
vaeqbt=4.04751e-009 FROM 1.30442e-007 TO 1.34489e-007
vagb=5.85466e-009 FROM 1.87503e-007 TO 1.93357e-007
vagbt=5.08886e-009 FROM 3.14594e-007 TO 3.19683e-007
vltb=3.941e-009 FROM 2.92957e-007 TO 2.96898e-007
vltbt=3.70259e-009 FROM 1.92886e-007 TO 1.96589e-007
```

3|Area calculations and Discussion



16 – bit : 2.3um²
4-bit : 0.4383435 um²
1-bit :0.04572 um²

The design and implementation of the 16-bit high-speed comparator presented in this paper demonstrate a successful application of a hierarchical design approach, which efficiently scales from a basic 1-bit comparator to a more complex 16-bit comparator. By building upon the simpler 1-bit comparator, the design process was streamlined, allowing for a systematic increase in complexity while maintaining consistency and reducing verification challenges. The use of CMOS technology, specifically leveraging the 16nm HP process parameters file, was pivotal in achieving a balance between speed, power consumption, and area, which are critical in high-speed digital circuit design. The detailed schematics and layouts provided for each stage of the design—1-bit, 4-bit, and 16-bit—highlight the careful consideration of design rules and manufacturability, ensuring that the circuit not only functions as intended but can also be efficiently fabricated. Performance evaluation, focusing on delay and power consumption, indicates that the design meets the desired speed requirements while keeping power usage within acceptable limits, making it suitable for integration into larger digital systems where high performance is essential. However, there are opportunities for future enhancements, such as further reducing power consumption, optimizing area utilization, and exploring newer technologies or circuit techniques to push the performance boundaries even further. The results validate the effectiveness of the hierarchical approach, the use of CMOS technology, and the 16nm HP process, underscoring the potential of this design in various high-speed applications. Overall, this work provides a robust and efficient solution to the challenge of high-speed digital comparison, contributing significantly to the field and offering a foundation for future research and development in comparator design.