Cairo University - Faculty of Engineering

Computer Engineering Department

VLSI

**Project Phase 1**

**Team 3**

**IO Sub-team**

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| Name | Sec. | B.N |
| Saad Eldeen Mohamed | 1 | 26 |
| Abdallah Hussien | 2 | 2 |
| Ali Adel | 2 | 4 |
| Mohamed Adel | 2 | 21 |

**Submitted To:**

**Eng.** Abdelrahman Abo Taleb

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**Control Signals:**

1. Load (from TCL 🡪 IO-Controller and DMA)
2. Interface\_Enable = !Load & Interrupt & CNN/Image
3. Decompressor\_Enable = Load & Interrupt & CNN/Image
4. Interrupt (From TCL 🡪 IO-Controller)
5. CNN/Image (From TCL 🡪 IO-Controller {1 image/ 0 CNN})
6. Done (From DMA 🡪IO-Controller 🡪 TCL)
7. DMA\_Enable (From IO-Controller 🡪 DMA)
8. RAM\_Write, RAM\_Enable (From DMA 🡪 RAM)
9. CNN\_Enable (From IO-Controller 🡪 Coordinator)
10. DMA\_Done (From DMA 🡪 IO\_Controller)

**Design Units:**

1. IO-Controller:
   * Input:
     1. Load
     2. CNN/Image
     3. Interrupt
     4. DMA\_Done
   * Output:
     1. IO-Interface\_Enable
     2. Decompressor\_Enable
     3. CNN\_Enable
     4. Done
   * Function:
     1. Takes control signals From TCL script.
     2. Sets remain control signals to manage communication between other units.
2. IO-Interface:
   * Input:
     1. Din (16 bits From TCL script)
     2. IO-Interface\_Enable ( From IO-Controller)
   * Output:
     1. CompressedData (512 bits One Row from image 🡪 Decompressor)
   * Function:
     1. Works in case we load an image (CNN/Image =1).
     2. Receives 16 bits block each clock and combine them to form the entire compressed row.
     3. Sends it to Decompressor.
3. Decompressor:
   * Input:
     1. CompressedData (512 bits From IO-Interface).
     2. Decompressor\_Enable ( From IO-Controller)
   * Output:
     1. DecompressedData (512 bits Original image Row 🡪 DMA)
   * Function:
     1. Decompress input Row.
4. DMA:
   * Input:
     1. DecompressedRow (512 bits From Decompressor)
     2. Din (16 bits From TCL)
     3. DMA\_Enable ( From IO-Controller)
     4. CNN/Image (From IO-Controller)
     5. Load (From IO-Controller)
   * Output:
     1. RAM\_Write (🡪RAM)
     2. RAM\_Enable (🡪RAM)
     3. RAM\_Address (Adress to write in 🡪RAM)
     4. DataToWrite (Data to be stored 🡪 RAM)
     5. DMA\_Done ( 🡪 IO-Controller)
   * Function:
     1. In case of CNN/Image =1 (Load Image)
        1. Splits the decompressed row into 16 bits blocks.
        2. Write each block in the ram each clock cycle.
        3. After writing a full row raise DMA\_Done signal.
     2. In case of CNN/Image =0 (Load CNN)
        1. Receive 16 bits block from TCL every clock cycle.
        2. Write the block in the ram

**IO Scenario:**

1. Set RST for one clock cycle.
2. Set signal interrupt – Set load, Reset CNN/Image.
   1. Send CNN each 16-bit block at a clock cycle
3. Reset Load, Set CNN/Image.
   1. Send one row from the compressed image, each 16 bits at a time
   2. Set load and wait for signal done
   3. When signal done rise, reset load and send the next row
   4. Repeat for all the image rows.