Cairo University - Faculty of Engineering
Computer Engineering Department
Computer Architecture

Team 5

Phase 2 Report

Name	Section	BN
Abdallah Hussien	2	2
Ali Adel	2	4
Mohamed Adel	2	21
Saad Eldeen Mohamed	1	26

Submitted to:

Eng/ **Maheed Hatem**

Academic Year:
2020 – 2021

Design Changes:

- Didn't implement branching and control hazards.
- Handled branching instructions in assembler only.

Hazards

Structural Hazards

- **Harvard architecture to handle memory access hazard**
  - Using two separate memories one for program instructions and the other for data to avoid the hazard.

Data Hazards

- **RAW**
  - Full forwarding unit.
    - Checks Rdstbits in (Memory, execution,wb) and the most updated one.
    - Checks Rsrcbits in execution with Rdstin (Memory,wb) and the most updated one.
- **WAW, WAR**
  - Won't reorder instructions so no need to handle them.
- **Load-Use**
  - Stalling for one clock cycle.
  - Hazard detection unit sends signal (Hazard detected).
  - Hazard detected disabled (IF/ID buffer, PC increment)
  - Hazard detected makes control unit out zeros.