Cairo University - Faculty of Engineering
Computer Engineering Department
Computer Architecture

Team 5

Phase 1 Report

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Submitted to:

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Instruction Format:

IR = 32 bit

Types of instructions

- 1-op
- 2-op
- Memory
- BR
- Signals (INT, RESET)

Those main types represented by the first three bits of the opcode (OP-A)

Bits indices		**15:13**	**12:9**	**2:0**
Type	**Operation**	**OP-A**	**OP-B**	**Rdst**
1-OP	NOP	000	0000	xxx
	SETC		0001	
	CLRC		0010	
	CLR Rdst		0011	
	NOT Rdst		0100	
	INC Rdst		0101	
	DEC Rdst		0110	
	NEG Rdst		0111	
	OUT Rdst		1000	
	IN Rdst		1001	
	RLC Rdst		1010	
	RRC Rdst		1011	

Bits indices		**31:16**	**15:13**	**12:9**	**5:3**	**2:0**
Type	**Operation**	**Offset / Imm**	**OP-A**	**OP-B**	**Rsrc**	**Rdst**
2-OP	MOV Rsrc, Rdst		001	0000	xxx	xxx
	ADD Rsrc, Rdst			0001		
	SUB Rsrc, Rdst			0010		
	AND Rsrc, Rdst			0011		
	OR Rsrc, Rdst			0100		
	IADD Rdst,Imm			0101		

Bits indices		**19:16**	**15:13**	**12:9**	**2:0**
Type	**Operation**	**Offset / Imm**	**OP-A**	**OP-B**	**Rdst**
2-OP	SHL Rsrc, Imm	xxxxx	001	0110	xxx
	SHR Rsrc, Imm			0111	

Bits indices		**31:16**	**15:13**	**12:9**	**2:0**
Type	**Operation**	**Offset / Imm**	**OP-A**	**OP-B**	**Rdst**
Memory	PUSH Rdst		010	0000	xxx
	POP Rdst			0001	
	LDM Rdst, Imm			0010	
	LDD Rdst, offset(Rsrc)			0011	
	STD Rdst, offset(Rsrc)			0100	
Branch	JZ Rdst		011	0000	xxx
	JN Rdst			0001	
	JC Rdst			0010	
	JMP Rdst			0011	
	CALL Rdst			0100	
	RET			0101	-
	RTI			0110	
Input SGL	Reset		111	0000	-
	Interrupt			0001	

Control Unit Design :

One Operand

	Alu Source **(1 bit)**	Alu Operation **(5bits)**	Read/Write **(1bit)**	Port I/O **(1 bit)**	Mem I/O **(1 bit)**	SP_Add/Subract **(1 bit)**	Push_Pop/ Load_Store **(1 bit)**	Sp Write **(1 bit)**	WB **(1 bit)**
NOP	0	00000	0	0	0	0	0	0	0
SETC	0	00010	0	0	0	0	0	0	0
CLRC	0	00011	0	0	0	0	0	0	0
CLR	0	00100	0	0	0	0	0	0	1
NOT	0	00101	0	0	0	0	0	0	1
INC	0	00110	0	0	0	0	0	0	1
DEC	0	00111	0	0	0	0	0	0	1
NEG	0	01000	0	0	0	0	0	0	1
OUT	0	00000	1	1	0	0	0	0	0
IN	0	00000	0	1	0	0	0	0	1
RLC	0	01111	0	0	0	0	0	0	1
RRC	0	10000	0	0	0	0	0	0	1

Two Operands

	Alu Source **(1 bit)**	Alu Operation **(5bits)**	Read/Write **(1bit)**	Port I/O **(1 bit)**	Mem I/O **(1 bit)**	SP_Add/Subract **(1 bit)**	Push_Pop /Load_Store **(1 bit)**	Sp Write **(1 bit)**	WB **(1 bit)**
MOV	0	00001	0	0	0	0	0	0	1
ADD	0	01001	0	0	0	0	0	0	1
SUB	0	01010	0	0	0	0	0	0	1
AND	0	01011	0	0	0	0	0	0	1
OR	0	01100	0	0	0	0	0	0	1
IADD	1	01001	0	0	0	0	0	0	1
SHL	1	01101	0	0	0	0	0	0	1
SHR	1	01110	0	0	0	0	0	0	1

Memory/Branch Operations

	Alu Source **(1 bit)**	Alu Operation **(5bits)**	Read/Write **(1bit)**	Port I/O **(1 bit)**	Mem I/O **(1 bit)**	SP_Add/Subract **(1 bit)**	Push_Pop/Load_Store **(1 bit)**	Sp Write **(1 bit)**	WB **(1 bit)**
PUSH	0	00000	1	0	1	0	0	1	0
POP	0	00000	0	0	1	1	0	1	1
LDM	1	00001	0	0	0	0	0	0	1
LDD	0	00000	0	0	1	0	1	0	1
STD	0	00000	1	0	1	0	1	0	0
JUMP	0	00000	0	0	0	0	0	0	0
CALL	0	00000	0	0	0	1	0	1	0
RET	0	00000	0	0	0	0	0	1	0

Pipeline Stages Design:

Fetching Stage (IF/ID Buffer) (29 bits):

1- Offset → 16 bits.
2- Opcode → 7 bits
3- Srcbits → 3 bits
4- Dstbits → 3 bits
5- PCUpdated → 32 bits (**optional** No Jump).

Decoding Stage (ID/EX Buffer) (115 bits):

1- Rsrc → 32 bits.
2- Rdst → 32bits
3- Srcbits → 3 bits
4- Dstbits → 3 bits
5- Offset Extended → 32 bits
6- PCUpdated → 32 bits (**optional** No Jump).
7- Control Signals (EX, M, WB) → 13 bits

Execution Stage (EX/M Buffer) (138 bits):

1- Rsrc → 32 bits.
2- AluResult → 32bits
3- SpBuffered → 32 bits
4- Dstbits → 3 bits
5- Offset Extended → 32 bits
6- PCUpdated → 32 bits (**optional** No Jump).
7- Control Signals (EX, M, WB) → 7 bits

MemoryStage (M/WB Buffer) (36 bits):

1- WriteBack Data→ 32bits
2- Dstbits → 3 bits
3- Control Signals (EX, M, WB) → 1 bits

Hazards

Structural Hazards

- **Harvard architecture to handle memory access hazard**
  - Using two separate memories one for program instructions and the other for data to avoid the hazard.

Data Hazards

- **RAW**
  - Full forwarding unit.
- **WAW, WAR**
  - Won’t reorder instructions so no need to handle them.
- **Load-Use**
  - Stalling for one clock cycle.