, • ABDALLA HELSAYED ELBORM

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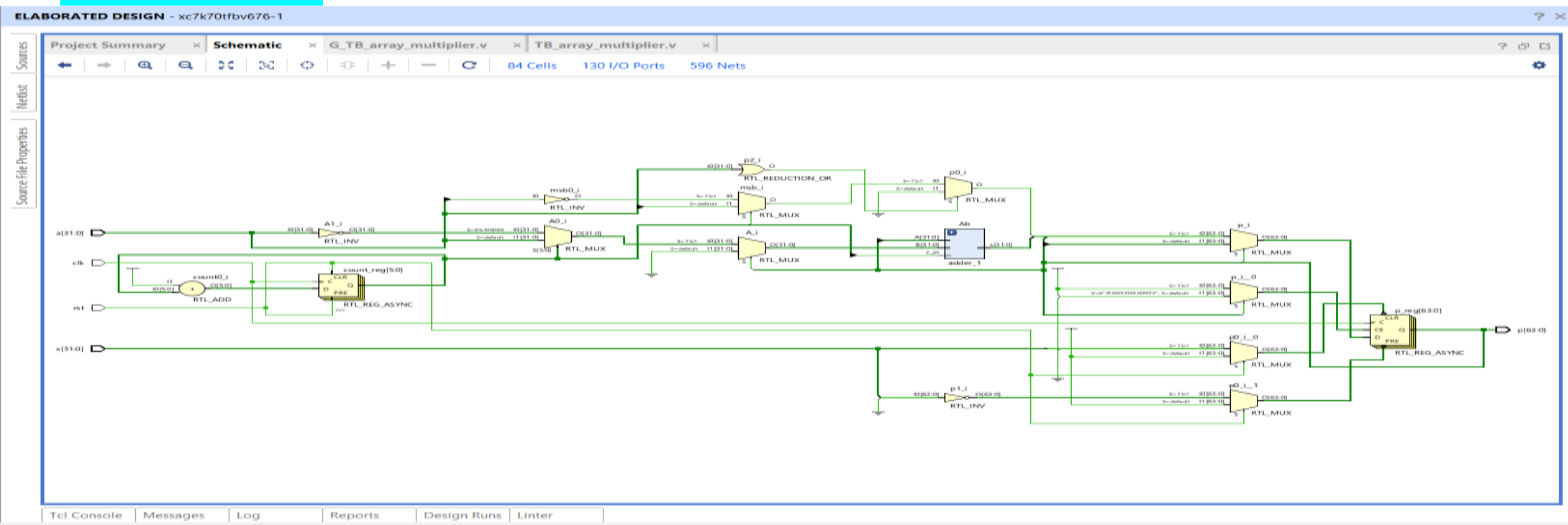
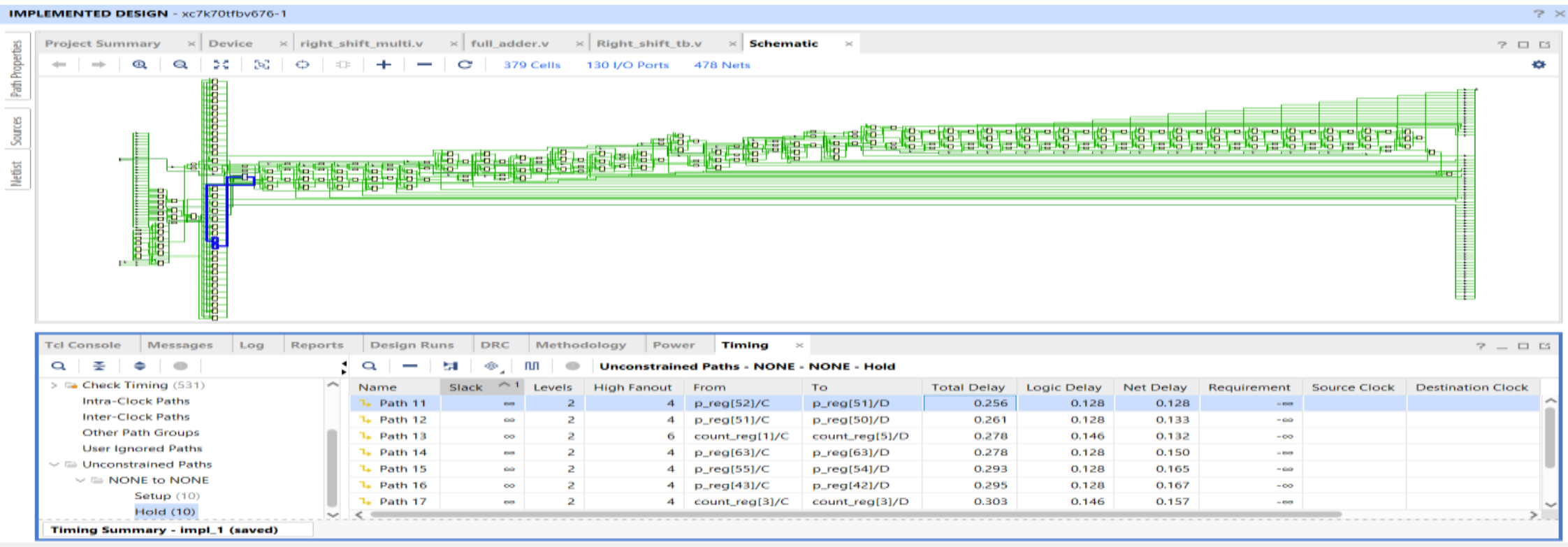
RIGHT SHIFT MULTIPLIER

Schematic



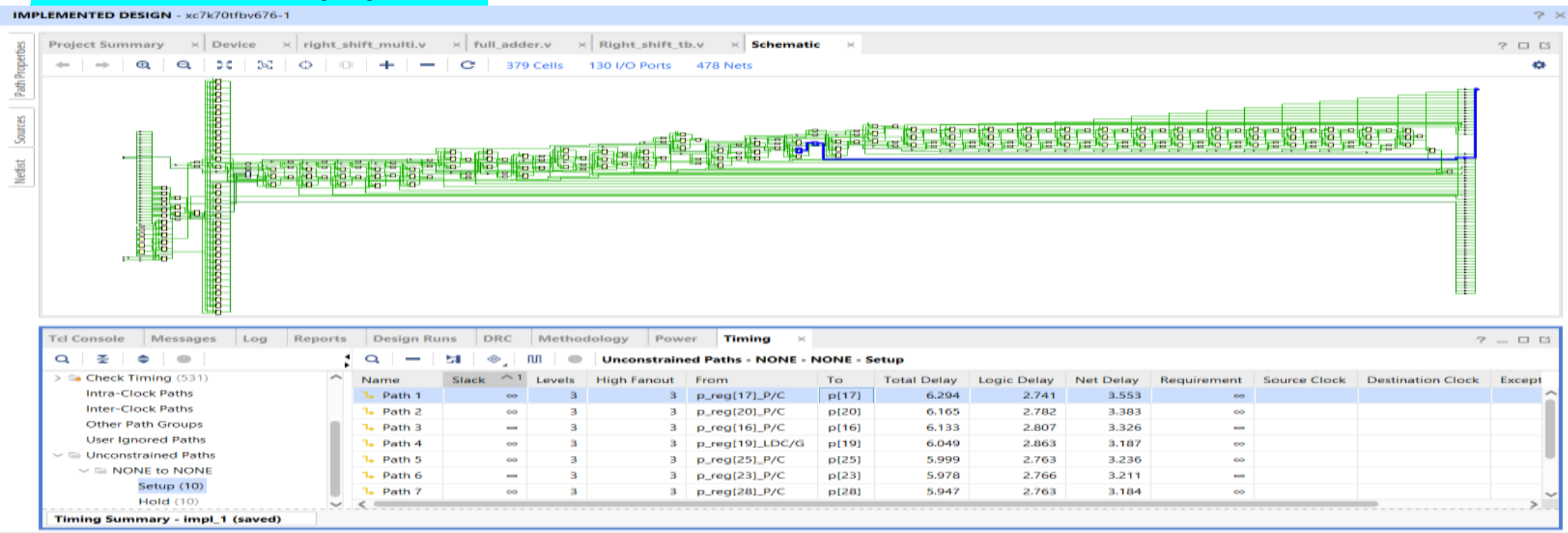
Critical Hold path



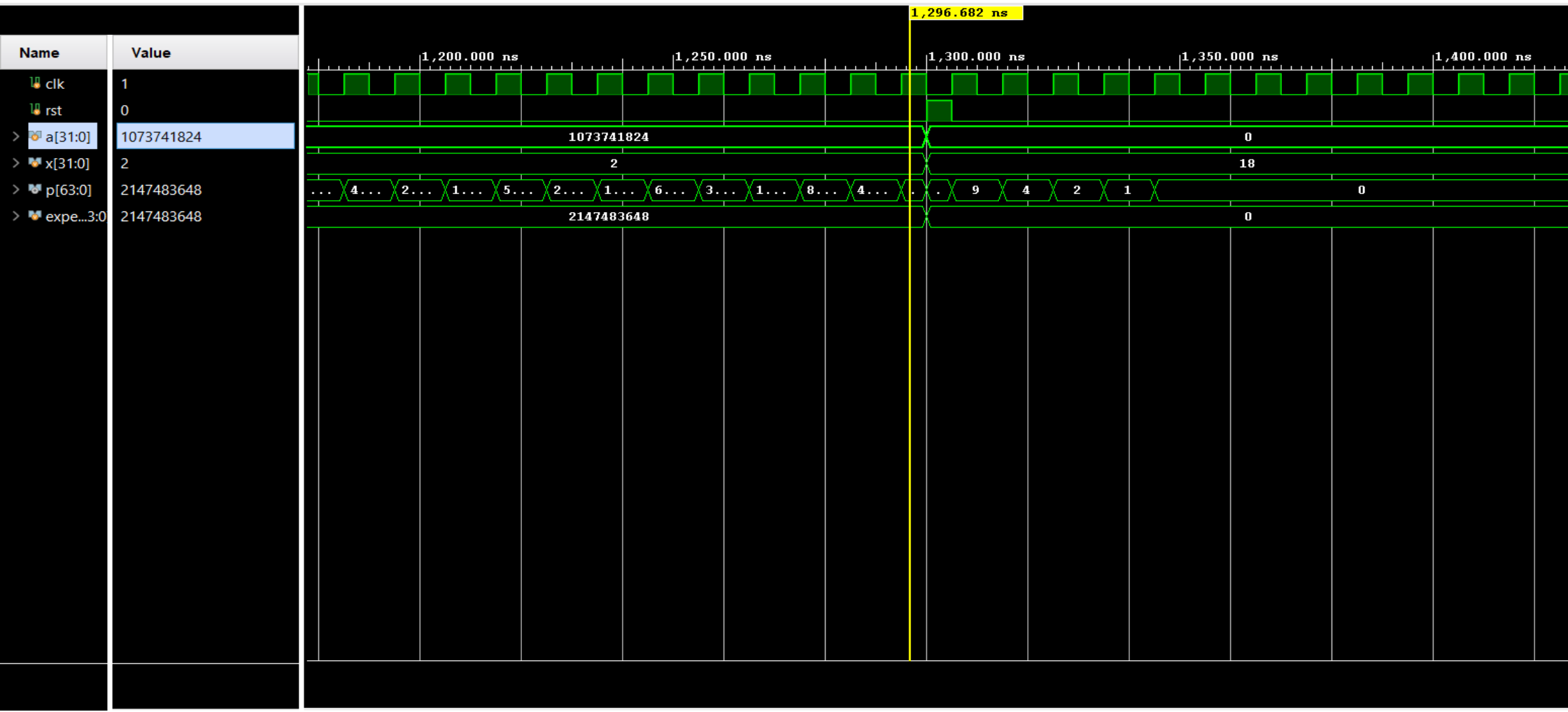
Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 11	∞	2	4	p_reg[52]/C	p_reg[51]/D	0.256	0.128	0.128	-∞		
Path 12	∞	2	4	p_reg[51]/C	p_reg[50]/D	0.261	0.128	0.133	-∞		
Path 13	∞	2	6	count_reg[1]/C	count_reg[5]/D	0.278	0.146	0.132	-∞		
Path 14	∞	2	4	p_reg[63]/C	p_reg[63]/D	0.278	0.128	0.150	-∞		
Path 15	∞	2	4	p_reg[55]/C	p_reg[54]/D	0.293	0.128	0.165	-∞		
Path 16	∞	2	4	p_reg[43]/C	p_reg[42]/D	0.295	0.128	0.167	-∞		
Path 17	∞	2	4	count_reg[3]/C	count_reg[3]/D	0.303	0.146	0.157	-∞		

RIGHT SHIFT MULTIPLIER

Critical setup path

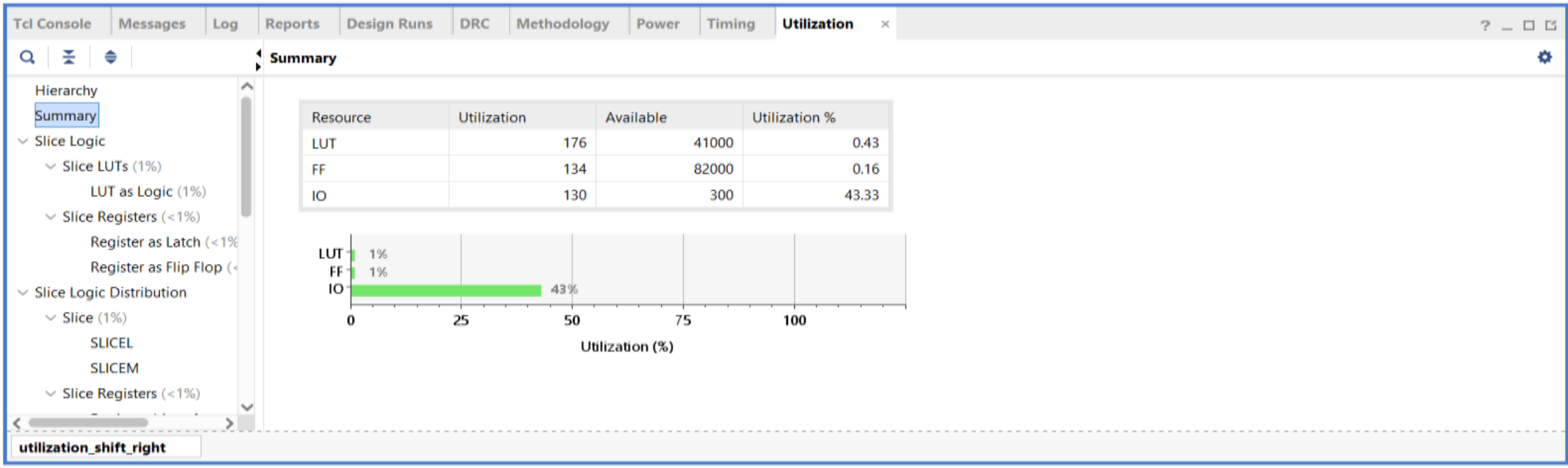


Wave form



RIGHT SHIFT MULTIPLIER

Utilization

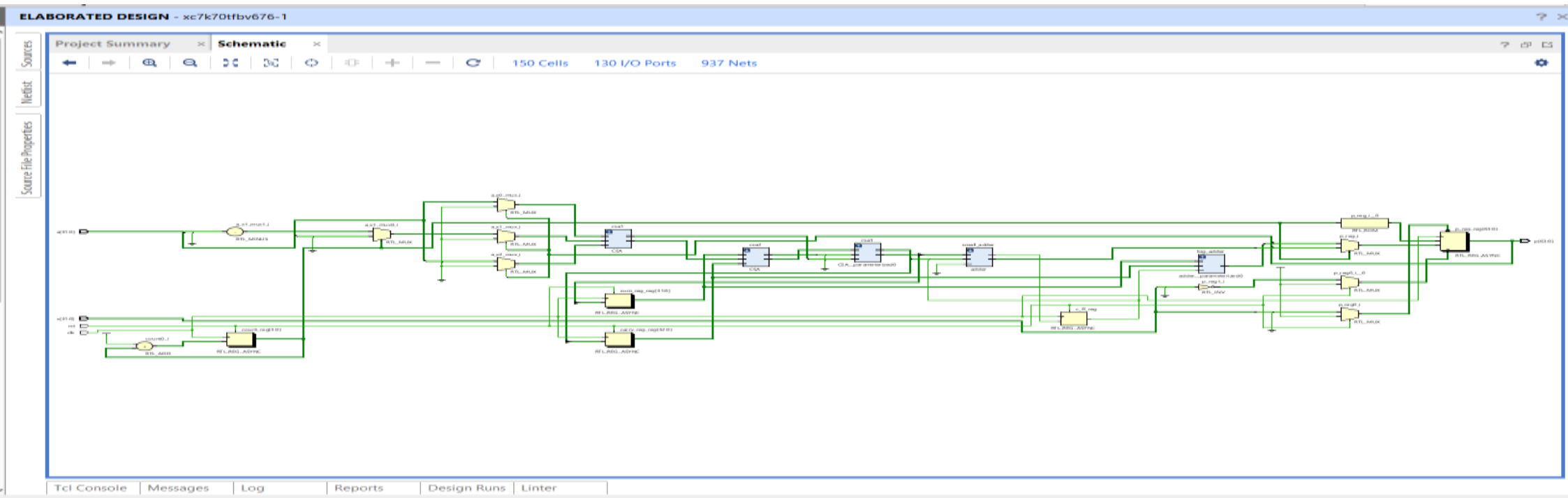


Test cases

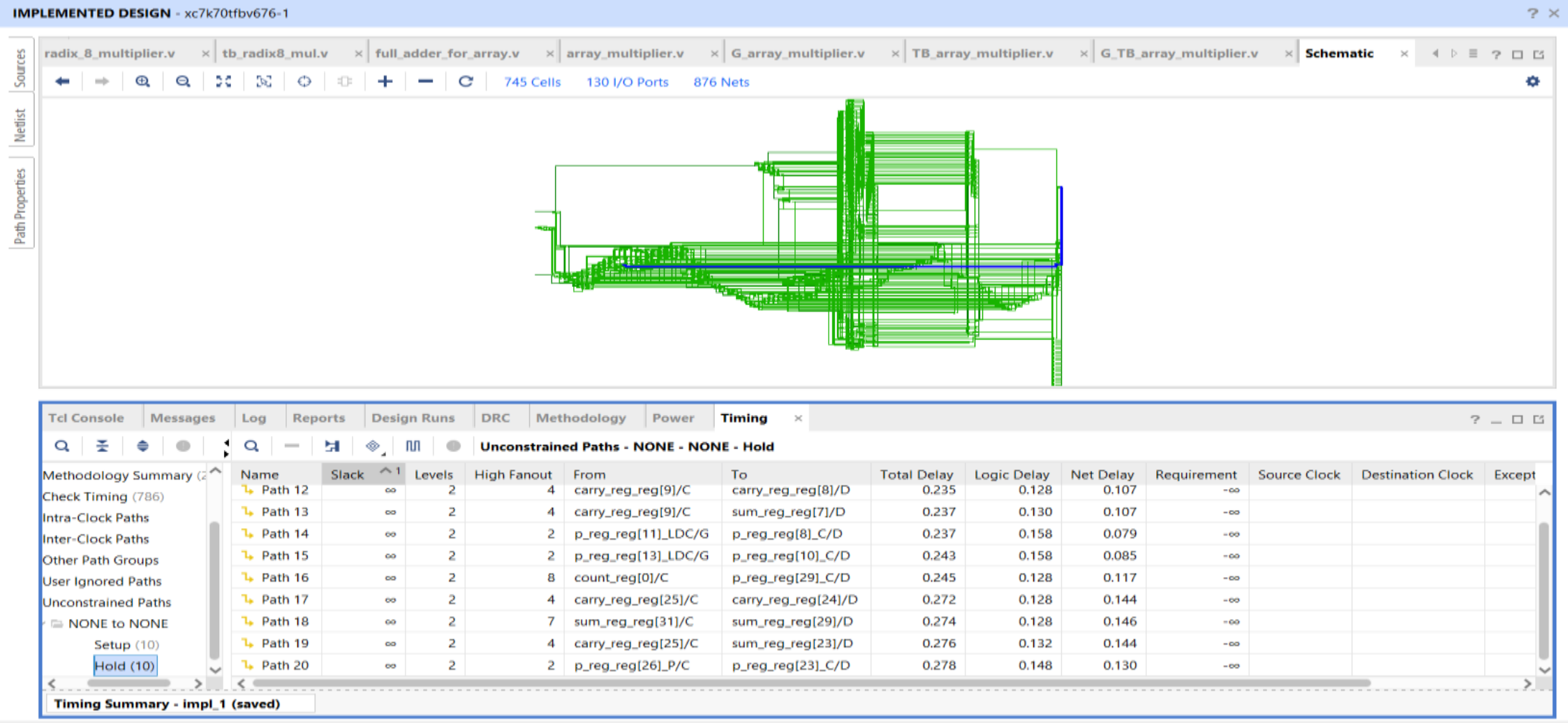
```
# Loading work.tb_R_shift_mul_32bitT(fast)
# Loading work.right_shift(fast)
# Loading work.adder_1(fast)
VSIM 109> run
#   305419896 *   305419896 =     93281312872650816 (expected     93281312872650816)
#   439041101 *   287454020 =    126204129427676020 (expected    126204129427676020)
#  2147483647 *           2 =           4294967294 (expected           4294967294)
#  1073741824 *           2 =           2147483648 (expected           2147483648)
run
#           0 *          18 =                    0 (expected                    0)
# -2147483648 *          -1 =           2147483648 (expected           2147483648)
#  1985229328 *   305419896 =    606328534893909888 (expected    606328534893909888)
#           2 *          -3 =                   -6 (expected                   -6)
#          -2 *           3 =                   -6 (expected                   -6)
VSIM 110> run
#           1 * -1985229328 =          -1985229328 (expected          -1985229328)
```

RADIX_8 MULTIPLIER CSA

Schematic



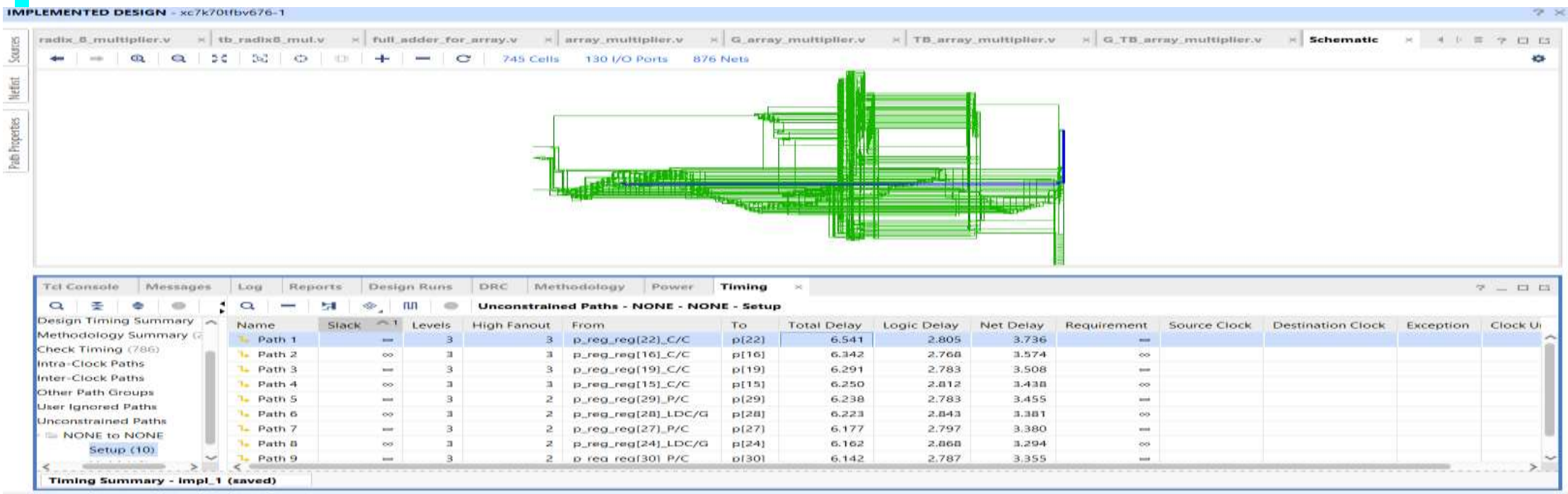
Critical Hold path



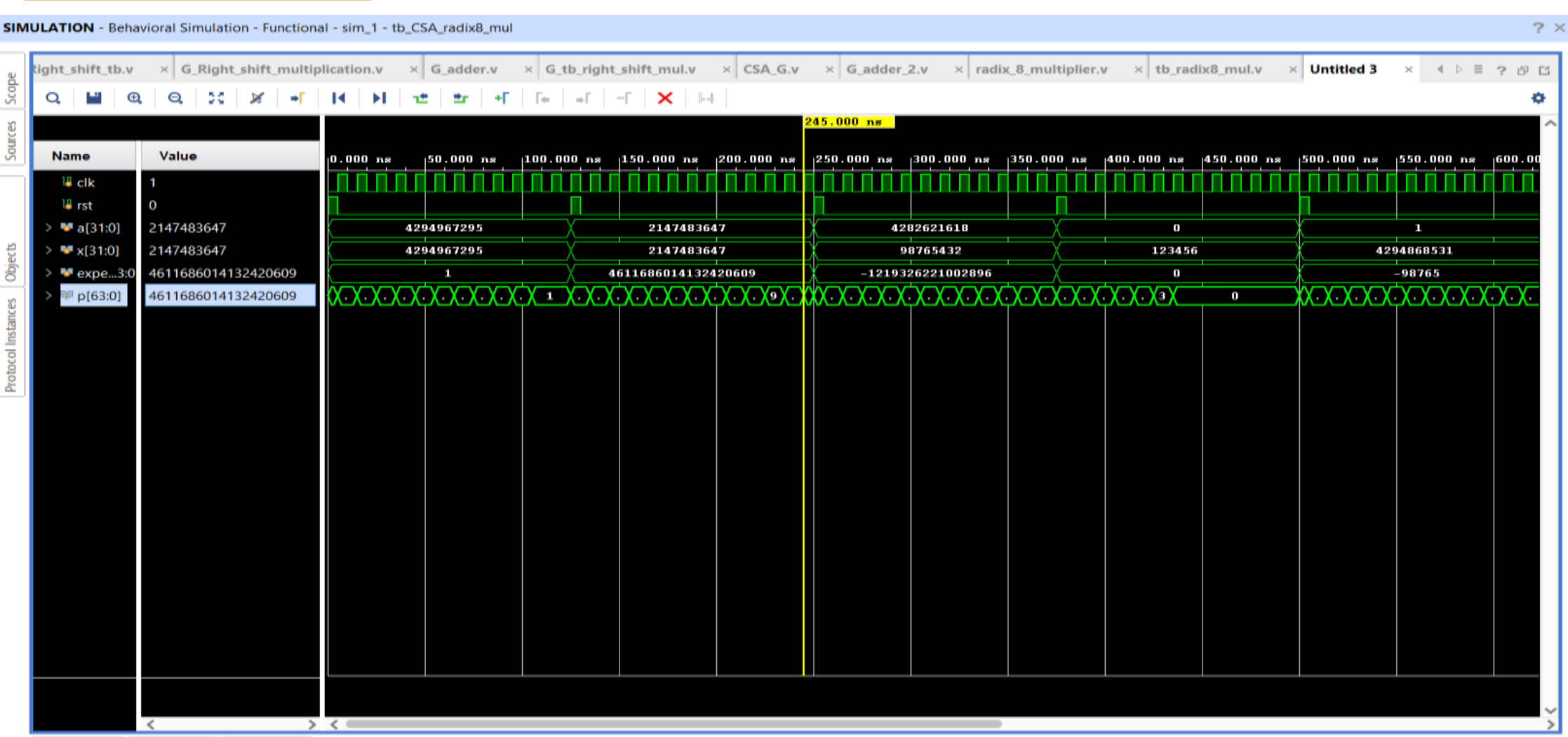
Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Except
Path 12	∞	2	4	carry_reg_reg[9]/C	carry_reg_reg[8]/D	0.235	0.128	0.107	-∞			
Path 13	∞	2	4	carry_reg_reg[9]/C	sum_reg_reg[7]/D	0.237	0.130	0.107	-∞			
Path 14	∞	2	2	p_reg_reg[11]_LDC/G	p_reg_reg[8]_C/D	0.237	0.158	0.079	-∞			
Path 15	∞	2	2	p_reg_reg[13]_LDC/G	p_reg_reg[10]_C/D	0.243	0.158	0.085	-∞			
Path 16	∞	2	8	count_reg[0]/C	p_reg_reg[29]_C/D	0.245	0.128	0.117	-∞			
Path 17	∞	2	4	carry_reg_reg[25]/C	carry_reg_reg[24]/D	0.272	0.128	0.144	-∞			
Path 18	∞	2	7	sum_reg_reg[31]/C	sum_reg_reg[29]/D	0.274	0.128	0.146	-∞			
Path 19	∞	2	4	carry_reg_reg[25]/C	sum_reg_reg[23]/D	0.276	0.132	0.144	-∞			
Path 20	∞	2	2	p_reg_reg[26]_P/C	p_reg_reg[23]_C/D	0.278	0.148	0.130	-∞			

RADIX_8 MULTIPLIER CSA

Critical setup path



Wave form



RADIX_8 MULTIPLIER CSA

Utilization

Tcl Console | Messages | Timing | **Utilization** | Debug | Linter

Hierarchy

- Hierarchy
- Summary
- Slice Logic
  - Slice LUTs (1%)
    - LUT as Logic (1%)
  - Slice Registers (<1%)
    - Register as Flip Flop (<
    - Register as Latch (<1%)

Name	Slice LUTs (41000)	Slice Registers (82000)	Bonded IOB (300)	BUFGCTRL (32)
N radix_8_multiplier_CSA	329	198	130	1
big_adder (adder__parameterized0)	31	0	0	0

utilization_1

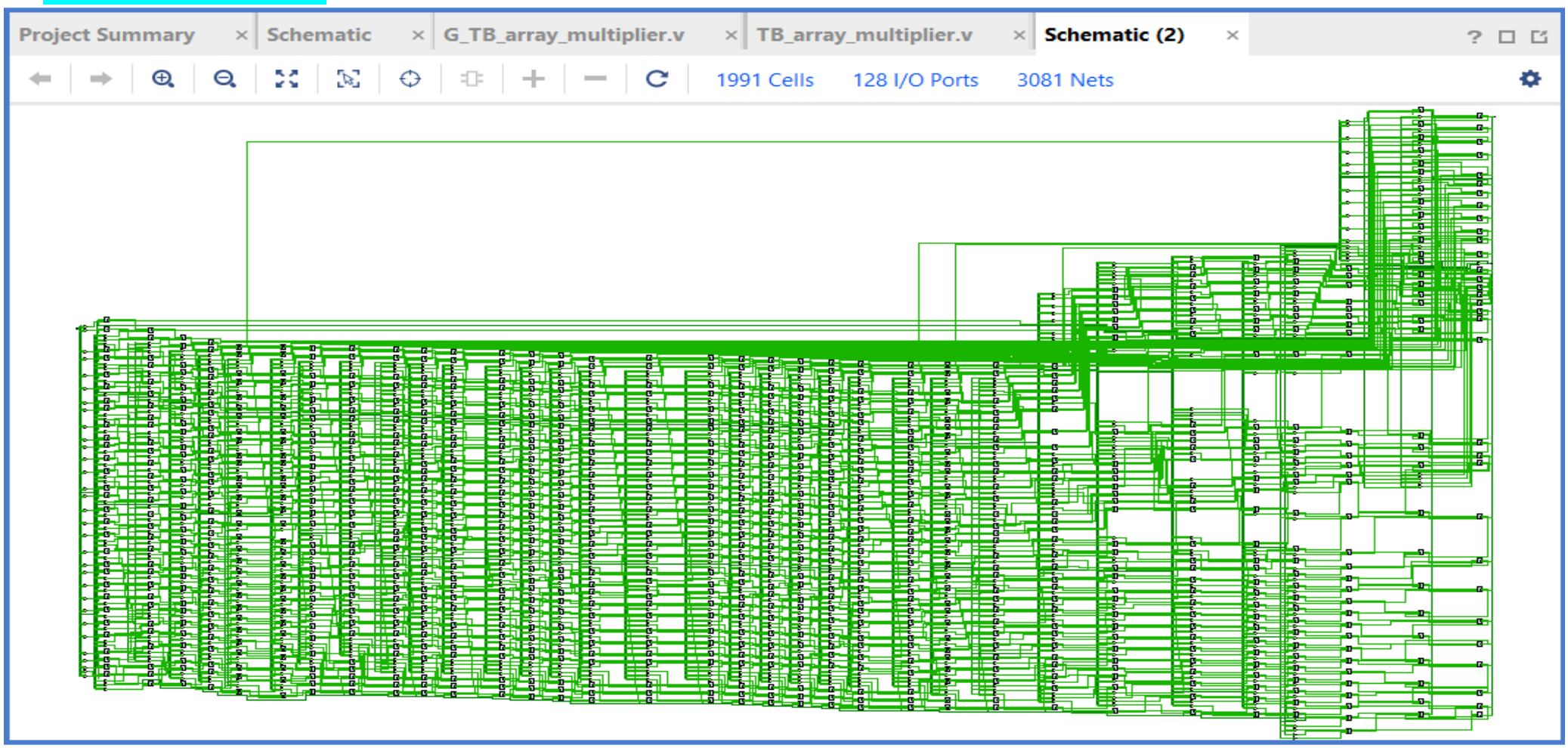
Test cases

```
#         -1 *         -1 =                    1 (expected                    1)
#  2147483647 *  2147483647 =   4611686014132420609 (expected   4611686014132420609)
#   -12345678 *    98765432 =     -1219326221002896 (expected     -1219326221002896)
#          0 *      123456 =                    0 (expected                    0)
#          1 *      -98765 =                -98765 (expected                -98765)
#         12 *          34 =                  408 (expected                  408)
# -2147483647 *           2 =           -4294967294 (expected           -4294967294)
#       1024 *        2048 =               2097152 (expected               2097152)
#         -3 *          -7 =                   21 (expected                   21)
#     987654 *      123456 =          121931812224 (expected          121931812224)
# ** Note: $stop    : C:/questasim64_2021.1/examples/random_project/r_8_CSA_M.v(236)
#    Time: 1250 ns  Iteration: 0  Instance: /tb_CSA_radix8_mul
# Break in Module tb_CSA_radix8_mul at C:/questasim64_2021.1/examples/random_project/r_8_CSA_M.v line 236

VSIM 3>
```

Array Multiplier

Schematic



Critical Hold path

Tcl Console | Messages | Log | Reports | Design Runs | DRC | Power | Linter | Timing

Unconstrained Paths - NONE - NONE - Hold

- Timer Settings
- Design Timing Summary
- Methodology Summary
- Check Timing (0)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths
- Unconstrained Paths
  - NONE to NONE
    - Setup (10)
    - Hold (10)

Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Clock Uncertainty
∞	3	122	a[31]	P[63]	2.742	1.523	1.218	-∞	input port clock			0.000
∞	4	122	a[31]	P[62]	2.764	1.542	1.222	-∞	input port clock			0.000
∞	3	55	a[0]	P[3]	2.798	1.421	1.377	-∞	input port clock			0.000
∞	4	115	a[29]	P[60]	2.810	1.559	1.251	-∞	input port clock			0.000
∞	4	134	a[30]	P[61]	2.888	1.601	1.286	-∞	input port clock			0.000
∞	3	55	a[0]	P[2]	2.904	1.447	1.457	-∞	input port clock			0.000
∞	4	117	a[11]	P[42]	2.907	1.494	1.413	-∞	input port clock			0.000
∞	4	91	a[27]	P[59]	2.992	1.560	1.432	-∞	input port clock			0.000
∞	4	121	a[16]	P[47]	2.999	1.536	1.463	-∞	input port clock			0.000
∞	3	55	a[0]	P[11]	3.029	1.442	1.587	-∞	input port clock			0.000

Timing Summary - impl_1 (saved)

Array Multiplier

Critical setup path

Tcl Console | Messages | Log | Reports | Design Runs | DRC | Power | Linter | Timing

Unconstrained Paths - NONE - NONE - Setup

- Timer Settings
- Design Timing Summary
- Methodology Summary
- Check Timing (0)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths
- Unconstrained Paths
  - NONE to NONE
    - Setup (10)
    - Hold (10)

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Clock
Path 1	∞	35	124	x[5]	P[62]	32.954	5.827	27.127	∞	input port clock			
Path 2	∞	35	124	x[5]	P[60]	32.946	5.830	27.116	∞	input port clock			
Path 3	∞	35	124	x[5]	P[61]	32.862	5.830	27.032	∞	input port clock			
Path 4	∞	34	124	x[5]	P[58]	32.817	5.664	27.153	∞	input port clock			
Path 5	∞	35	124	x[5]	P[63]	32.475	5.584	26.892	∞	input port clock			
Path 6	∞	34	124	x[5]	P[59]	32.305	5.647	26.658	∞	input port clock			
Path 7	∞	33	124	x[5]	P[55]	31.943	5.718	26.224	∞	input port clock			
Path 8	∞	33	124	x[5]	P[57]	31.934	5.485	26.449	∞	input port clock			
Path 9	∞	33	124	x[5]	P[56]	31.878	5.469	26.409	∞	input port clock			
Path 10	∞	31	124	x[5]	P[50]	31.860	5.617	26.244	∞	input port clock			

Timing Summary - impl_1 (saved)

Wave form

SIMULATION - Behavioral Simulation - Functional - sim_1 - TB_array_multiplier

G_TB_array_multiplier.v | Untitled 5 | TB_array_multiplier.v

Zoom In

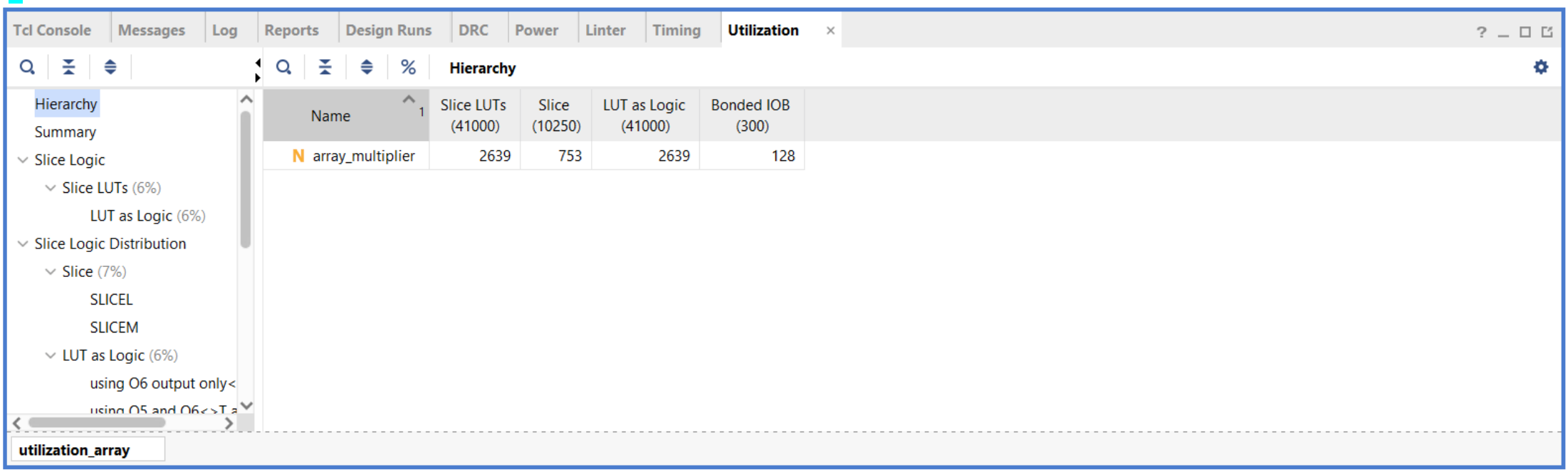
Name	Value
a[31:0]	2147483648
x[31:0]	4294967295
P[63:0]	2147483648
expe...3:0	2147483648

5.000 ns | 10.000 ns | 15.000 ns | 20.000 ns | 25.000 ns | 30.000 ns | 35.000 ns | 40.000 ns | 45.000 ns | 50.000 ns | 55.000 ns | 60.000 ns | 65.000

0	4294967295	4294967286	2147483647	10	4294967146	543		
0	4294967295	5	2147483647	4294967286	4294967291	9889		
0	1	-50	4611686014132420609	-100	750	5369727		
0	1	-50	4611686014132420609	-100	750	5369727		

Array Multiplier

Utilization



Test cases

```
# Loading work.TB_array_multiplier(fast)
# Loading work.array_multiplier(fast)
# Loading work.full_adder(fast)
VSIM 11> run
# Time = 0 | a =           0 | x =           0 | P =                    0 | Expected =                    0
# Time = 10000 | a =          -1 | x =          -1 | P =                    1 | Expected =                    1
# Time = 20000 | a =         -10 | x =           5 | P =                  -50 | Expected =                  -50
# Time = 30000 | a =  2147483647 | x =  2147483647 | P =   4611686014132420609 | Expected =   4611686014132420609
# Time = 40000 | a =          10 | x =         -10 | P =                 -100 | Expected =                 -100
# Time = 50000 | a =        -150 | x =          -5 | P =                  750 | Expected =                  750
# Time = 60000 | a =         543 | x =        9889 | P =              5369727 | Expected =              5369727
# Time = 70000 | a =         -45 | x =         569 | P =               -25605 | Expected =               -25605
# Time = 80000 | a =           0 | x =       33234 | P =                    0 | Expected =                    0
# Time = 90000 | a =        5678 | x =           0 | P =                    0 | Expected =                    0
# Time = 100000 | a =  2147483647 | x =           2 | P =           4294967294 | Expected =           4294967294
# Time = 110000 | a = -2147483648 | x =          -1 | P =           2147483648 | Expected =           2147483648
# ** Note: $stop    : C:/questasim64_2021.1/examples/random_project/array_mul.v(131)
#    Time: 120 ns  Iteration: 0  Instance: /TB_array_multiplier
# Break in Module TB_array_multiplier at C:/questasim64_2021.1/examples/random_project/array_mul.v line 131
```

قال رسول الله صلي الله عليه وسلم (من قال لأخية جزاك الله خيرا فقد أجزل في العطاء)

جزاك الله خيرا