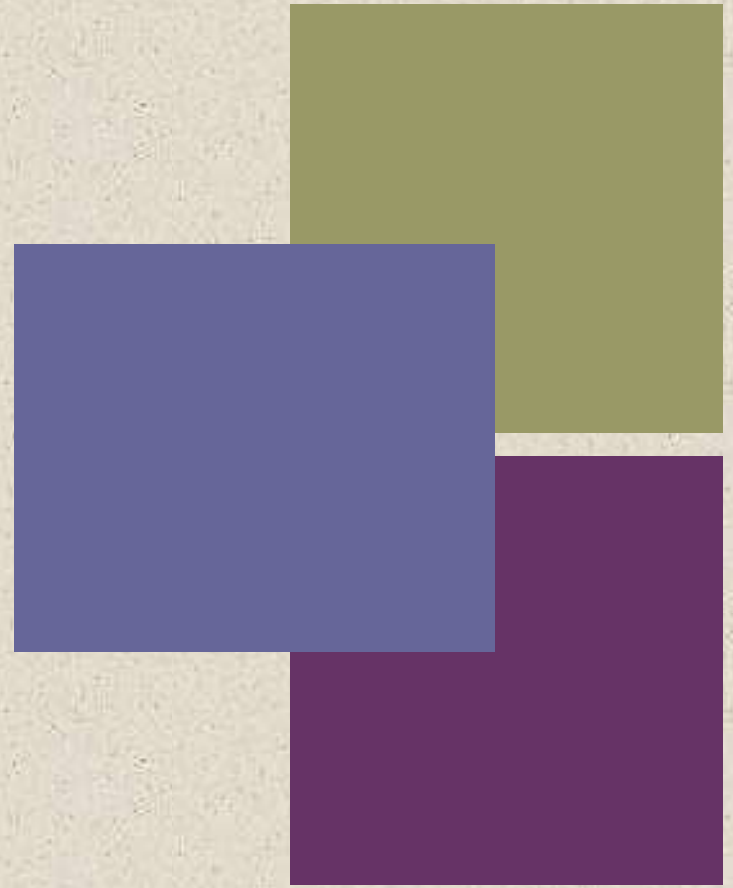
William Stallings
Computer Organization and Architecture
9th Edition



Chapter 2

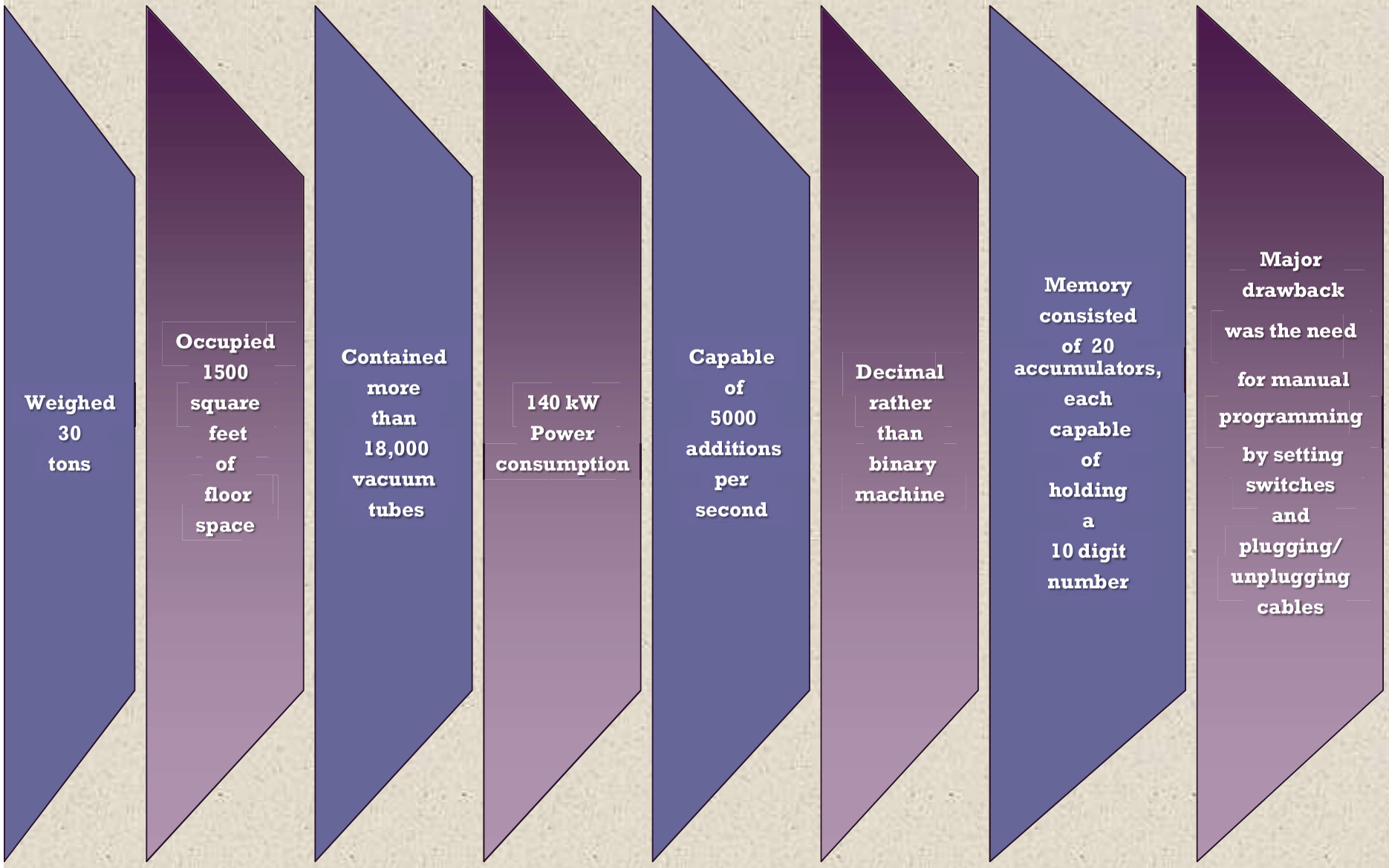
Computer Evolution and Performance

History of Computers

First Generation: Vacuum Tubes

- ENIAC
  - Electronic Numerical Integrator And Computer
- Designed and constructed at the University of Pennsylvania
  - Started in 1943 – completed in 1946
  - By John Mauchly and John Eckert
- World's first general purpose electronic digital computer
  - Army's Ballistics Research Laboratory (BRL) needed a way to supply trajectory tables for new weapons accurately and within a reasonable time frame
  - Was not finished in time to be used in the war effort
- Its first task was to perform a series of calculations that were used to help determine the feasibility of the hydrogen bomb
- Continued to operate under BRL management until 1955 when it was disassembled

ENIAC


Weighed 30 tons
Occupied 1500 square feet of floor space
Contained more than 18,000 vacuum tubes
140 kW Power consumption
Capable of 5000 additions per second
Decimal rather than binary machine
Memory consisted of 20 accumulators, each capable of holding a 10 digit number
Major drawback was the need for manual programming by setting switches and plugging/ unplugging cables

John von Neumann

EDVAC (Electronic Discrete Variable Computer)

- First publication of the idea was in 1945
- Stored program concept
  - Attributed to ENIAC designers, most notably the mathematician John von Neumann
  - Program represented in a form suitable for storing in memory alongside the data
- IAS computer
  - Princeton Institute for Advanced Studies
  - Prototype of all subsequent general-purpose computers
  - Completed in 1952

Structure of von Neumann Machine

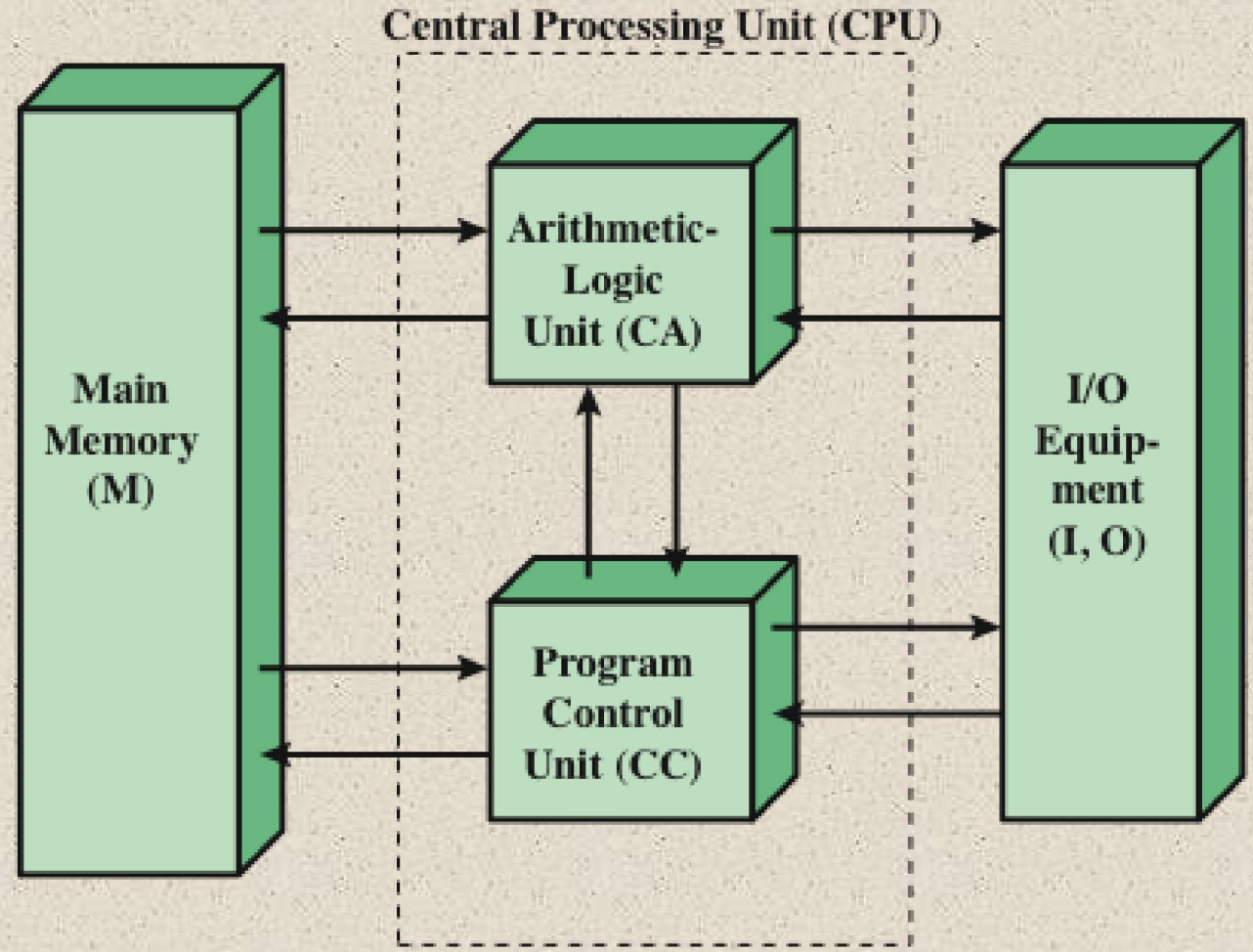


Figure 2.1 Structure of the IAS Computer

IAS Memory Formats

- The memory of the IAS consists of 1000 storage locations (called ***words***) of 40 bits each
- Both data and instructions are stored there
- Numbers are represented in binary form and each instruction is a binary code

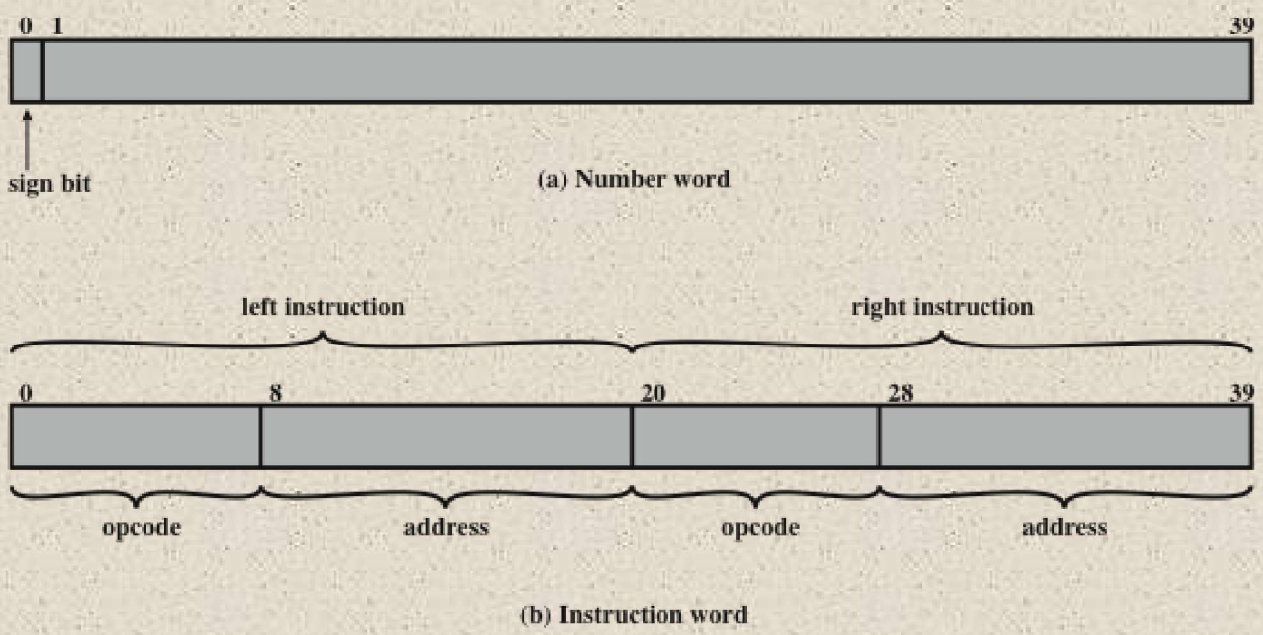


Figure 2.2 IAS Memory Formats

Structure of IAS Computer

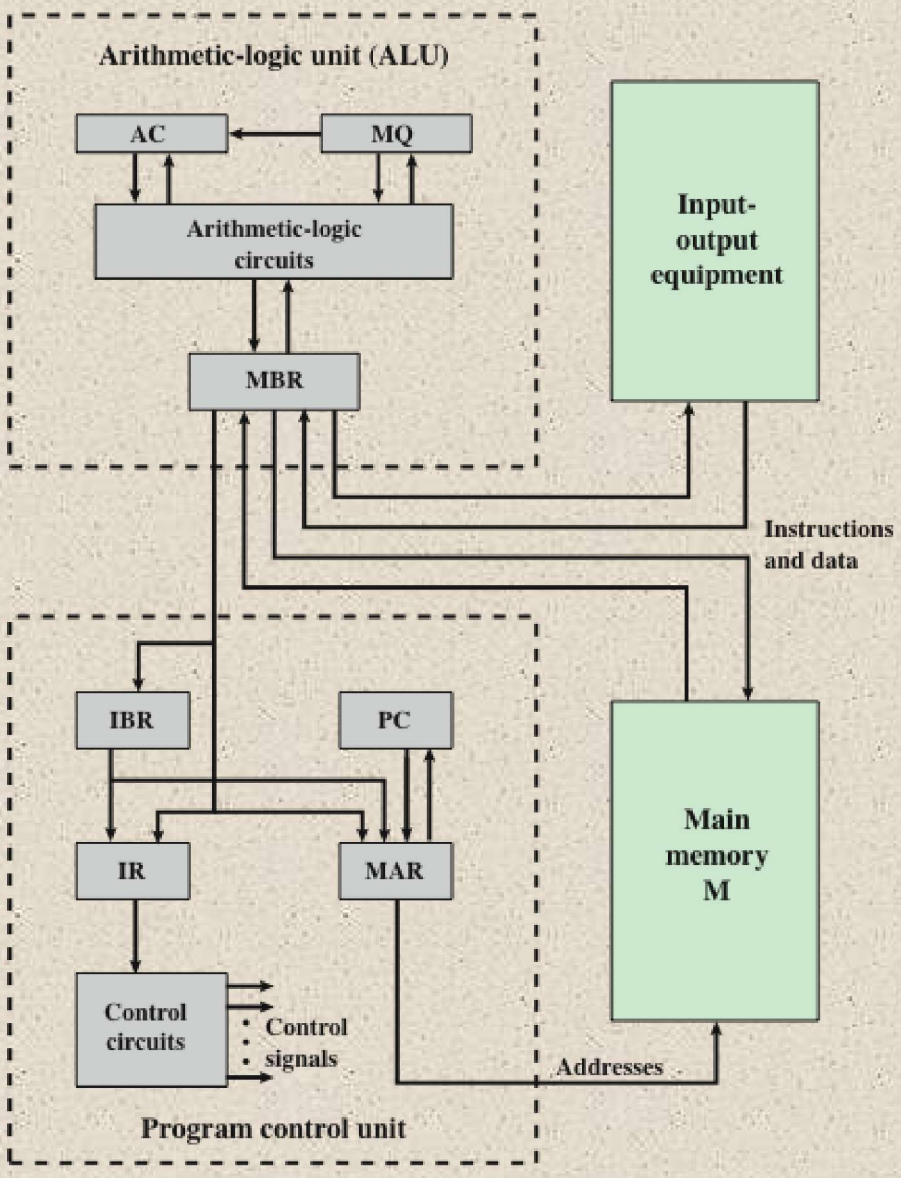


Figure 2.3 Expanded Structure of IAS Computer

Registers

Memory buffer register (MBR)	• Contains a word to be stored in memory or sent to the I/O unit • Or is used to receive a word from memory or from the I/O unit
Memory address register (MAR)	• Specifies the address in memory of the word to be written from or read into the MBR
Instruction register (IR)	• Contains the 8-bit opcode instruction being executed
Instruction buffer register (IBR)	• Employed to temporarily hold the right-hand instruction from a word in memory
Program counter (PC)	• Contains the address of the next instruction pair to be fetched from memory
Accumulator (AC) and multiplier quotient (MQ)	• Employed to temporarily hold operands and results of ALU operations

IAS Operations

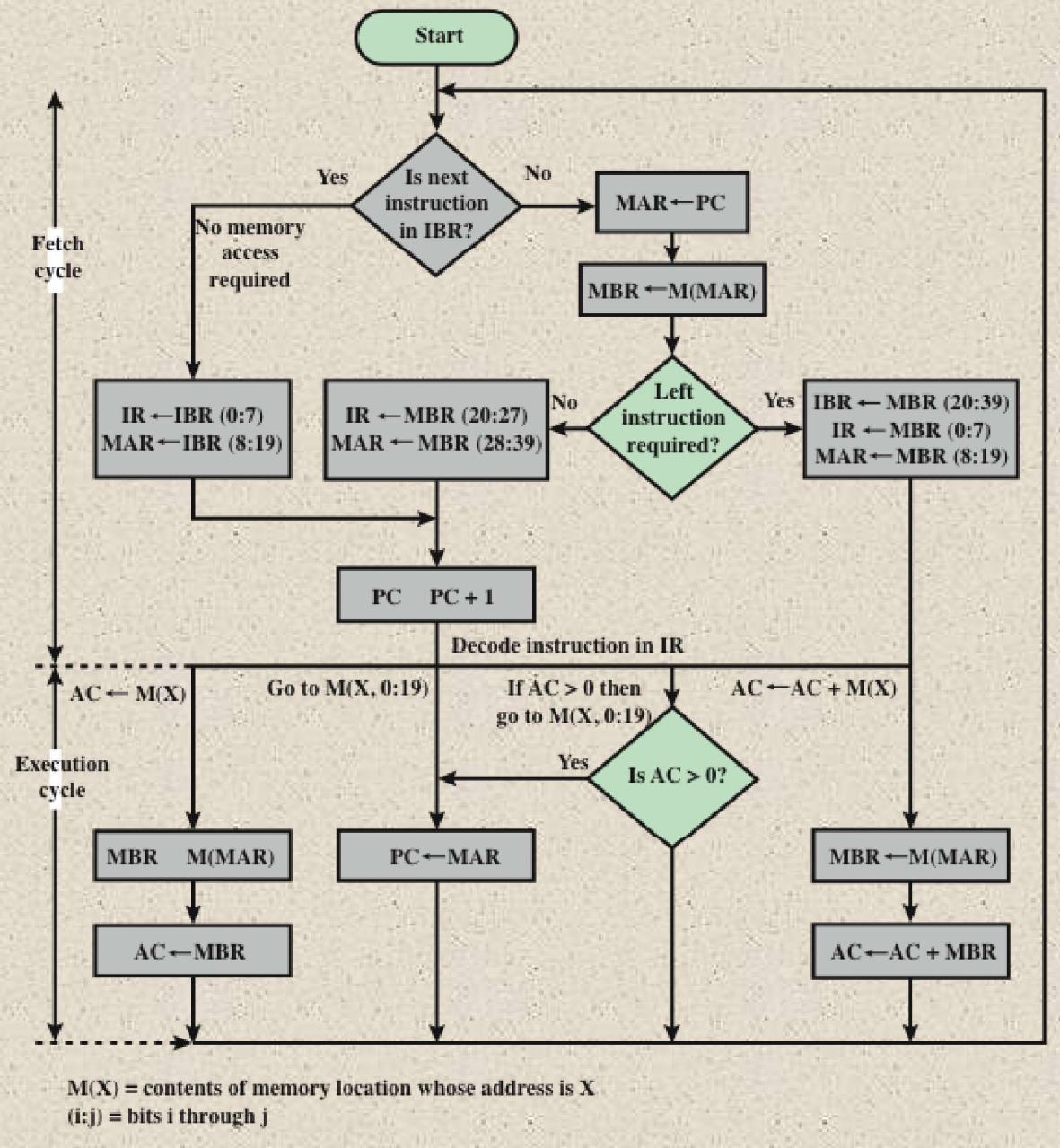


Figure 2.4 Partial Flowchart of IAS Operation