Cairo University
Faculty of Engineering
Computer Engineering

Computer Architecture
Lab 4

You are required to build the following:

- A 3-bit counter that starts at 0 at reset and increments with 1 each clock cycle. The counter increments only if the enable is set to 1.
- A RAM with width 16-bits and an address bus of 20-bits. The memory has 2^{20} entries.
- A small control unit that takes the counter as input and outputs the control signal to both the ram and the decoder. The control is shown in the table below.
- A 16-bit width input bus and 16-bit width output bus.

Input	Operation
1	Write the data from the input bus to address 0x0200
2	Read the data from address 0x0200 and write it to the output bus
3	Write the data from the input bus to address 0x0500 in one cycle, then write the data from the input bus to address 0x0501 in another cycle. You should disable the counter until you finish both cycles. **Hint**: You would need a variable to let you know which cycle is done.

0,4,5,6,7	Do nothing

Build a simulation wave by performing the following steps:

- Reset the wave
- Force the input bus with 0x00AA.

Run the simulation for 6 clock cycles.