Two-Stage Miller OTA

Mini Project

Information
Technology
Institute

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PART 1:OTA SPECS vs calculated

I will design ta have minimum AREA

	SPECS	CALCULATED
VDD	1.8V	1.8V
Static gain error	<= 0.05%	0.042%
CMRR@DC	>= 74dB	77.36db
Phase margin (avoid pole_zero doublets)	>= 70o	70.23 deg
OTA current consumption (without current source)	<= 60uA	58.56uA
CMIR_high	>= 1V	810mv
CMIR_low	<= 0.2V	92mv
Output swing	0.2 – 1.6V	0.154v – 1.645v
load	5pF	5pF
Buffer closed loop rise time (10% to 90%)	<= 70ns	34.27ns
Slew rate (SR)	$5V/\mu s$	5.094 $V/\mu s$
AREA	_	38.3 P

Use gm/Id methodology to design a differential input, single-ended output two-stage Miller-compensated OTA. The OTA is to be used as a buffer (unity gain feedback configuration) to probe sensitive internal signals in a complex mixed-signal design. The OTA should achieve the specs below

Use an ideal external 10uA DC current source in your test bench (not included in the OTA current consumption spec), but design your own bias circuit (current mirrors). Create a schematic and an appropriate symbol for the OTA.

PART 2: OTA Design

1) <u>**Detailed design procedure and hand analysis. Justify why you used NMOS or PMOS input pair for each stage**</u>**:**

First we want to get some information from our specs :

$* \ static\ error \leq 0.05\%$

$\frac{1}{LG} \leq 0.05\%$ $\quad ,LG \geq 2000 \quad ,\beta = 1 \quad so\ Avol =\geq 2000$

$we\ will\ design\ two\ stage\ first\ stage\ will\ take\ gain\ A\ and\ second \frac{A}{2}\ why?$

$becuase\ we\ want\ second\ stage\ be\ large\ to\ not\ amplify\ common\ mode\ gain\ from\ first$

$stage\ \ so\ A * \frac{A}{2} \geq 2000\ \ so\ A \geq 63.25\ and\ \frac{gm*ro}{2}\ (\text{first stage}) \geq 63.25\ ,\ \text{gm} * \text{ro} \geq 127$

as same gm*ro (second stage)>=63.25

- **CMRR >=74db**
  CMRR>=5011
  $(gm * ro)^2 \geq 5011 \quad , \quad gm\ ro \geq 70.8$
  $(we\ assume\ Rss = ro\ M5, 1, 2, 3, 4\ same\ ro)$

- **Current consumtion <=60uA**

  IB1+IB2<=60uA
- **phase margin >=70**
  I will make it ciritical damped so
  I want male Cc=0.5cl=2.5pF
  And IB2=4IB1

Avoid pole and zero doplets I will put RZ to make zero

Go to infinity $Rz = \frac{1}{gm7}$

- **CMIR is near to gnd so we will use Pmos input pair (CMIR : 0.2v:0.8v)**
  And because we mirror by pmos we will use second stage NMOS
  $Vinmax = VDD - Vov5 - vgs1 \quad , \quad Vinmin > vgs3 - vth1$

- **Output swing : 0.2v:1.6v**

$$Vov7 \leq vout \leq VDD - Vov6$$

So Vov6,7 should be <=200m

- $SR \geq \frac{5Mv}{s} \quad \left(SR = \frac{IB1}{C1+Cc}, ignore\ C1\right)\ if\ we\ assume\ Cc = 0.5Cl = 2.5p$
  $so\ IB1 = 5 * 2.5 = 12.5uA\ \ to\ achieve\ phase\ margin\ IB2 = 4IB = 60uA$
  $(bigger\ than\ total\ consumtoion)\ \ so$
  $assume\ SR = 5.2\ , Cc = 2.3PF \quad so\ IB1 = 12ua\ , IB2 = 48uA\ (total = 60uA)$

- $trise \leq 70n \quad (trisecl = 2.2\tau cl)\ ,\ \frac{Acl}{Wucl} \leq 31ns \quad , wu \geq 32.258rad \quad \left(wu = \frac{gm1}{Cc}\right)$

$$\frac{gm1,2}{Cc} \geq 32.258rad$$

$gm1,2 \geq 75uS\ \ , \qquad from\ static\ error\ wen\ know\ \mathbf{gm} * \mathbf{ro} \geq 127\ \mathbf{so\ ro} \geq 1.69\mathbf{M}$

We deduce

VDD =1.8

Iref=10ua

Cl=5pF

gm*ro (first stage)>=127 (must be $gm\ ro \geq 70.8$)

gm*ro (second stage)>=63.25

IB1+IB2<=60uA

Cc=0.5cl=2.5pF , IB2=4IB1 $, Rz = \frac{1}{gm7} =$

Pmos input pair

$Vinmax = VDD - Vov5 - vgs1$

$Vinmin > vgs3 - vth1$

$Vov6,7 \leq 200m$

$Cc = 2.3PF \quad , IB1 = 12ua\ , IB2 = 48uA$

$gm1,2 \geq 75uS$

$\mathbf{ro} \geq 1.69\mathbf{M}$

- **Design M1,2 (Pmos input pair) :**
  VDS=VDD/3 , VSB=0 , ID=6ua , gmro>=127 ,
  I will sweep on gm/id to have minimum area and avhive that vgs isnot too large to achive Vinmax.
- **design M3,4 (NMOS load) :**

  VDS=VDD/3 , VSB=0 , ID=6uA , ro = 1.32M

  (like what appear to me in M1,2)

  I will sweep on gm/id to have minimum area and avhieve that vgs isnot too large to achive Vinmin

- **Design M5 (tail source)**
  VDS=VDD/3 , VSB=0 , id=12uA
  I find vgs1,2 take 825m so V* to achieve vinmax <=175m but (icrease V* decrease area so I choose this)
  Ro I find it achieve CMRR I want minimize area
- **Design M6 (mirror second stage) : w6=4* w5=38.2 u, L6=L5=370n**
- **Design M8 (main mirror) : w8=(10/12) w5= 7.958 u , L8=L5 =370n**
- **Design M7 (CS second stage):**

  VDS=VDD/2 , VSB=0 , id=48uA

  VGS= VG3,4 (to have zero offset voltage) ,gmro>65

ID	6u
gm/ID	16
gm/gds	130
VDS	0.6
VSB	0

Results:

	Name	TT-27.0
1	ID	6u
2	IG	N/A
3	L	410n
4	W	15.99u
5	VGS	824.5m
6	VDS	600m
7	VSB	0
8	gm/ID	15.92
9	Vstar	125.6m
10	fT	605.5MEG
11	gm/gds	129.7
12	VA	8.146
13	ID/W	375.2m
14	gm/W	5.974
15	AREA	6.556p
16	gm	95.52u
17	gmb	39.77u
18	gds	736.5n
19	ro	1.358MEG
20	VTH	778.1m
21	VDSAT	100.4m
22	cgg	25.11f
23	cgs	17.44f

Figure 1:M1,M2

ID	6u
gm/ID	12
ro	1.32M
VDS	0.6
VSB	0

Results:

	Name	TT-27.0
1	ID	6u
2	IG	N/A
3	L	440n
4	W	2u
5	VGS	794.6m
6	VDS	600m
7	VSB	0
8	gm/ID	11.85
9	Vstar	168.8m
10	fT	3.884G
11	gm/gds	92.29
12	VA	7.79
13	ID/W	3
14	gm/W	35.54
15	AREA	880f
16	gm	71.08u
17	gmb	23.78u
18	gds	770.2n
19	ro	1.298MEG
20	VTH	701.9m
21	VDSAT	140.6m
22	cgg	2.912f
23	cgs	1.979f

Figure 2:M3,M4

ID	12u
Vstar	175m
ro	600K
VDS	0.6
VSB	0

Results:

	Name	TT-27.0
1	ID	12u
2	IG	N/A
3	L	370n
4	W	9.55u
5	VGS	896m
6	VDS	600m
7	VSB	0
8	gm/ID	11.25
9	Vstar	177.8m
10	fT	1.512G
11	gm/gds	80.33
12	VA	7.14
13	ID/W	1.257
14	gm/W	14.14
15	AREA	3.534p
16	gm	135u
17	gmb	53.62u
18	gds	1.681u
19	ro	595k
20	VTH	770.3m
21	VDSAT	156.1m
22	cgg	14.22f
23	cgs	10.1f

Figure 3:M5

Import: Plot 1B OK

LUT Settings

W	38.2u
ID/W	1.256
L	370n
VDS	0.9
VSB	0

Results:

	Name	TT-27.0
1	ID	47.98u
2	IG	N/A
3	L	370n
4	W	38.2u
5	VGS	891.4m
6	VDS	900m
7	VSB	0
8	gm/ID	11.39
9	Vstar	175.6m
10	fT	1.519G
11	gm/gds	97.42
12	VA	8.555
13	ID/W	1.256
14	gm/W	14.3
15	AREA	14.13p
16	gm	546.3u
17	gmb	216.5u
18	gds	5.608u
19	ro	178.3k
20	VTH	769.1m
21	VDSAT	153.6m
22	cgg	57.25f
23	cgs	40.71f

Y-Expr: gm/ID*fT

Plot Append

Figure 4:M6

ID	48u
VGS	794.6m
gm/gds	65
VDS	0.9
VSB	0

Results:

	Name	TT-27.0
1	ID	48.83u
2	IG	N/A
3	L	360n
4	W	10u
5	VGS	794.6m
6	VDS	900m
7	VSB	0
8	gm/ID	10.55
9	Vstar	189.7m
10	fT	6.206G
11	gm/gds	60.77
12	VA	5.763
13	ID/W	4.883
14	gm/W	51.49
15	AREA	3.6p
16	gm	514.9u
17	gmb	150u
18	gds	8.473u
19	ro	118k
20	VTH	681.2m
21	VDSAT	153m
22	cgg	13.2f
23	cgs	9.314f

Figure 5:M7

W	7.958 u
ID/W	1.25659
L	370n
VDS	0.9
VSB	0

Results:

	Name	TT-27.0
1	ID	10u
2	IG	N/A
3	L	370n
4	W	7.96u
5	VGS	891.4m
6	VDS	900m
7	VSB	0
8	gm/ID	11.38
9	Vstar	175.7m
10	fT	1.519G
11	gm/gds	97.41
12	VA	8.556
13	ID/W	1.257
14	gm/W	14.31
15	AREA	2.945p
16	gm	113.9u
17	gmb	45.13u
18	gds	1.169u
19	ro	855.4k
20	VTH	769.1m
21	VDSAT	153.6m
22	cgg	11.93f
23	cgs	8.483f

Figure 6:M8

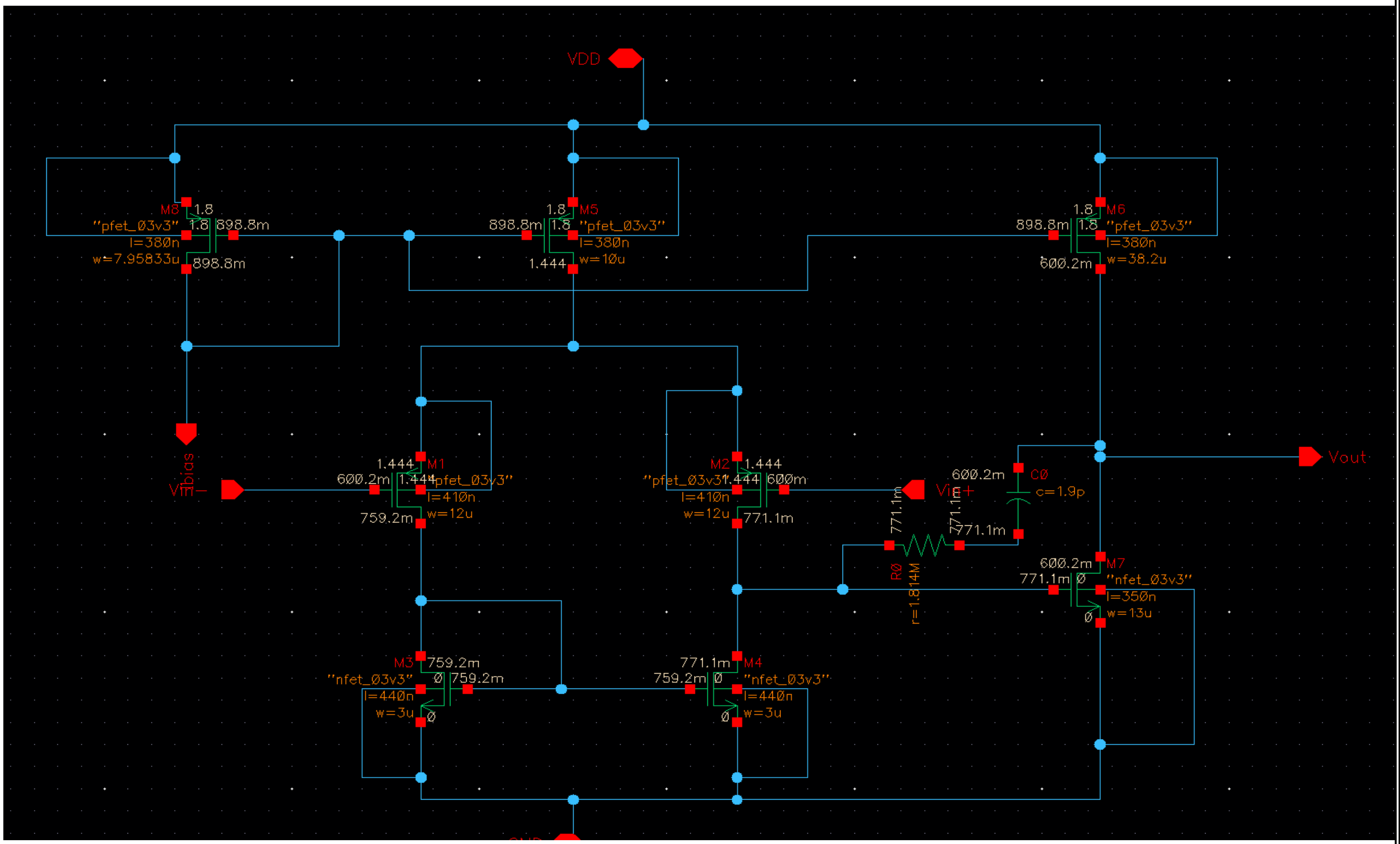
2) A table showing W, L, gm, ID, gm/ID, $vdsat$, $Vov = VGS - VTH$, and $V* = 2ID/gm$ of all transistors (as calculated from gm/ID curves)

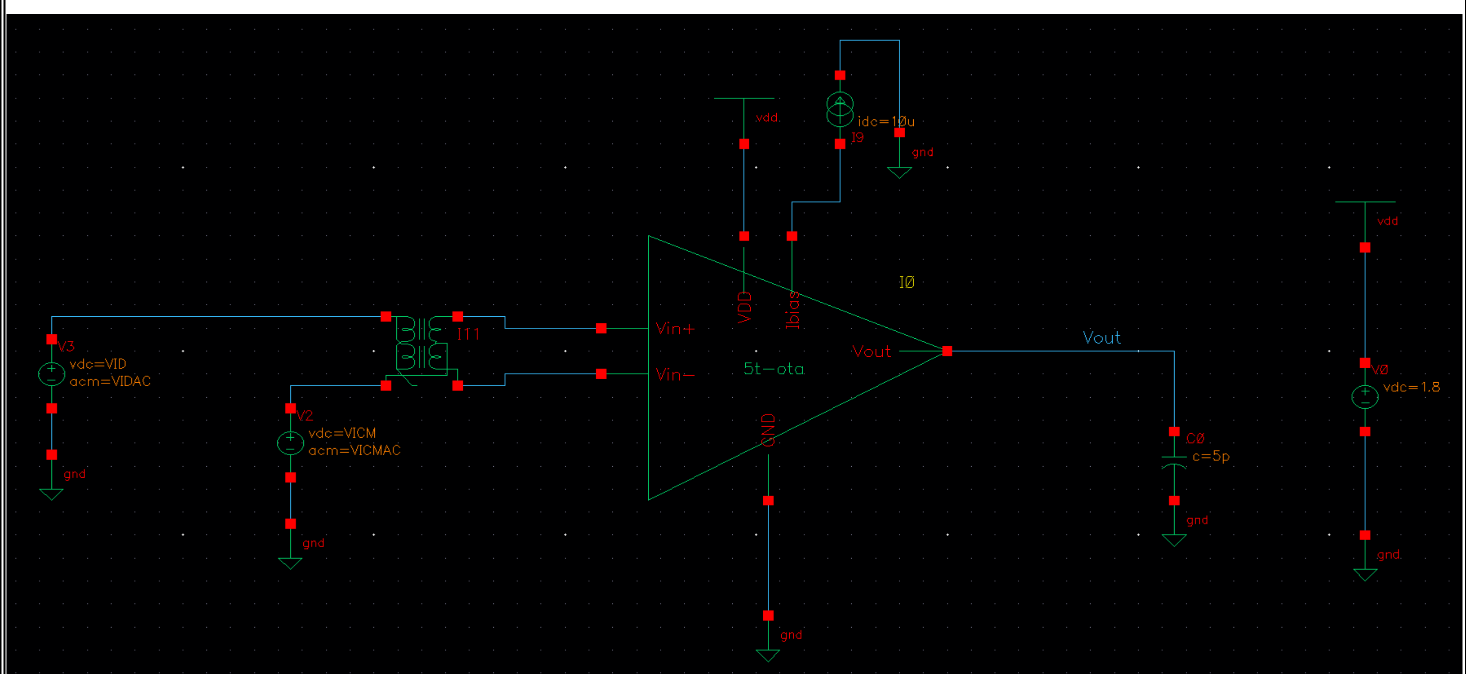
	M1,2	M3,4	M5	M6	M7	M8
W	15.99u	2u	9.55u	38.2u	10u	7.96u
L	410n	440n	370n	370n	360n	370n
Gm	95.52u	71.08u	135u	546.3u	514.9u	113.9u
Gm/id	15.92	11.85	11.25	11.39	10.55	11.38
Vdsat	100.4m	140.6m	156.1m	153.6m	153m	153.6m
Vov	46.4m	92.7m	25.7m	122m	113.4m	122m
V*	125.6m	168.8m	177.8m	175.6m	189.7m	175.7m

Its initial point not exact designed

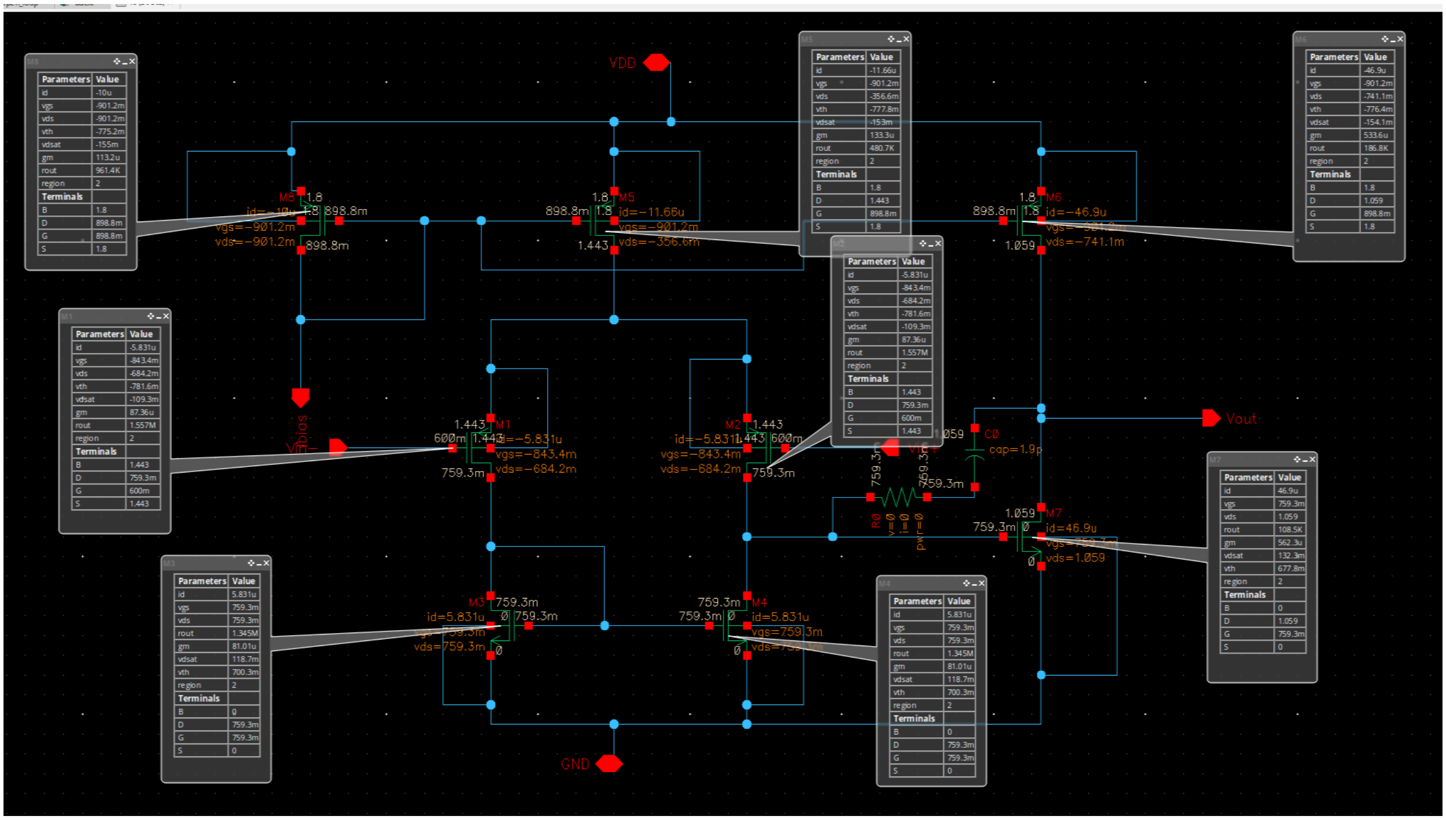
When we go to cadence we will find that some error in slewrate and phase margin we will decrease cc to improve slewrate and decrease gm1 to decrease gx and improve margin but it will affect on slewrate too , so we will increase gm2 to increase wp2 and improve margin take care increase w with same all things will make decrease vds might enter triode take care .

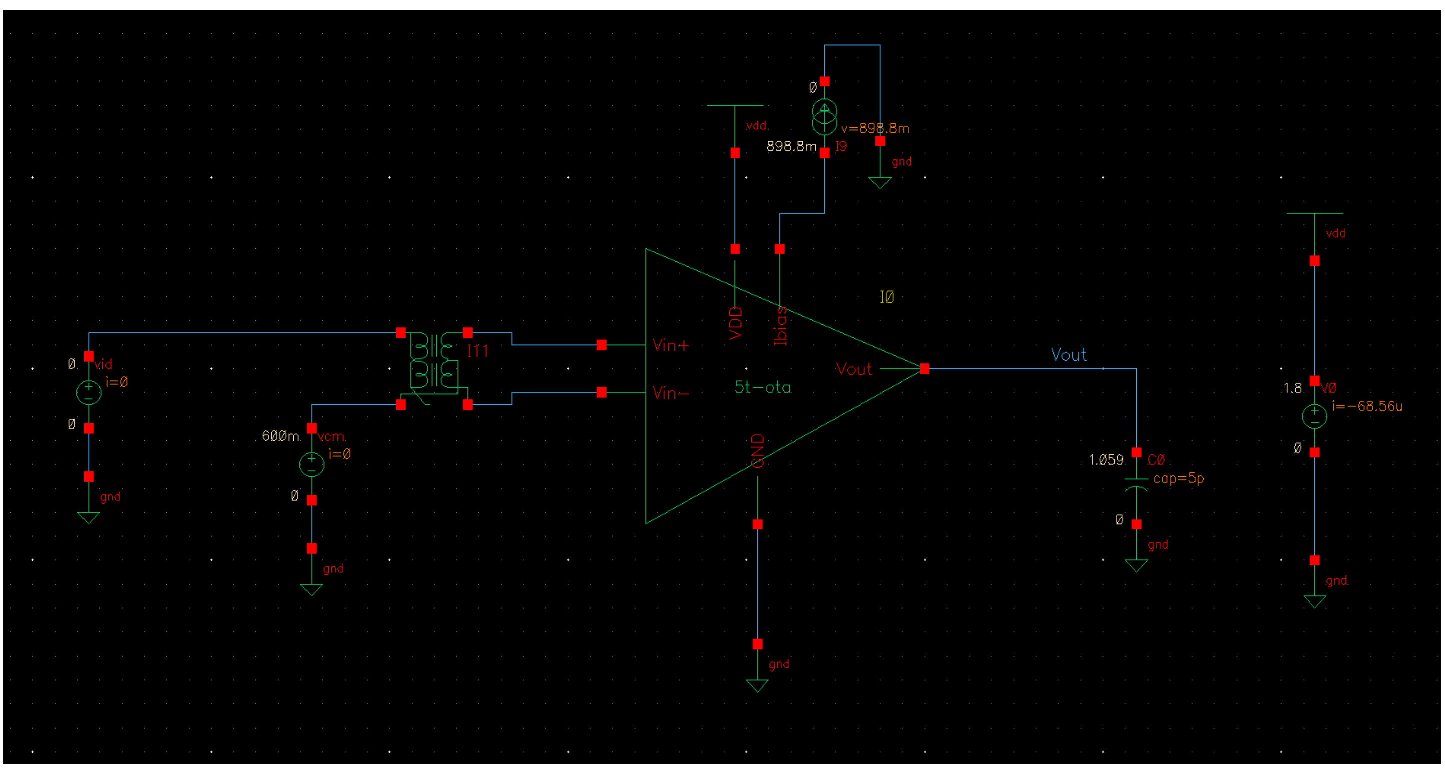
PART 3: Open-Loop OTA Simulation





1) **Schematic of the OTA and bias circuit with DC node voltages clearly annotated.**
   - **Use VICM = VDD/3.**





• **Is the current (and gm) in the input pair exactly equal?**

Yes,because same w,l,id like two halfes branches and same vin+=vin-

• **What is DC voltage at the output of the first stage? Why?**

759.3m , because equal VM and I design to vgs7=vgs3,4=759.3m to have zero offset voltage

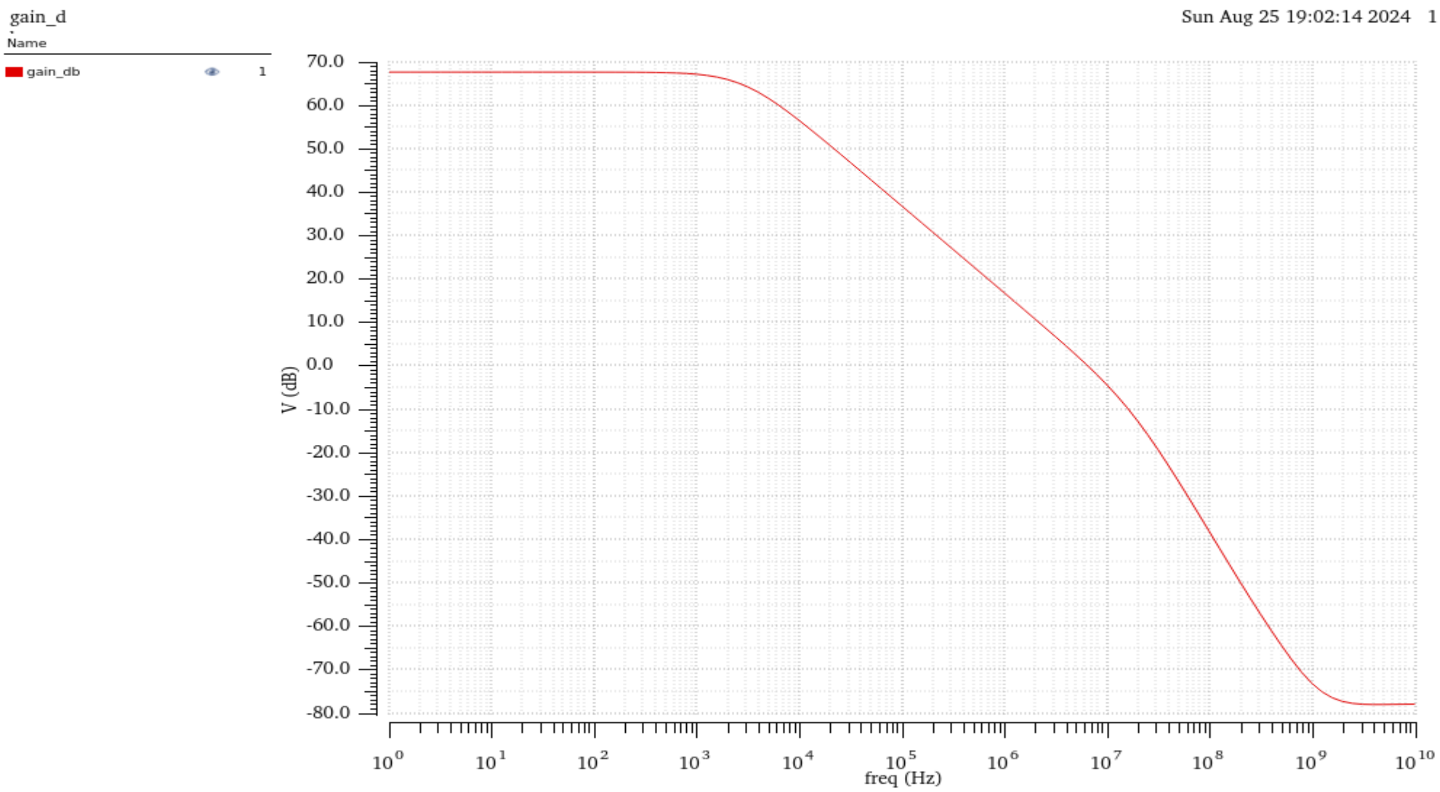
• **What is DC voltage at the second stage? Why?**

1.059 ,because vdd-vds6=1.8-.741=1.059

1) Diff small signal ccs:

• **Set VIDAC = 1 , VICMAC = 0 ,Use VICM = VDD/3.**

• **Plot diff gain (in dB) vs frequency.**



Test	Name	Type	Details
miniproject1:open_loop:1	A0	expr	ymax(mag(VF("/Vout")))
miniproject1:open_loop:1	A0_db	expr	dB20(ymax(mag(VF("/Vout"))))
miniproject1:open_loop:1	BW	expr	bandwidth(VF("/Vout") 3 "low")
miniproject1:open_loop:1	fu	expr	unityGainFreq(VF("/Vout"))
miniproject1:open_loop:1	GBW	expr	(A0 * BW)

miniproject1:open_loop:1	A0	2.422k
miniproject1:open_loop:1	A0_db	67.68
miniproject1:open_loop:1	BW	2.891k
miniproject1:open_loop:1	fu	6.622M
miniproject1:open_loop:1	GBW	7M

• **Compare simulation results with hand calculations in a table.**

Hand analysis:

Dc gain: $(gm1,2 * ro2\\ro4) * (gm7 * ro6\\ro7)$ **=2433**

BW: $\frac{1}{2*\pi*(ro2\\ro4)*(ro6\\ro7)*gm7*cc} = 3Khz$

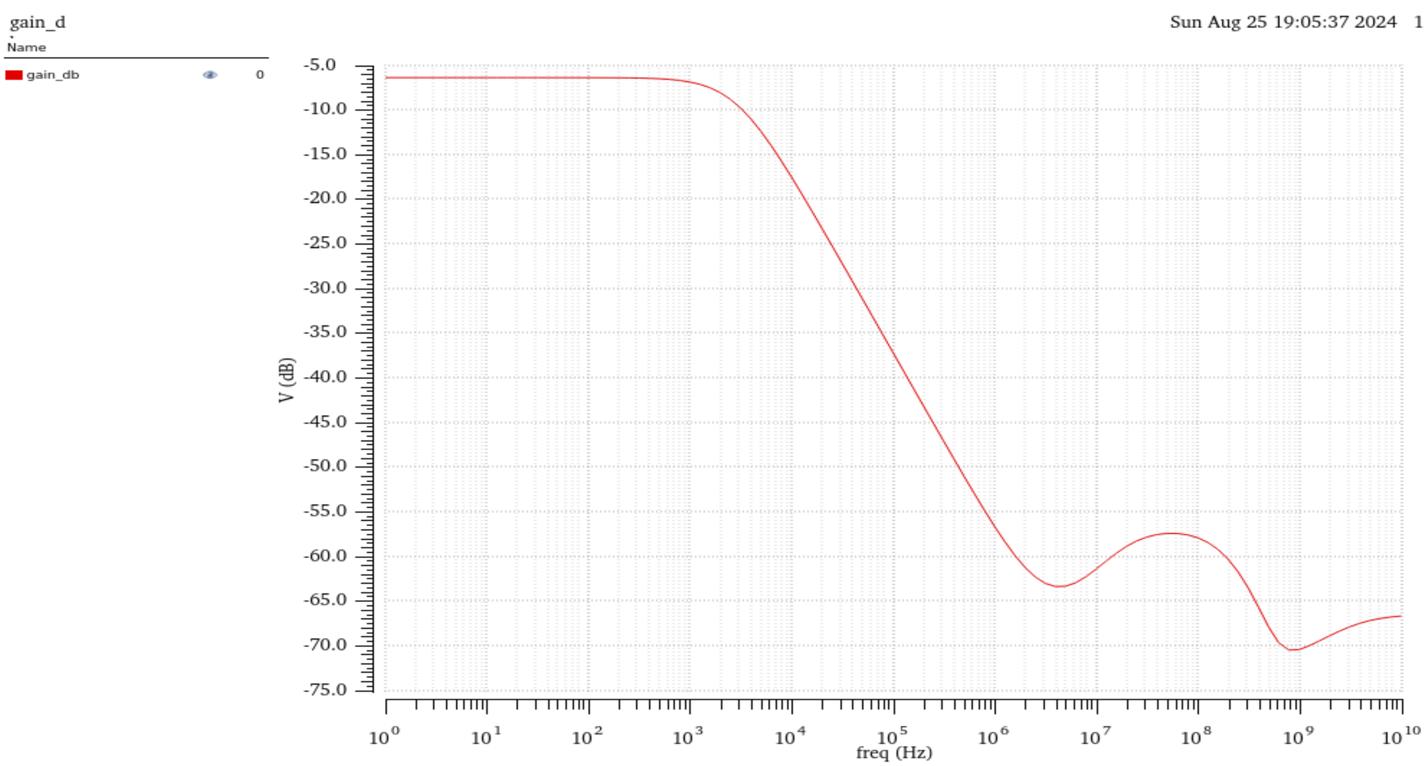
GBW: gain * Bw = 7.3Mhz

Fu: fu~gbw=7.3M

	Hand analysis	simulation
Dc gain	2433	2.422K
BW	3Khz	2.891khz
GBW	7.3Mhz	7Mhz
Fu	7.3Mhz	6.622Mhz

2) CM small signal ccs:

• **Plot CM gain in dB vs frequency.**



• **Compare simulation results with hand calculations in a table.**

Test	Name	Type	Details
miniproject1:open_loop:1	A0	expr	ymax(mag(VF("/Vout")))
miniproject1:open_loop:1	A0_db	expr	dB20(ymax(mag(VF("/Vout"))))
miniproject1:open_loop:1	BW	expr	bandwidth(VF("/Vout") 3 "low")
miniproject1:open_loop:1	fu	expr	unityGainFreq(VF("/Vout"))
miniproject1:open_loop:1	GBW	expr	(A0 * BW)

miniproject1:open_loop:1	A0	481.6m
miniproject1:open_loop:1	A0_db	-6.346
miniproject1:open_loop:1	BW	2.891k
miniproject1:open_loop:1	fu	eval err
miniproject1:open_loop:1	GBW	1.392k

Hand analysis:

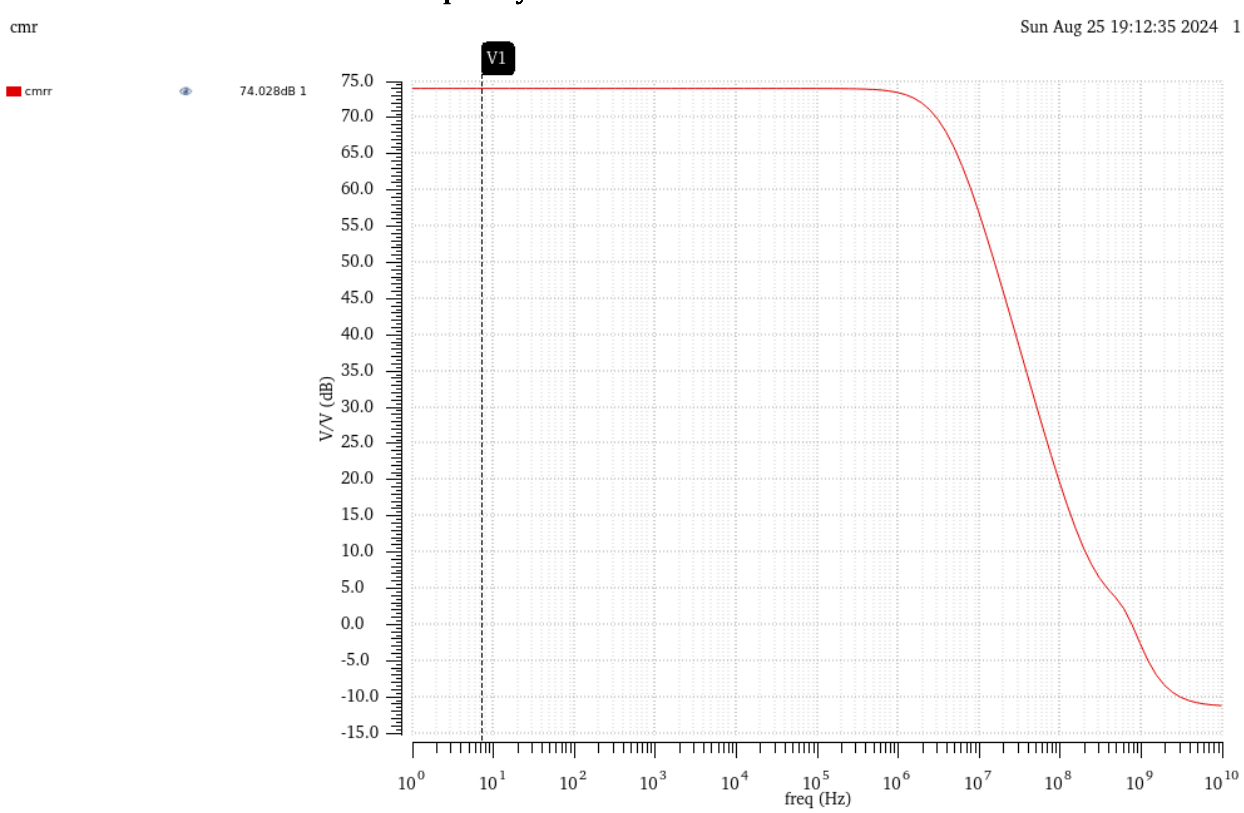
Dc gain: $\frac{1}{2*gm3,4*ro5} * (gm7 * ro6\backslash\backslash ro7) = 495m$, **BW:** $\frac{1}{2*\pi*(ro2\backslash\backslash ro4)*(ro6\backslash\backslash ro7)*gm7*cc} =$ **3Khz**

GBW: gain * Bw = 7.3Mhz , **Fu: not applicable because gain<0db**

	Hand analysis	simulation
Dc gain	495m	481.6m
BW	3Khz	2.891Khz
GBW	1.486khz	1.392khz
Fu	N/A	N/A

3) CMRR:

- **Plot CMRR in dB vs frequency.**



miniproject1:open_loop:1	cmrr	expr	dB20((mag(getData("/vid" ?result "xf")) / mag(getData("/vc...
miniproject1:open_loop:1	cmrr_dc	expr	ymax(dB20((mag(getData("/vid" ?result "xf")) / mag(getDat...

miniproject1:open_loop:1	cmrr	
miniproject1:open_loop:1	ymax(dB20((mag(getData("/vid" ...	74.03

- **Compare simulation results with hand calculations in a table.**

Hand analysis:

CMRR=Avd/Avcm (we get them from requirement 1, 2) = 4915=73.83db

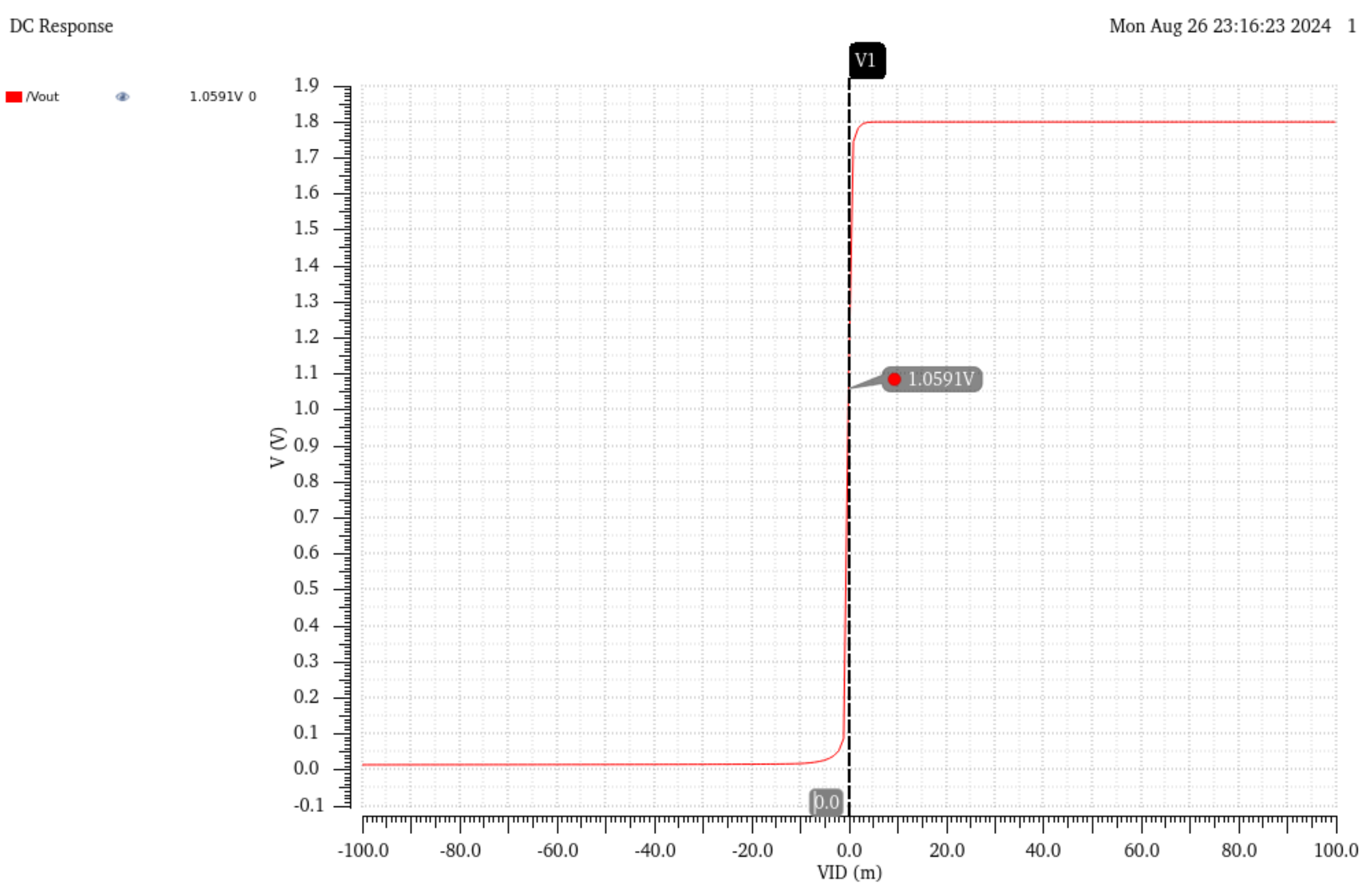
	Hand analysis	simulation
CMRR	**73.83db**	**74.03db**

2) Diff large signal ccs:

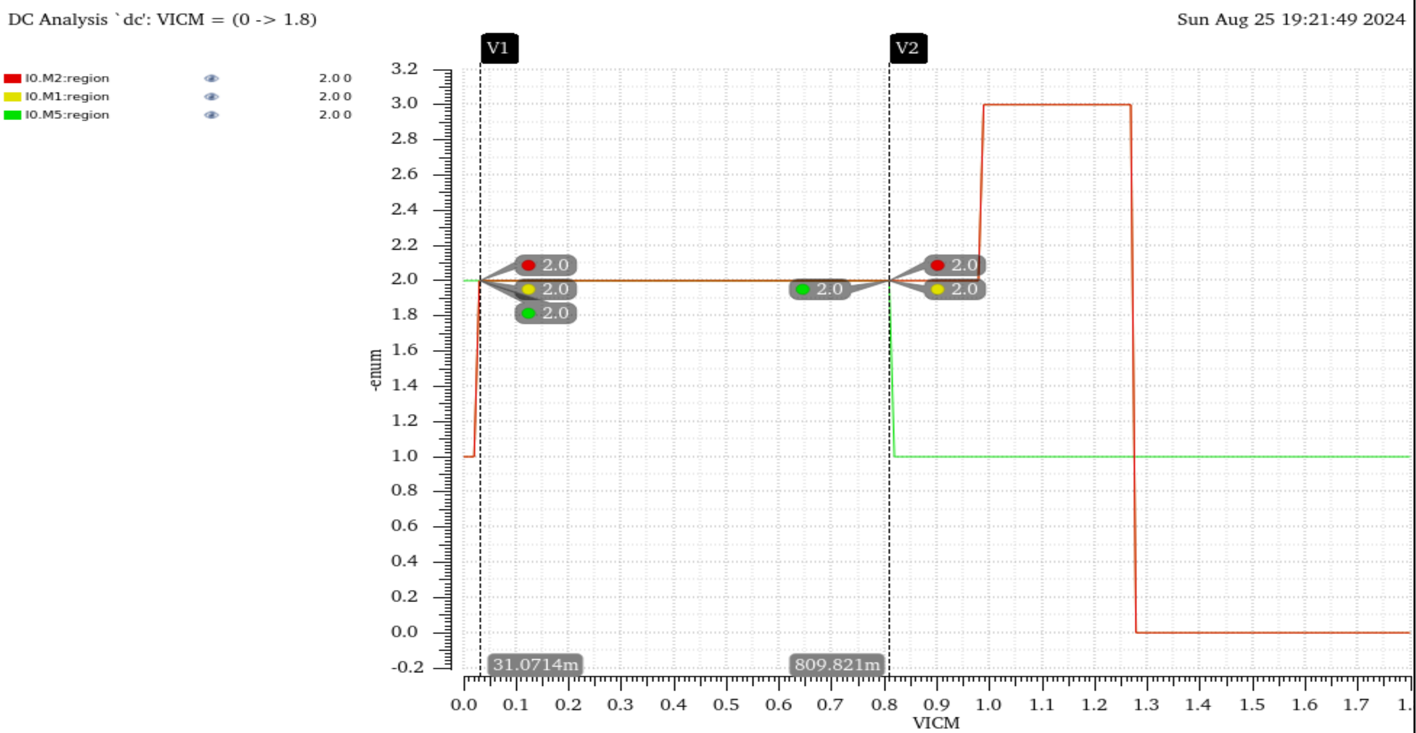
- **From the plot, what is the value of Vout at VID = 0. Compare it with the value you obtained in DC OP.**

From plot Vout = 1.059 (same value obtained in DC OP)

- **Plot VOUT vs VID.**



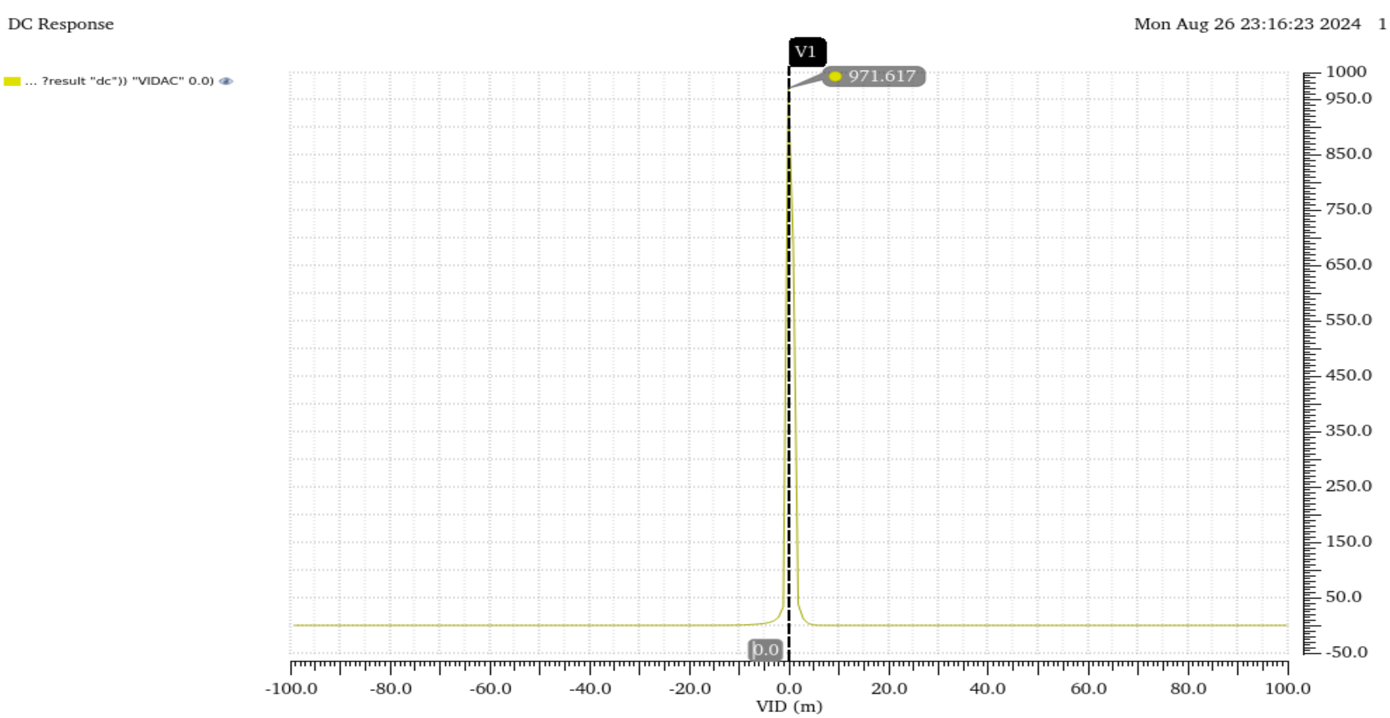
• **Plot the derivative of VOUT vs VID. Is the peak less than the value of Avd obtained from ac analysis? Why?**



smaller step curve be more smoother and slope be more accurate it will be more near to Avd

4) **CM large signal ccs (region vs VICM):**

• **Plot "region" OP parameter vs VICM for the input pair and the tail current source.**



• **Find the CM input range (CMIR). Compare with hand analysis in a table.**

Simulation : 30m:810m

Hand analysis :

Vicm max = VDD-Vdsat5-Vgs1,2 =803.6m

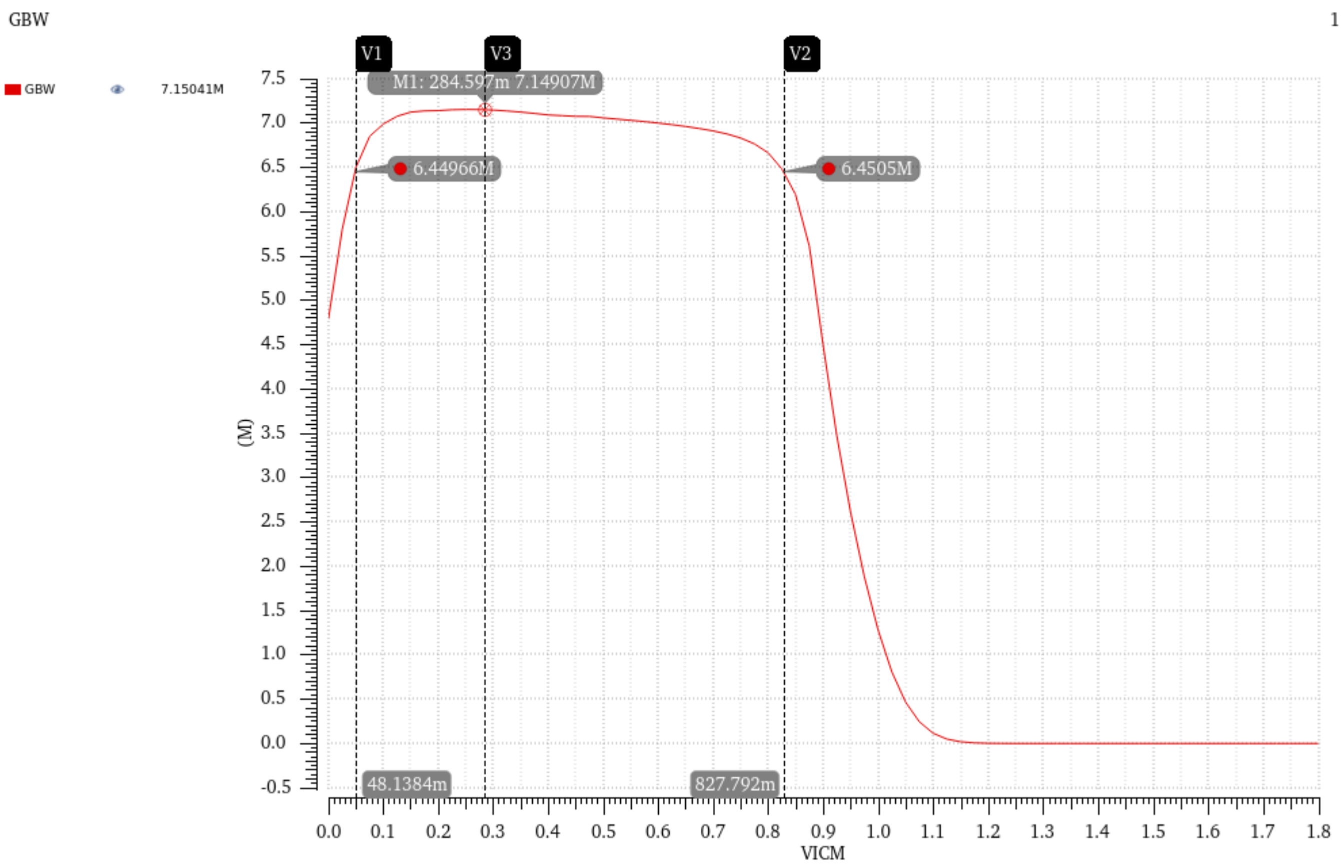
Vicm min = Vgs3-vth1=22.3m

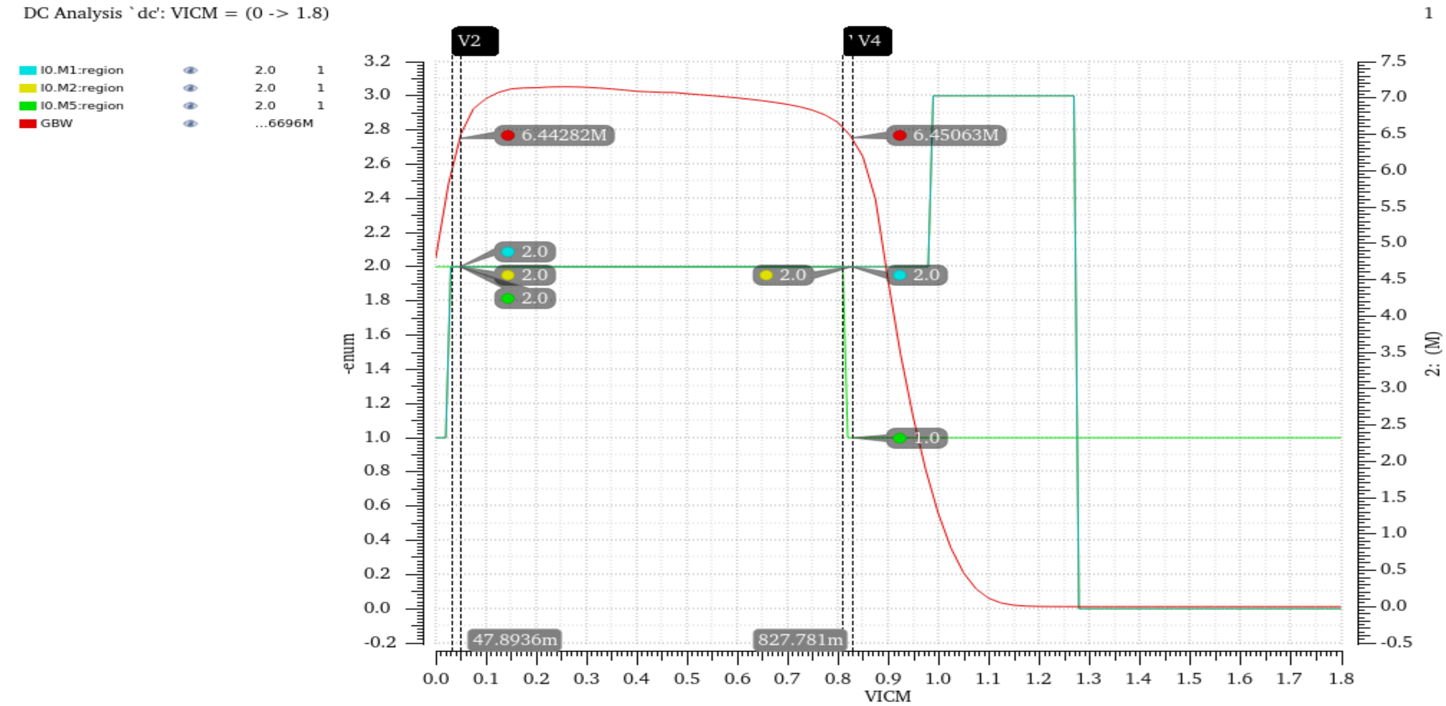
	Hand analysis	simulation
VICM	22.3m:803.6m	30m:810m

• **Note that the drawback of this method is that the "region" parameter cannot be experimentally measured in the lab.**

5) CM large signal ccs (GBW vs VICM):

• **Plot GBW vs VICM. Plot the results overlaid on the results of the previous method (region parameter).**

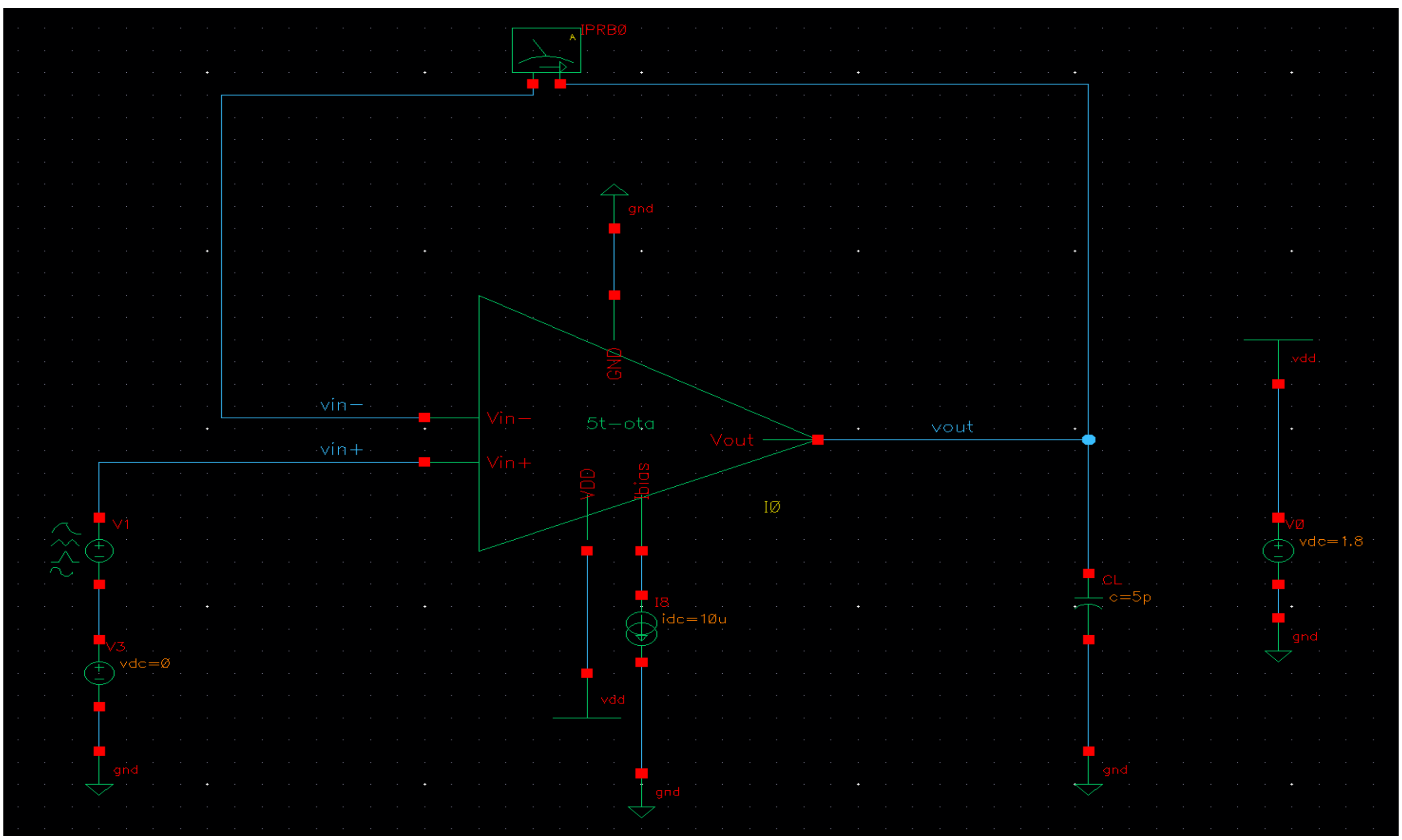




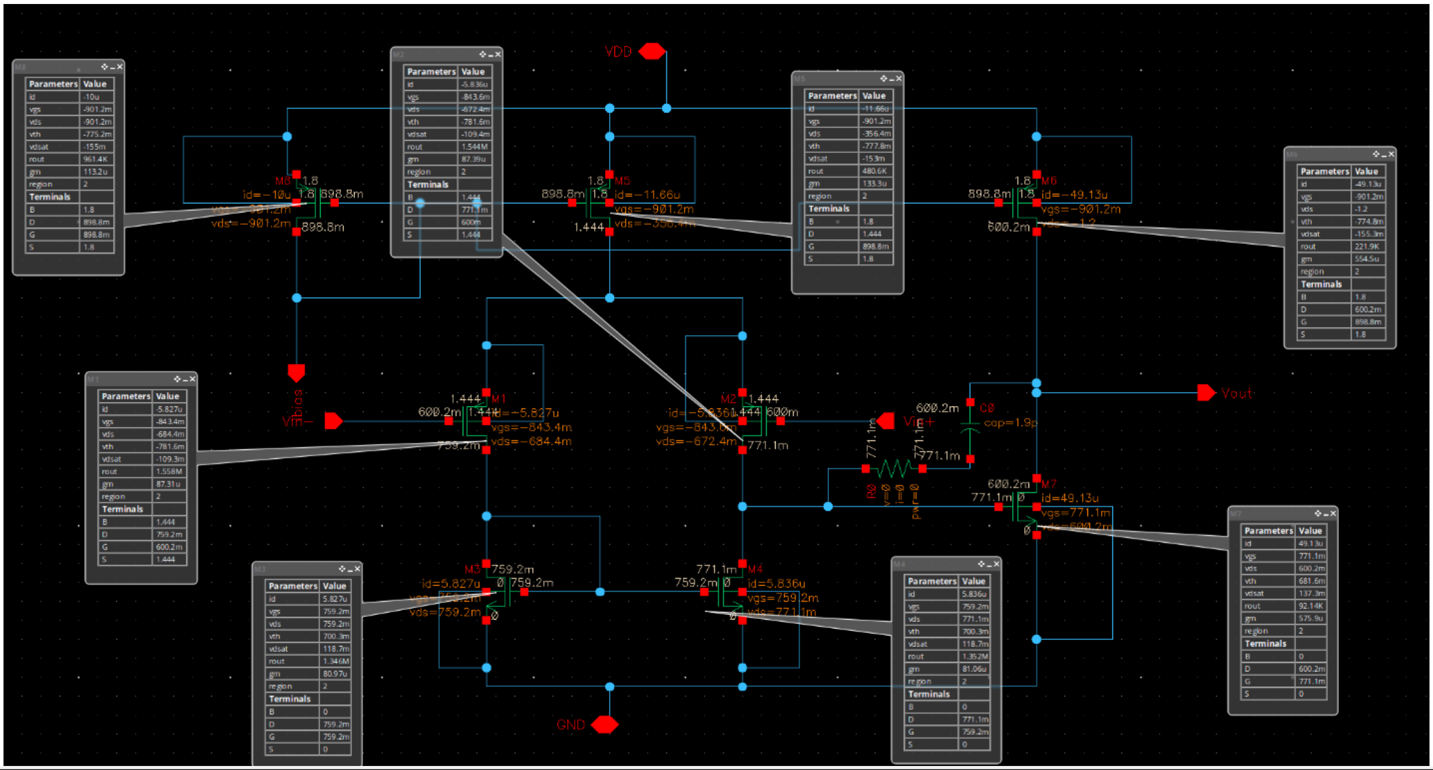
• **Annotate the CM input range. Calculate the input range as the range over which the GBW is within 90% of the max GBW, i.e., 10% reduction in GBW3**

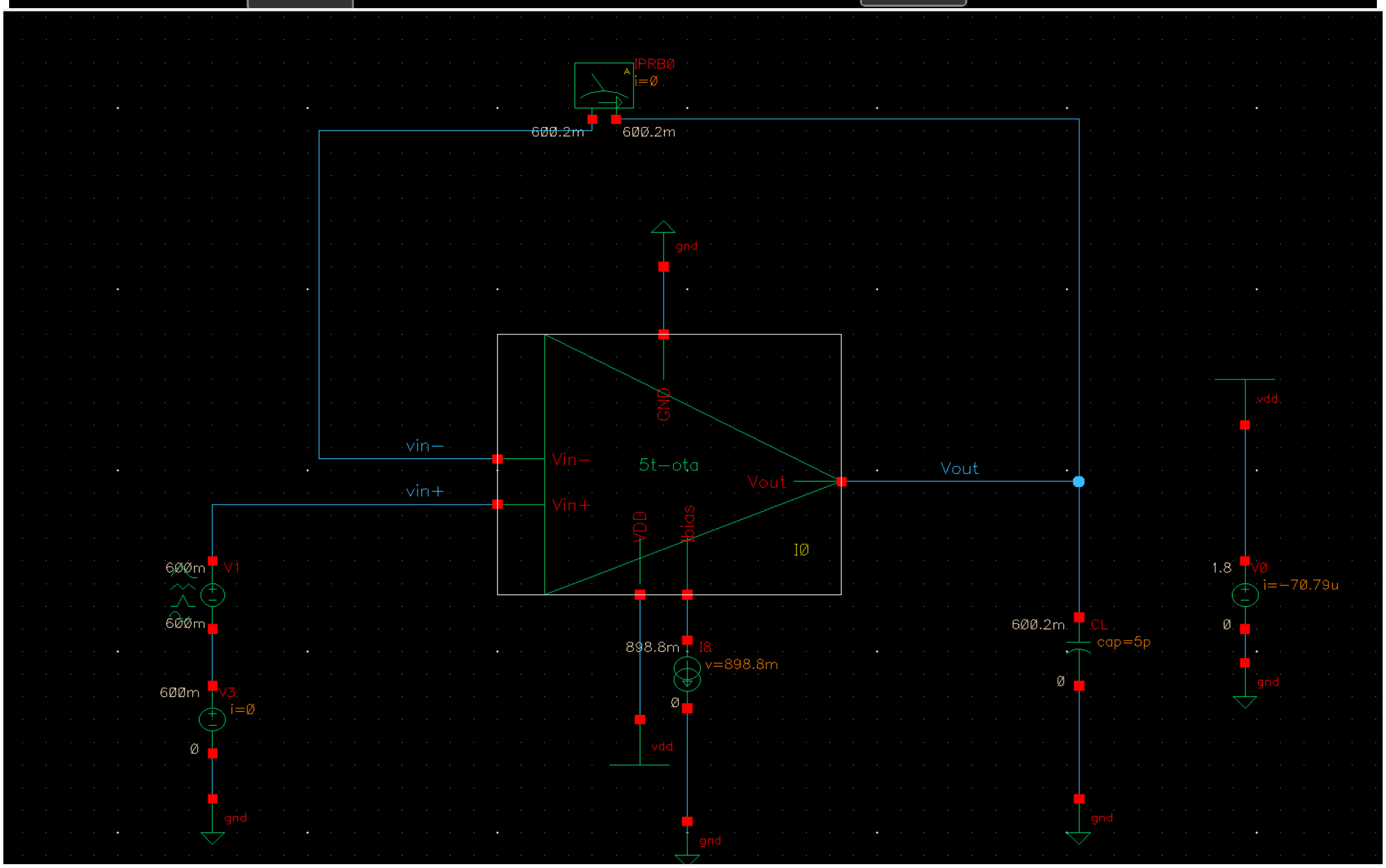
VICM range = 48m:827m

PART 4: Closed-Loop OTA Simulation



1) **Schematic of the OTA and the bias circuit with DC OP point clearly annotated in unity gain buffer configuration.**





3 If you are using NMOS input pair, body effect may cause CMIR to extend till VDD (why?). If you are using PMOS input pair, body effect may cause CMIR to extend till GND (why?).

Because in Nmos vinmax=Vth+VDD-Vgsload , Pmos vinmax= VDD-Vovtail -Vgsinput

- Use VICM = VDD/3.
- Are the DC voltages at the input terminals of the op-amp exactly equal? Why?

Vin+=600m , vin-=602m the feed back want vin+=vin- but it will happen if open loop gain infinity

- Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?

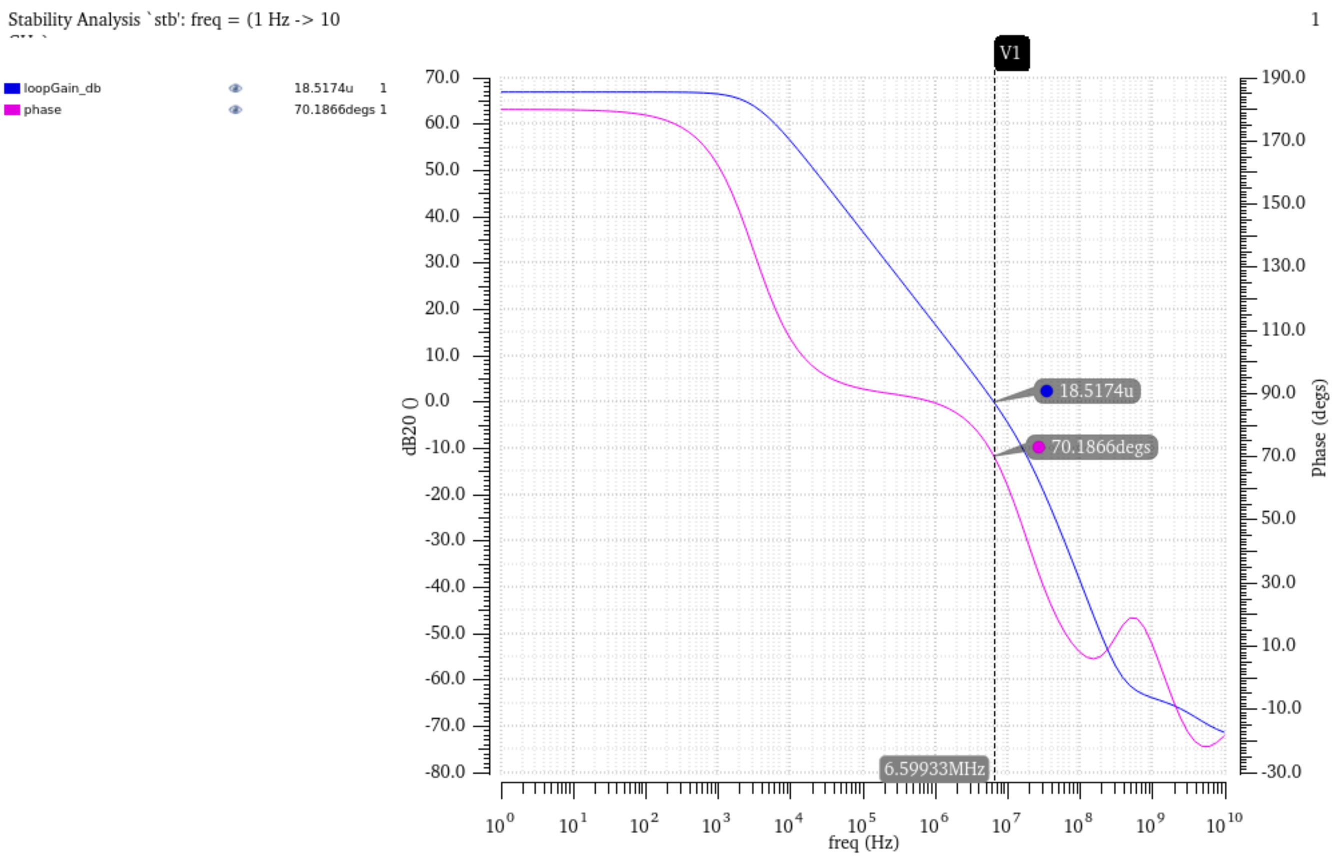
Because it now vin+ not equal vin- so circuit isnot symmetric so vout will not follow VM and I force vout with initial value not like part 3

- Is the current (and gm) in the input pair exactly equal? Why?

Not equal because vin+ and vin- not exactly equal so there is some variation in id and gm

2) Loop gain:

- **Plot loop gain in dB and phase vs frequency.**



miniproject1:closed_loop:1	phase margin	expr	getData("/phaseMargin" ?result "stb_margin")

miniproject1:closed_loop:1	phase margin	70.23

• **Compare DC gain, fu, and GBW with those obtained from open-loop simulation. Comment**

miniproject1:closed_loop:1	A0	2.351k
miniproject1:closed_loop:1	A0_db	67.42
miniproject1:closed_loop:1	BW	2.975k
miniproject1:closed_loop:1	fu	6.635M
miniproject1:closed_loop:1	GBW	6.993M

	From loop gain	From open loop
Dc gain	2.351k	2.422K
BW	2.975Khz	2.891khz
GBW	6.993Mhz	7Mhz
Fu	6.635Mhz	6.622Mhz

They are almost the same because LG=Avol * β ($\beta = 1$)=Avol

• **Report PM. Compare with hand calculations. Comment.**

miniproject1:closed_loop:1	phase margin	expr	getData("/phaseMargin" ?result "stb_margin")

miniproject1:closed_loop:1	phase margin	70.23

Hand analysis :

Wp2 = gm2/cl = 112.46Mrad

Gx= gm1/Cc = 45.97Mrad

PM=90-$\tan^{-1}\left(\frac{Gx}{wp2}\right) = 67.75$

	Hand analysis	simulation
Phase margin	67.75 deg	70.23 deg

Of course hand analysis not accurate because we ignore parasitic of M6,7 will affect in wp2

• **Compare simulation results with hand calculations in a table.**

Hand analysis:

Dc gain: $(gm1,2 * ro2\backslash\backslash ro4) * (gm7 * ro6\backslash\backslash ro7)$ =2.367k

BW: $\frac{1}{2*\pi*(ro2\backslash\backslash ro4)*(ro6\backslash\backslash ro7)*gm7*cc} = 3$Khz

GBW: gain * Bw = 7.1Mhz , Fu: fu~gbw=7.1Mhz

Wp2 = gm2/cl = 112.46Mrad , Gx= gm1/Cc = 45.97Mrad , PM=90-$\tan^{-1}\left(\frac{Gx}{wp2}\right) = 67.75$

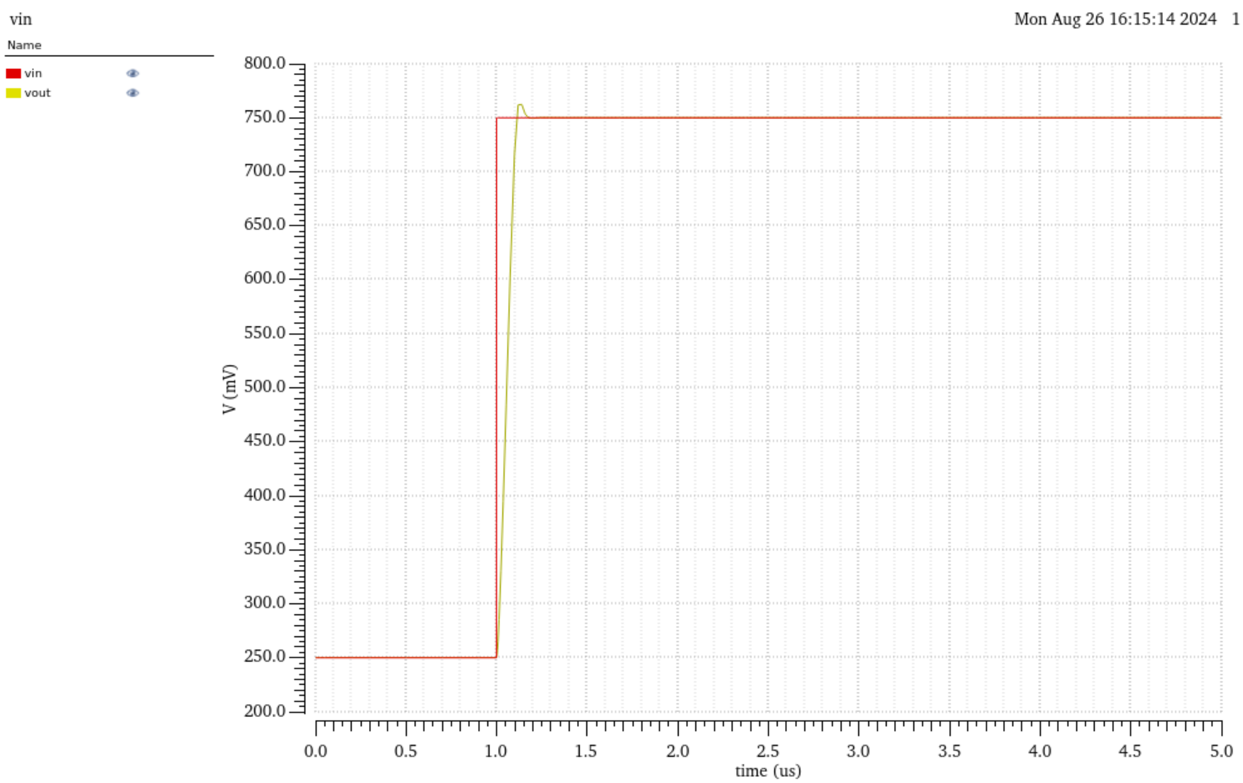
	Hand analysis	simulation
Phase margin	67.75 deg	70.23 deg
Dc gain	2.367k	2.351k
BW	3Khz	2.975Khz
GBW	7.1Mhz	6.993Mhz
Fu	7.1Mhz	6.635Mhz

3) Slew rate:

• Apply a step input with the following parameters (delay = 1us, initial value = CMIR-low + 50mV, final value = CMIR-high – 50mV, rise time = 1ns, period = 1s, width = 1s). Note that we want a single step input, which is why we selected very large period and width for the pulse.

• Run transient analysis (stop = 5us and step = 0.1ns).

• Report Vin and Vout overlaid.



• Report the slew rate.

miniproject1:closed_loop:1	slew rate	expr	slewRate(VT("/Vout") 0.25 nil 0.75 nil 10 90 nil "time")

miniproject1:closed_loop:1	slew rate	5.094M

• Compare simulation results with hand calculations in a table.

Hand analysis :

C1 = cdd2+cdd4+cgg7

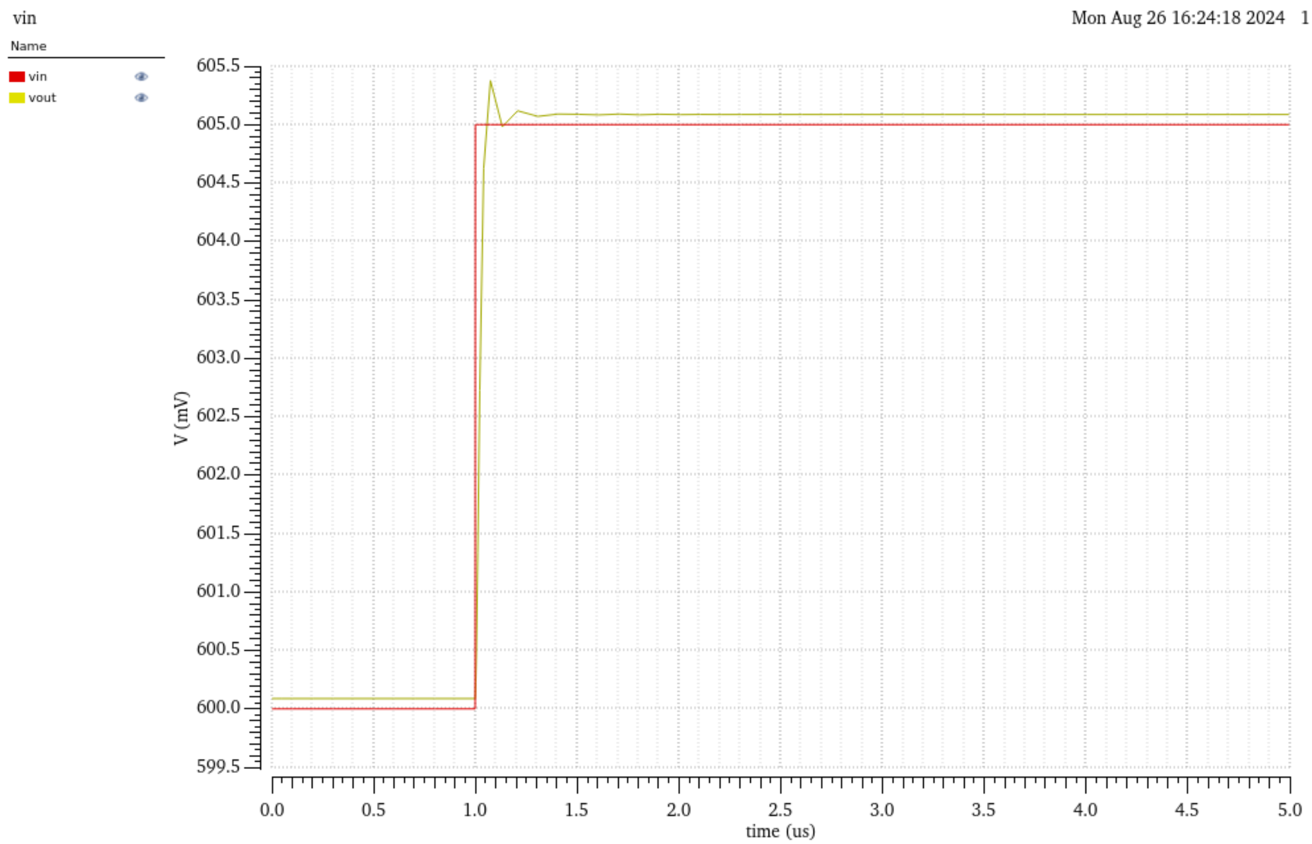
Slew rate = $\frac{ISS}{c1+Cc}$ **=6 M**

	Hand analysis	simulation
Slew rate	6M	5.094M

4) **Settling time:**

• Apply a small signal step input with the following parameters (delay = 1us, initial value = VDD/3, final value = VDD/3 + 5mV, rise time = 1ns, period = 1s, width = 1s). Note that we want a single step input, which is why we selected very large period and width for the pulse. Note that we apply a small signal pulse (5mV step) to measure the small signal settling time.

• Calculate the output rise time from simulation.



miniproject1:closed_loop:1	rise time	expr	riseTime(VT("/Vout") 0.6 nil 0.605 nil 10 90 nil "time")

miniproject1:closed_loop:1	rise time	34.27n

• Compare simulation results with hand calculations in a table .

Trise cl $= 2.2\frac{1}{Bwcl*2*\pi} = 35.8ns$

This is band width of closed loop

miniproject1:closed_loop:1	bandwidth(VF("/Vout") 3 "low")	9.761M

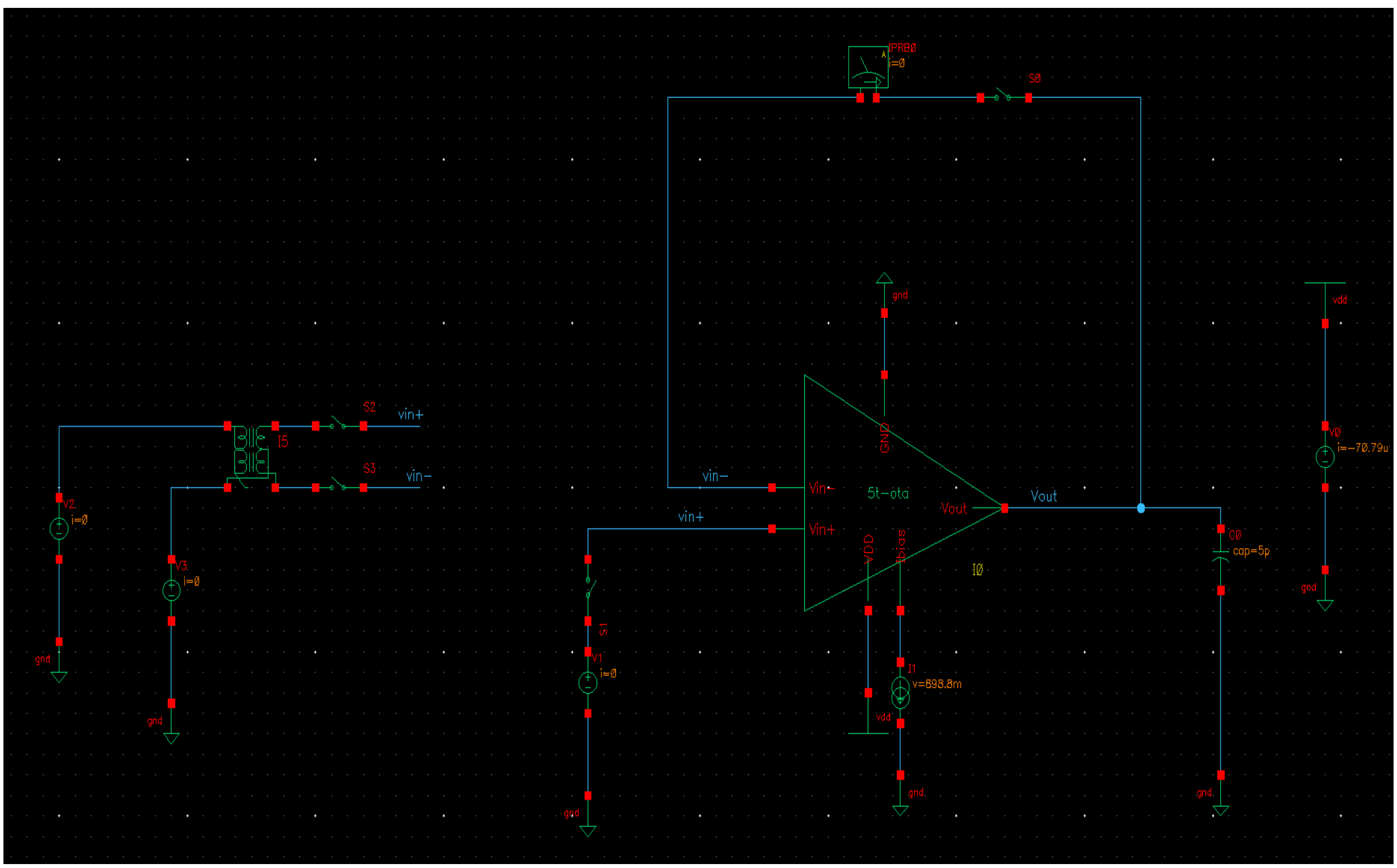
	Hand analysis	simulation
Settling time	35.8M	34.27 n

- **Do you see any ringing? Why?**

Yes,but is very very small because phase margin not equal 76 but =70.23 (not critical damped) so that wp2 is almost near

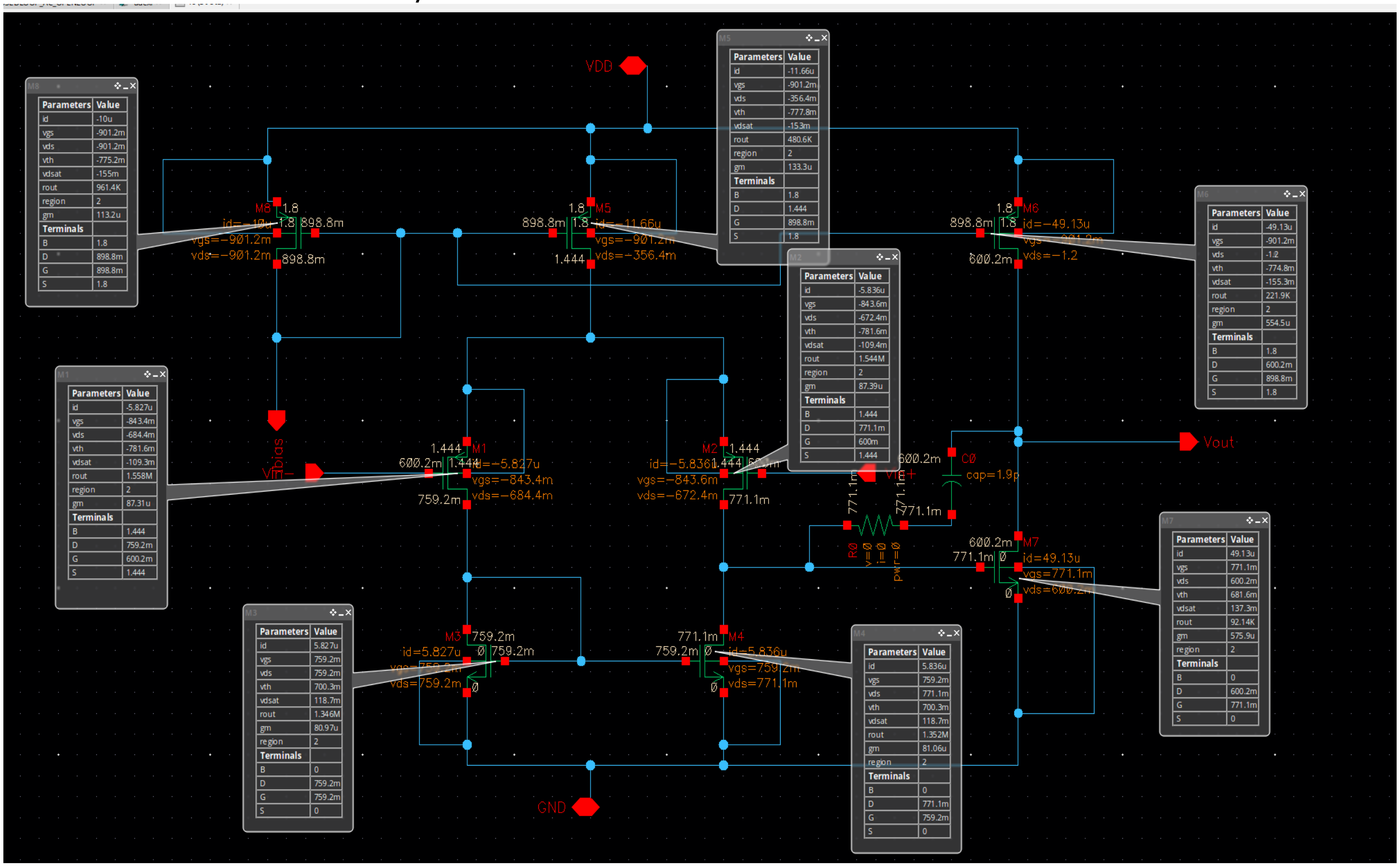
Part 5 : DC Closed Loop AC Open-Loop OTA Simulation

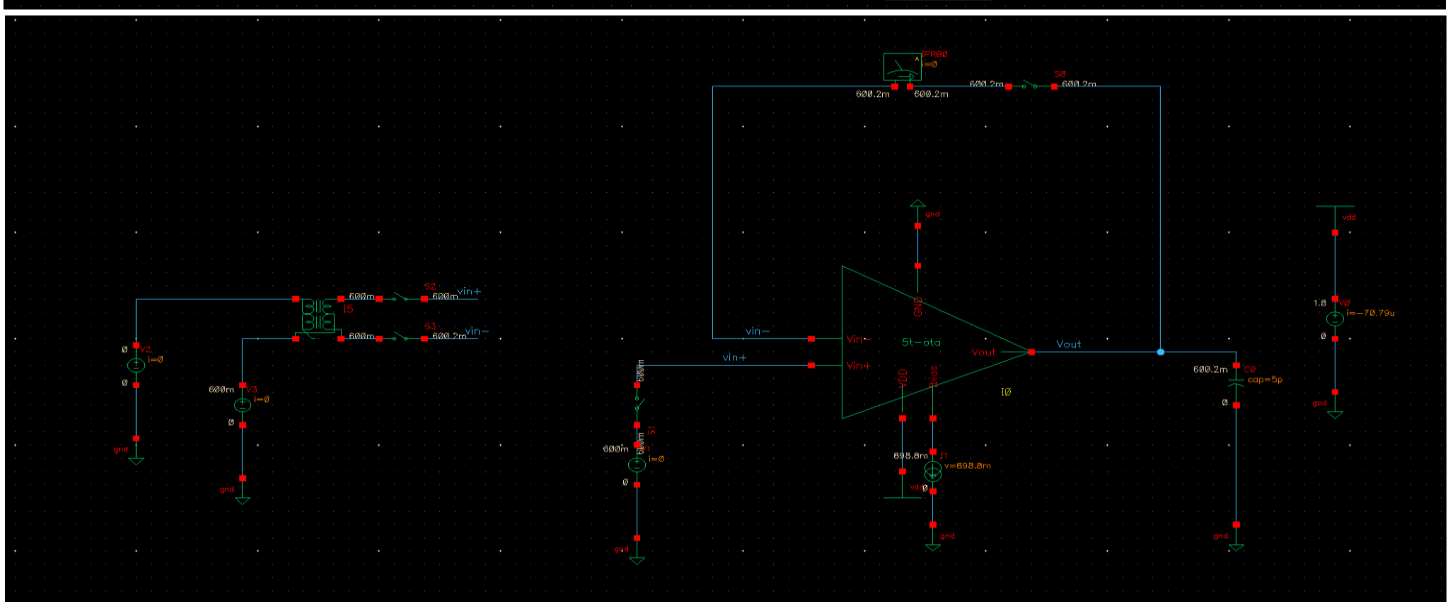
Note that there will always be residual offset voltage between the first and second stages. This offset will drive the second stage output to one of the rails; thus, the biasing of the output stage will be disturbed. In order to avoid this problem, the DC OP point must be set by feedback, e.g., by putting the amplifier in unity gain buffer configuration in DC. Use a testbench similar to the one used in the 5T OTA lab as shown below. Switches (sp1tswitch from analogLib library) are added in order to connect the feedback loop in DC and break it in AC (another option is to use resistors with different AC/DC values). Set S0 and S1 DC closed, and set S2 and S3 AC closed. The DC OP point is set by the unity gain feedback buffer connection, while the AC stimulus is set by the balun.



The simulation result will be better than expected. Why? (Hint: Using trise = 2.2□ is based on first-order model. Is second-order system faster? Because of we forced value to output not leave it in part 3 we should make zero offset voltage to get right value of output it make result b better

3) **Schematic of the OTA and bias circuit with DC node voltages clearly annotated.**
   - **Use VICM = VDD/3.**





- **Is the current (and gm) in the input pair exactly equal?**

No , because vin- =vout = 600.2m not equal vin+ so there is some variation in gm , id

- **What is DC voltage at the output of the first stage? Why?**

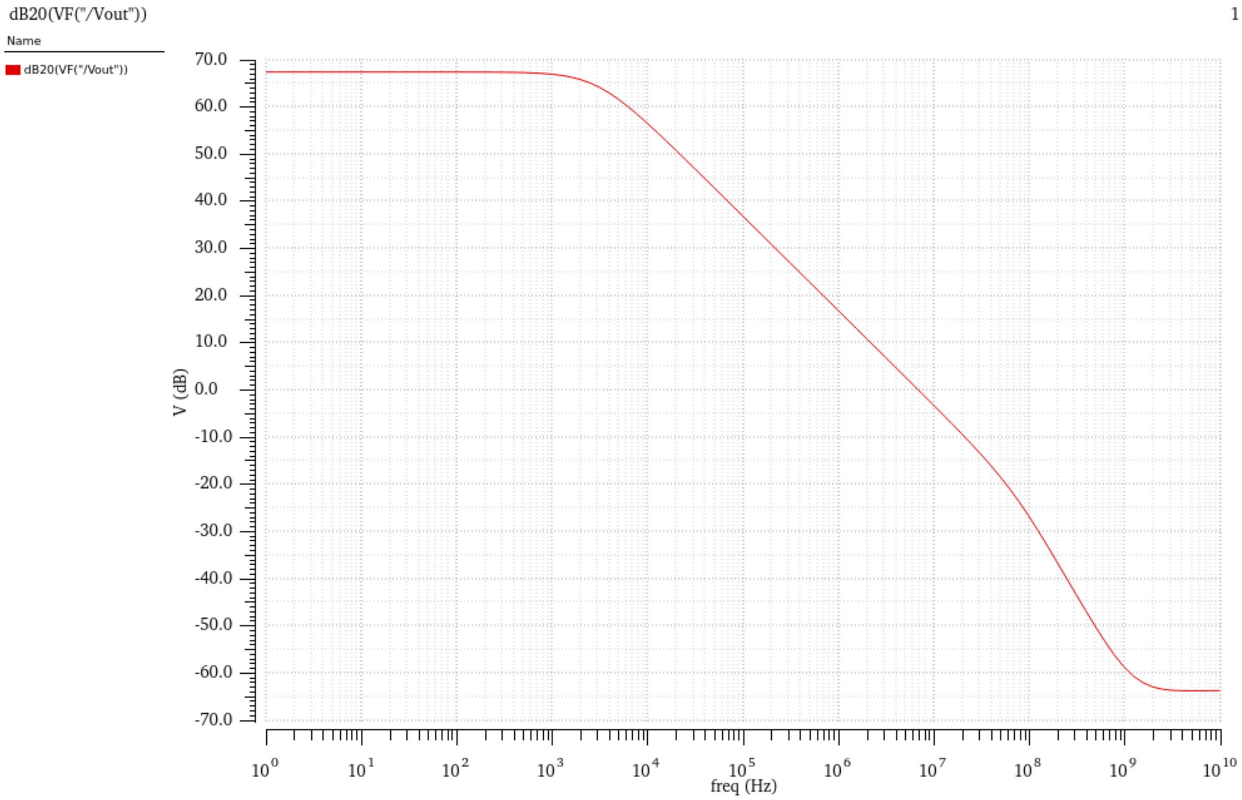
771.1m

- **What is DC voltage at the output of the second stage? Why?**

600.2m ,because vin-=vout feed back want vin-=vin+

6) **Diff small signal ccs:**

- **Plot diff gain (in dB) vs frequency.**



Test	Name	Type	Details
miniproject1:open_loop:1	A0	expr	ymax(mag(VF("/Vout")))
miniproject1:open_loop:1	A0_db	expr	dB20(ymax(mag(VF("/Vout"))))
miniproject1:open_loop:1	BW	expr	bandwidth(VF("/Vout") 3 "low")
miniproject1:open_loop:1	fu	expr	unityGainFreq(VF("/Vout"))
miniproject1:open_loop:1	GBW	expr	(A0 * BW)

miniproject1:DC_CLOSEDLOOP_AC_OPENLOOP:1	A0	2.351k
miniproject1:DC_CLOSEDLOOP_AC_OPENLOOP:1	A0_db	67.43
miniproject1:DC_CLOSEDLOOP_AC_OPENLOOP:1	BW	2.988k
miniproject1:DC_CLOSEDLOOP_AC_OPENLOOP:1	fu	7.102M
miniproject1:DC_CLOSEDLOOP_AC_OPENLOOP:1	GBW	7.026M

- **Compare simulation results with hand calculations in a table.**

Hand analysis:

Dc gain: $(gm1,2 * ro2\backslash\backslash ro4) * (gm7 * ro6\backslash\backslash ro7)$ **=2.361K**

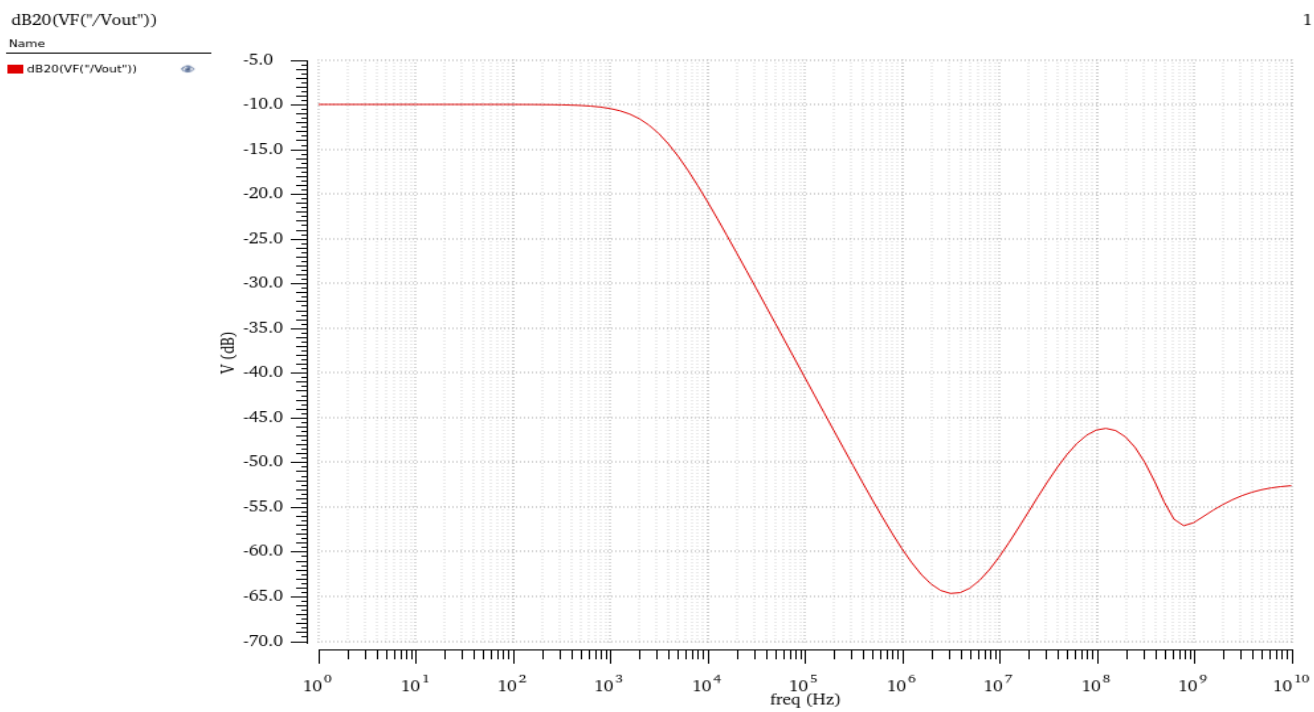
BW: $\frac{1}{2*\pi*(ro2\backslash\backslash ro4)*(ro6\backslash\backslash ro7)*gm7*cc} = 3000\text{khz}$

GBW: gain * Bw = 7.31Mhz

Fu: fu~gbw=7.31M

	Hand analysis	simulation
Dc gain	2.361K	2.351K
BW	3Khz	2.988Khz
GBW	7.083Mhz	7.026Mhz
Fu	7.083Mhz	7.102Mhz

7) **CM small signal ccs:**
   - **Plot CM gain in dB vs frequency.**



Test	Name	Type	Details
miniproject1:open_loop:1	A0	expr	ymax(mag(VF("/Vout")))
miniproject1:open_loop:1	A0_db	expr	dB20(ymax(mag(VF("/Vout"))))
miniproject1:open_loop:1	BW	expr	bandwidth(VF("/Vout") 3 "low")
miniproject1:open_loop:1	fu	expr	unityGainFreq(VF("/Vout"))
miniproject1:open_loop:1	GBW	expr	(A0 * BW)

miniproject1:DC_CLOSEDLOOP_AC_OPENLOOP:1	A0	318.6m
miniproject1:DC_CLOSEDLOOP_AC_OPENLOOP:1	A0_db	-9.934
miniproject1:DC_CLOSEDLOOP_AC_OPENLOOP:1	BW	2.988k
miniproject1:DC_CLOSEDLOOP_AC_OPENLOOP:1	fu	eval err
miniproject1:DC_CLOSEDLOOP_AC_OPENLOOP:1	GBW	952.2

- **Compare simulation results with hand calculations in a table.**

Hand analysis:

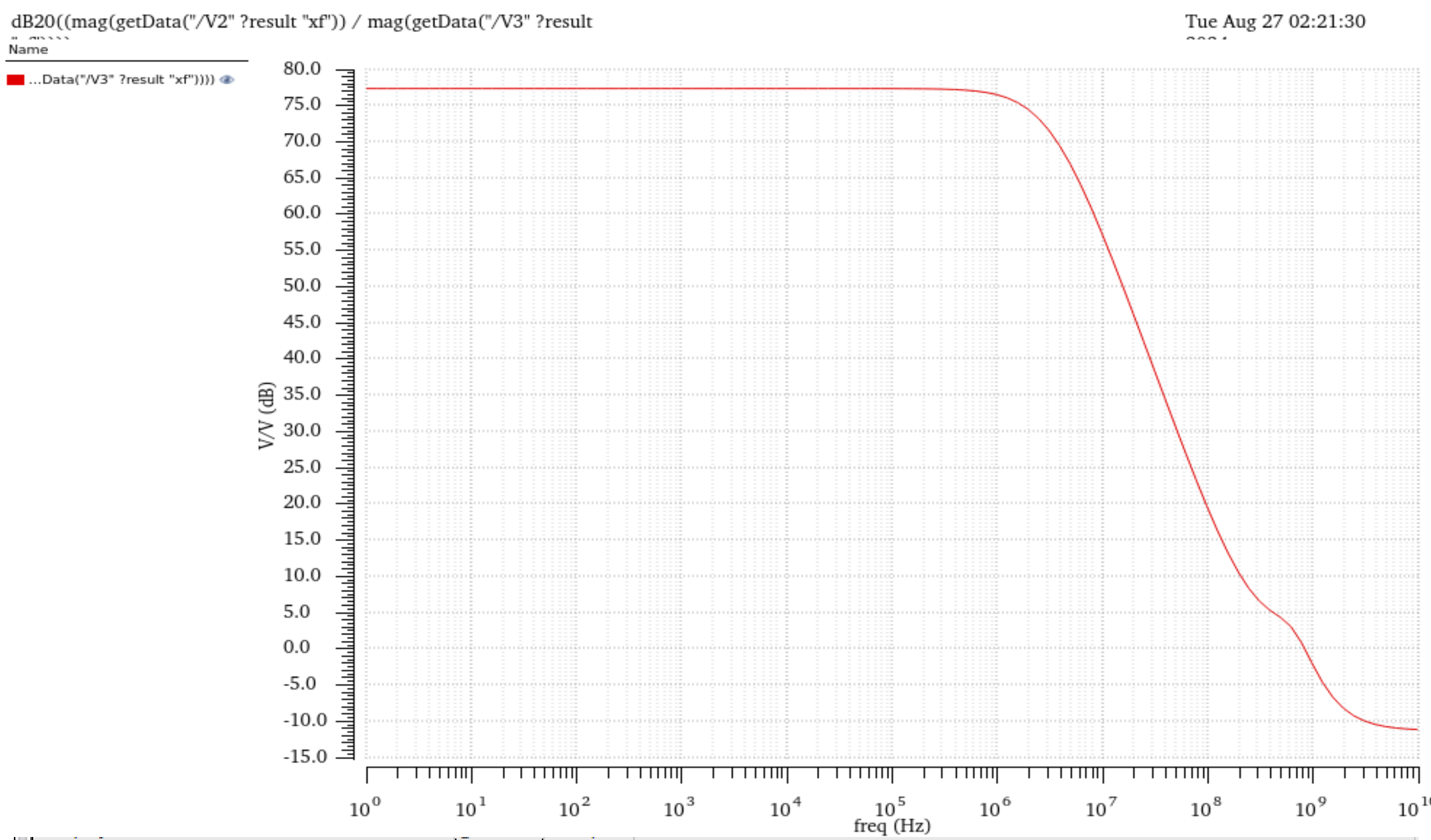
Dc gain: $\frac{1}{2*gm3,4*ro5}*(gm7*ro6\backslash\backslash ro7)=482m$, **BW:** $\frac{1}{2*\pi*(ro2\backslash\backslash ro4)*(ro6\backslash\backslash ro7)*gm7*cc}=$ **3000khz**

GBW: gain * Bw = 1.447 khz **, Fu: not applicable because gain<0db**

	Hand analysis	simulation
Dc gain	482m	318.6m
BW	3Khz	2.988Khz
GBW	1.447khz	952.2
Fu	N/A	N/A

8) CMRR:

- **Plot CMRR in dB vs frequency.**



miniproject1:DC_CLOSEDLOOP_AC_OPENLOOP:1	cmrr	expr	dB20((mag(getData("/V2" ?result "xf")) / mag(getData("/V3" ?result "xf"))))
miniproject1:DC_CLOSEDLOOP_AC_OPENLOOP:1	cmrr_dc	expr	ymax(dB20((mag(getData("/V2" ?result "xf")) / mag(getData("/V3" ?result "xf")))))

miniproject1:DC_CLOSEDLOOP_AC_OPENLOOP:1	dB20((mag(getData("/V2" ?resul...	
miniproject1:DC_CLOSEDLOOP_AC_OPENLOOP:1	ymax(dB20((mag(getData("/V2" ...	77.36

• **Compare simulation results with hand calculations in a table.**

Hand analysis:

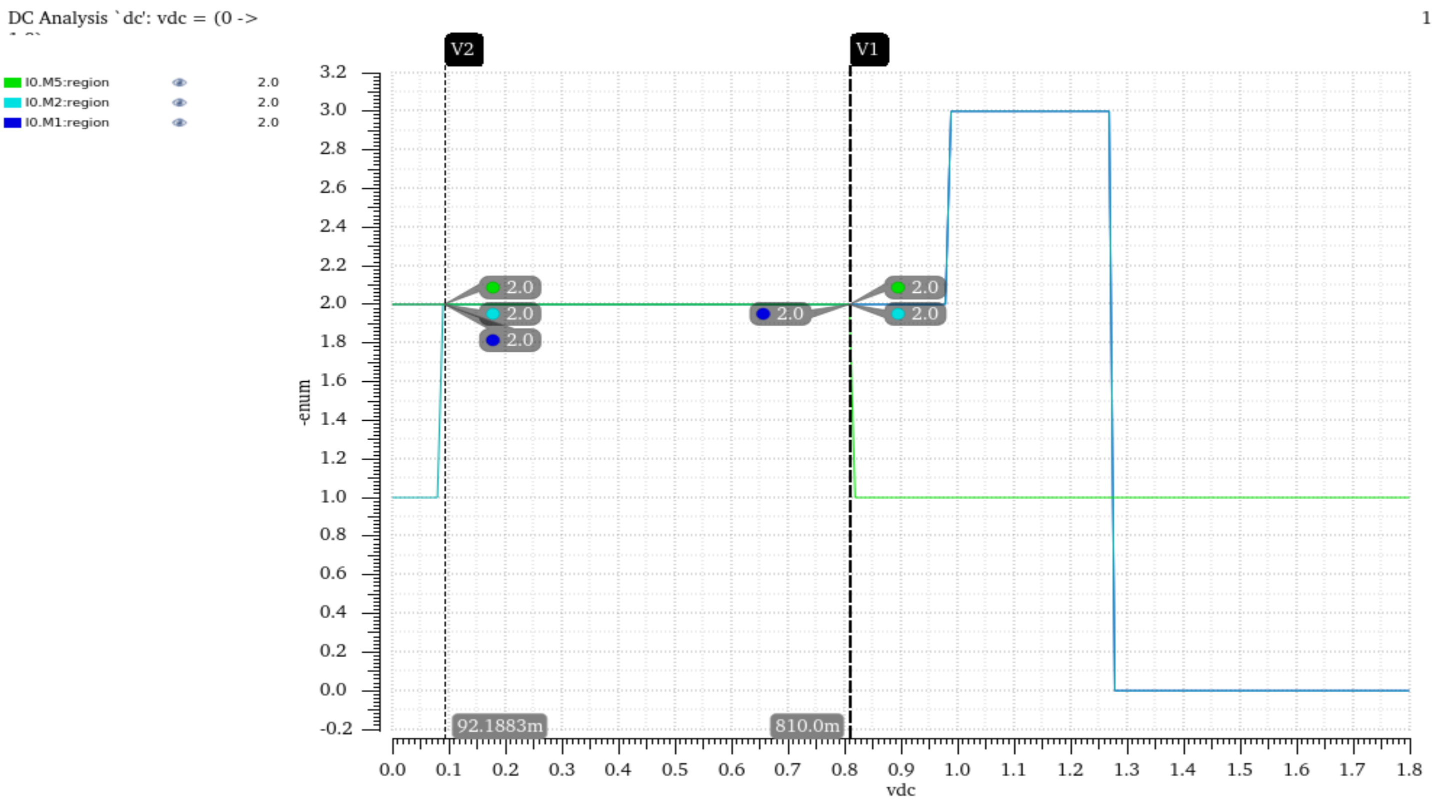
CMRR=Avd/Avcm (we get them from requirement 1, 2) = 4898=73.8db

	Hand analysis	simulation
CMRR	73.8db	77.36db

8) CM large signal ccs (region vs VICM):

I will make battery in vin+ to variable vdc and I will sweep on it

• **Plot "region" OP parameter vs VICM for the input pair and the tail current source.**



• **Find the CM input range (CMIR). Compare with hand analysis in a table.**

Simulation : 92m:810m

Hand analysis :

Vicm max = VDD-Vdsat5-Vgs1,2 =804m

Vicm min = Vgs3-vth1=22.3m

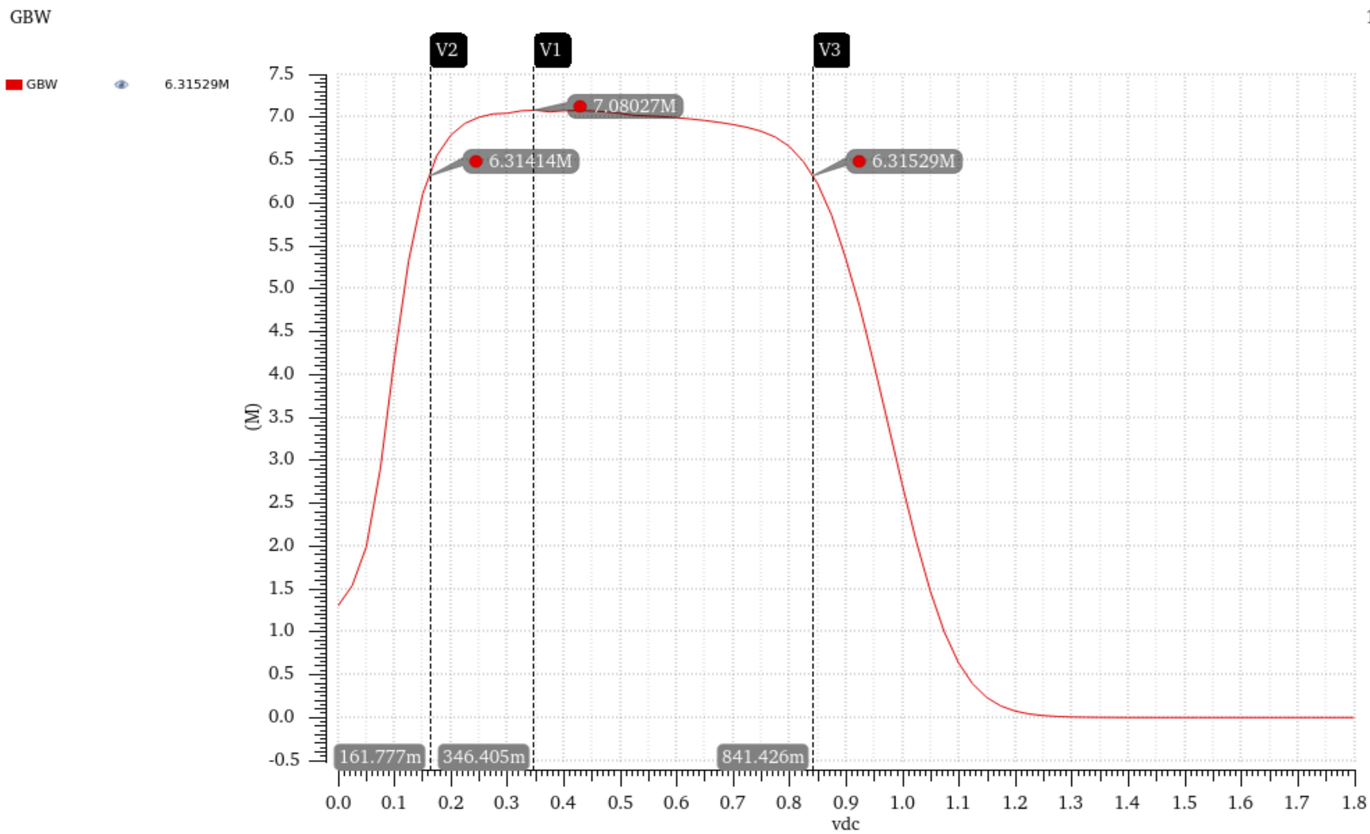
	Hand analysis	simulation
VICM	22.3m:804m	92m:810m

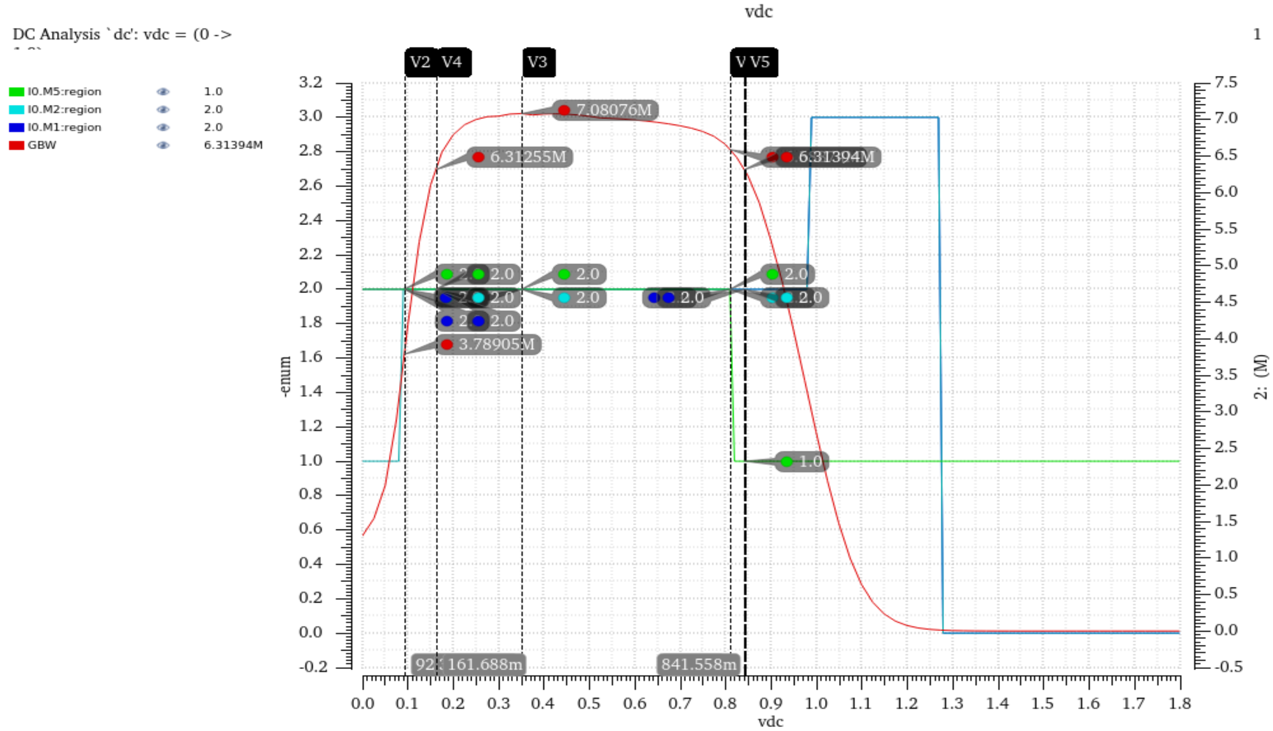
• **Note that the drawback of this method is that the "region" parameter cannot be experimentally measured in the lab.**

9) CM large signal ccs (GBW vs VICM):

I will make battery in vin+ to variable vdc and I will sweep on it

- **Plot GBW vs VICM. Plot the results overlaid on the results of the previous method (region parameter).**

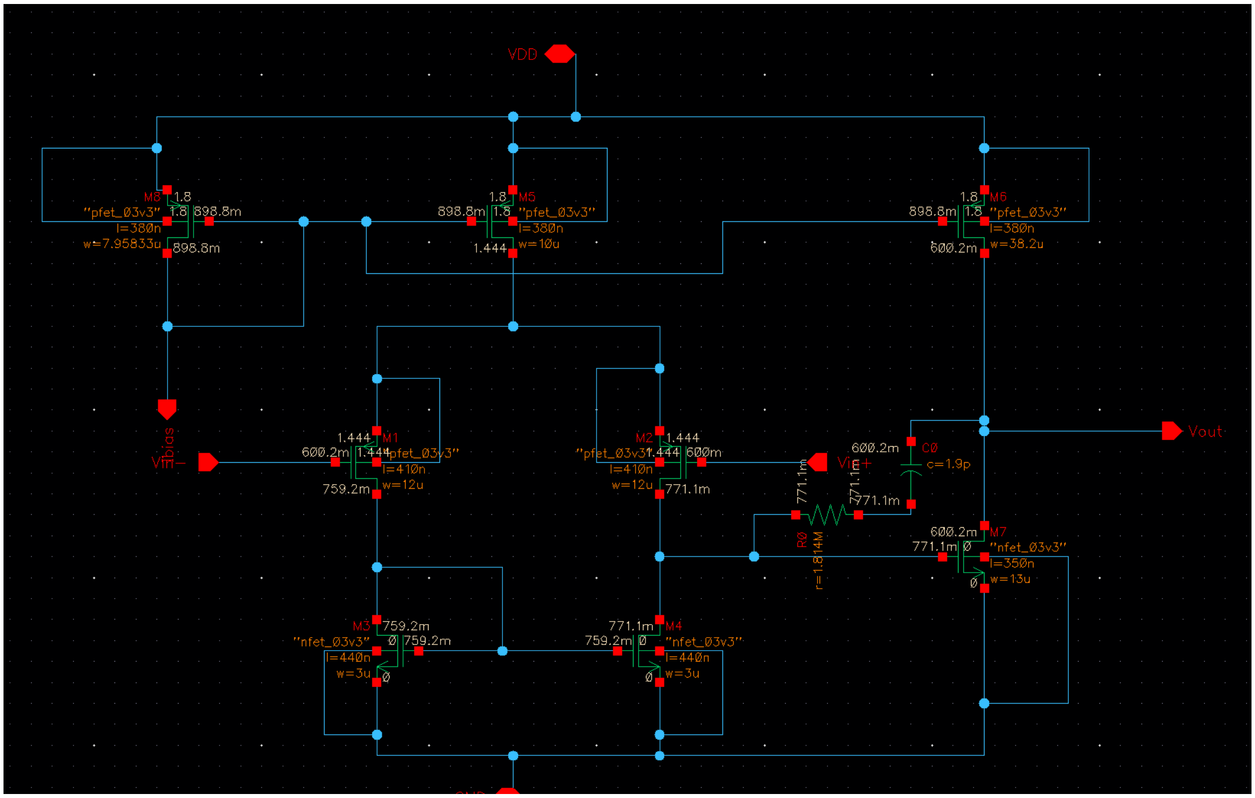




• **Annotate the CM input range. Calculate the input range as the range over which the GBW is within 90% of the max GBW, i.e., 10% reduction in GBW3**

VICM range = 160m:840m

AREA



ALL AREA OF ALL MOSFETS = 38.3 P