معماريات الحاسب
9:11
الاثنين 14/6/2021
أ.د/مصطفى مكى

Faculty of Computers & Information, Assiut University
2nd Level
Final Exam
Duration: 2 hours

1. الإسم الرباعي (بالعربي فقط) *

ماريا سامح الفونس قزمان

2. رقم الجلوس *

1620195209

3. المستوي *

- [ ] الاول
- [x] الثاني
- [ ] الثالث

- رابعة 2013
- رابعة 2014
- رابعة 2015
- رابعة 2016
- رابعة 2017

4. البرنامج *

- عام
- بايو
- هندسة

5. رقم المعمل *

- ج٠
- د٠
- اب
- اد
- اهـ
- أ٢
- ب٢
- ج٢
- د٢
- هـ٢
- أ٣
- ب٣

- ٣ج
- ٣د
- ٣هـ
- ٤أ
- ٤ب

6. رقم الكمبيوتر *

19

7. الكود (قد تمت مراجعة بيانات الطالب ورقم الجلوس) *

hLqg

8. The ALU makes use of _____ to store the intermediate results.
a) Accumulators
b) Registers
c) Heap
d) Stack
(2 Points)

- a
- b
- c
- d

9. The _____ format is usually used to store data.
   a) BCD
   b) Decimal
   c) Hexadecimal
   d) Octal
   (2 Points)

   - (•) a
   - ( ) b
   - ( ) c
   - ( ) d

10. The final addition sum of the numbers, 0110 & 0110 is _____
    a) 1101
    b) 1111
    c) 1001
    d) 1010
    (2 Points)

    - (•) a
    - ( ) b
    - ( ) c
    - ( ) d

11. Circuits that can hold their state as long as power is applied is _____
    a) Dynamic memory
    b) Static memory
    c) Register
    d) Cache
    (2 Points)

    - ( ) a
    - (•) b

c

d

12. The method of accessing the I/O devices by repeatedly checking the status flags is _____
    a) Program-controlled I/O
    b) Memory-mapped I/O
    c) I/O mapped
    d) None of the mentioned
    (2 Points)

    a

    b

    c

    d

13. VLSI stands for _____
    a) Very Large Scale Integration
    b) Very Large Stand-alone Integration
    c) Volatile Layer System Interface
    d) None of the mentioned
    (2 Points)

    a

    b

    c

    d

14. . Which registers can interact with the secondary storage?

a) MAR
b) PC
c) IR
d) R0
(2 Points)

- (●) a
- ( ) b
- ( ) c
- ( ) d

15. The time delay between two successive initiations of memory operation _____

a) Memory access time
b) Memory search time
c) Memory cycle time
d) Instruction delay
(2 Points)

- ( ) a
- ( ) b
- (●) c
- ( ) d

16. The 8-bit encoding format used to store data in a computer is _____

a) ASCII
b) EBCDIC
c) ANCI
d) USCII
(2 Points)

- ( ) a
- (●) b

- c
- d

17. Which memory device is generally made of semiconductors?
    a) RAM
    b) Hard-disk
    c) Floppy disk
    d) Cd disk
    (2 Points)

- a
- b
- c
- d

18. The control unit controls other units by generating _____
    a) Control signals
    b) Timing signals
    c) Transfer signals
    d) Command Signals
    (2 Points)

- a
- b
- c
- d

19. _____ is used to choose between incrementing the PC or performing ALU operations.
    a) Conditional codes
    b) Multiplexer
    c) Control unit
    d) None of the mentioned
    (2 Points)

- [ ] a
- [x] b
- [ ] c
- [ ] d

20. A 16 X 8 Organization of memory cells, can store up to _____
    a) 256 bits
    b) 1024 bits
    c) 512 bits
    d) 128 bits
    (2 Points)

- [ ] a
- [ ] b
- [ ] c
- [x] d

21. The special communication used in RAMBUS are _____
    a) RAMBUS channel
    b) D-link
    c) Dial-up
    d) None of the mentioned
    (2 Points)

- [x] a

- b
- c
- d

22. To reduce the memory access time we generally make use of _____
    a) Heaps
    b) Higher capacity RAM's
    c) SDRAM's
    d) Cache's
    (2 Points)

- a
- b
- c
- d

23. How can the processor ignore other interrupts when it is servicing one _____
    a) By turning off the interrupt request line
    b) By disabling the devices from sending the interrupts
    c) BY using edge-triggered request lines
    d) All of the mentioned
    (2 Points)

- a
- b
- c
- d

24. The fastest data access is provided using _____
    a) Caches
    b) DRAM's
    c) SRAM's
    d) Registers
    (2 Points)

    - [ ] a
    - [ ] b
    - [ ] c
    - [x] d

25. The multiplier is stored in _____
    a) PC Register
    b) Shift register
    c) Cache
    d) None of the mentioned
    (2 Points)

    - [ ] a
    - [x] b
    - [ ] c
    - [ ] d

26. The logic operations are implemented using _____ circuits.
    a) Bridge
    b) Logical
    c) Combinatorial
    d) Gate
    (2 Points)

    - [ ] a
    - [ ] b

- c
- d

27. The usual implementation of the carry circuit involves _____
    a) And & or gates
    b) XOR
    c) NAND
    d) XNOR
    (2 Points)

- a
- b
- c
- d

28. _____ is generally used to increase the apparent size of physical memory.
    a) Secondary memory
    b) Virtual memory
    c) Hard-disk
    d) Disks
    (2 Points)

- a
- b
- c
- d

29. DDR stands for _____
a) Data Direction Register
b) Data Decoding Register
c) Data Decoding Rate
d) None of the mentioned
(2 Points)

- (●) a
- ( ) b
- ( ) c
- ( ) d

30. The signal sent to the device from the processor to the device after receiving an interrupt is _____
a) Interrupt-acknowledge
b) Return signal
c) Service signal
d) Permission signal
(2 Points)

- (●) a
- ( ) b
- ( ) c
- ( ) d

31. The registers, ALU and the interconnection between them are collectively called as _____
a) process route
b) information trail
c) information path
d) data path
(2 Points)

- ( ) a

- b
- c
- d

32. The advantage of CMOS SRAM over the transistor one's is _____
    a) Low cost
    b) High efficiency
    c) High durability
    d) Low power consumption
    (2 Points)

- a
- b
- c
- d

33. The decoded instruction is stored in _____
    a) IR
    b) PC
    c) Registers
    d) MDR
    (2 Points)

- a
- b
- c
- d

34. The interrupt-request line is a part of the _____
    a) Data line
    b) Control line
    c) Address line
    d) None of the mentioned
    (2 Points)

    a

    b

    c

    d

35. MFC stands for _____
    a) Memory Format Caches
    b) Memory Function Complete
    c) Memory Find Command
    d) Mass Format Command
    (2 Points)

    a

    b

    c

    d

36. The registers, ALU and the interconnection between them are collectively called as _____
    a) process route
    b) information trail
    c) information path
    d) data path
    (2 Points)

    a

- b
- c
- d

37. The Input devices can send information to the processor.
    a) When the SIN status flag is set
    b) When the data arrives regardless of the SIN flag
    c) Neither of the cases
    d) Either of the cases
    (2 Points)

- a
- b
- c
- d

38. A source program is usually in _____
    a) Assembly language
    b) Machine level language
    c) High-level language
    d) Natural language
    (2 Points)

- a
- b
- c
- d

39. _____ is used to store data in registers.
a) D flip flop
b) JK flip flop
c) RS flip flop
d) None of the mentioned
(2 Points)

- (●) a
- ( ) b
- ( ) c
- ( ) d

40. A single Interrupt line can be used to service n different devices.
a) True
b) False
(2 Points)

- (●) a
- ( ) b

41. The usual BUS structure used to connect the I/O devices is _____
a) Star BUS structure
b) Multiple BUS structure
c) Single BUS structure
d) Node to Node BUS structure
(2 Points)

- ( ) a
- ( ) b
- (●) c
- ( ) d

42. The I/O interface required to connect the I/O device to the bus consists of _____
a) Address decoder and registers
b) Control circuits
c) Address decoder, registers and Control circuits
d) Only Control circuits
(2 Points)

- a
- b
- c
- d

43. _____ are numbers and encoded characters, generally used as operands.
a) Input
b) Data
c) Information
d) Stored Values
(2 Points)

- a
- b
- c
- d

44. To overcome the lag in the operating speeds of the I/O device and the processor we use _____
a) BUffer spaces
b) Status flags
c) Interrupt signals
d) Exceptions
(2 Points)

- a

b

c

d

45. _____ bus structure is usually used to connect I/O devices.
a) Single bus
b) Multiple bus
c) Star bus
d) Rambus
(2 Points)

a

b

c

d

46. Which memory device is generally made of semiconductors?
a) RAM
b) Hard-disk
c) Floppy disk
d) Cd disk
(2 Points)

a

b

c

d

47. CSA stands for?
a) Computer Speed Addition
b) Carry Save Addition
c) Computer Service Architecture
d) None of the mentioned
(2 Points)

- (●) a
- ( ) b
- ( ) c
- ( ) d

48. The product of 1101 & 1011 is _____
a) 10001111
b) 10101010
c) 11110000
d) 11001100
(2 Points)

- (●) a
- ( ) b
- ( ) c
- ( ) d

49. A source program is usually in _____
a) Assembly language
b) Machine level language
c) High-level language
d) Natural language
(2 Points)

- ( ) a
- ( ) b

- [x] c
- [ ] d

50. The internal components of the processor are connected by _____
    a) Processor intra-connectivity circuitry
    b) Processor bus
    c) Memory bus
    d) Rambus
    (2 Points)

- [ ] a
- [x] b
- [ ] c
- [ ] d

51. Interrupts form an important part of _____ systems.
    a) Batch processing
    b) Multitasking
    c) Real-time processing
    d) Multi-user
    (2 Points)

- [ ] a
- [ ] b
- [x] c
- [ ] d

52. In full adders the sum circuit is implemented using _____
    a) And & or gates
    b) NAND gate
    c) XOR
    d) XNOR
    (2 Points)

- [ ] a
- [ ] b
- [x] c
- [ ] d

53. _____ is the bottleneck, when it comes computer performance.
    a) Memory access time
    b) Memory cycle time
    c) Delay
    d) Latency
    (2 Points)

- [ ] a
- [x] b
- [ ] c
- [ ] d

54. The small extremely fast, RAM's are called as _____
    a) Cache
    b) Heaps
    c) Accumulators
    d) Stacks
    (2 Points)

- [x] a
- [ ] b

c

d

55. The method of synchronizing the processor with the I/O device in which the device sends a signal when it is ready is?
    a) Exceptions
    b) Signal handling
    c) Interrupts
    d) DMA
    (2 Points)

a

b

c

d

56. During the execution of a program which gets initialized first?
    a) MDR
    b) IR
    c) PC
    d) MAR
    (2 Points)

a

b

c

d

57. Which of the register/s of the processor is/are connected to Memory Bus?

a) PC
b) MAR
c) IR
d) Both PC and MAR
(2 Points)

- [ ] a
- [x] b
- [ ] c
- [ ] d