



دوائر رقمية

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الثلاثاء 8/6/2021

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Faculty of Computers & Information, Assiut University

1st Level

Final Exam

Duration: 2 hours

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\* الإسم الرباعي (بالعربي فقط)

نرمين محب خير عوض الله

2

\* رقم الجلوس

162020677

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\* المستوى

- ☒ الاول
- ☐ الثاني
- ☐ الثالث
- ☐ رابعة 2013
- ☐ رابعة 2014
- ☐ رابعة 2015
- ☐ رابعة 2016
- ☐ رابعة 2017

4

\* البرنامج

- ☒ عام
- ☐ بايو
- ☐ هندسة

5

\* رقم المعمل

- ☐ ج•
- ☐ د•
- ☐

- ☐ ا ب
- ☐ ا د
- ☐ ا هـ
- ☐ أ ٢
- ☐ ب ٢
- ☐ ج ٢
- ☐ د ٢
- ☐ هـ ٢
- ☐ أ ٣
- ☐ ب ٣
- ☒ ج ٣
- ☐ د ٣
- ☐ هـ ٣
- ☐ أ ٤
- ☐ ب ٤

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\* رقم الكمبيوتر

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\* الكود (قد تمت مراجعة بيانات الطالب ورقم الجلوس)

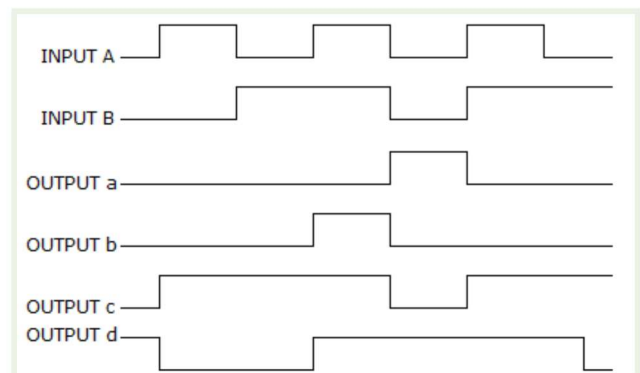
8

If a Boolean expression has four variables, then the truth table has \_\_\_\_\_ values.

(4 Points)

- ☐ 4
- ☐ 8
- ☒ 16
- ☐ 2

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For a two-input XNOR gate, with the input waveforms as shown below, which output waveform is correct?

(4 Points)

- ☒ d
- ☐ a
- ☐ c
- ☐ b

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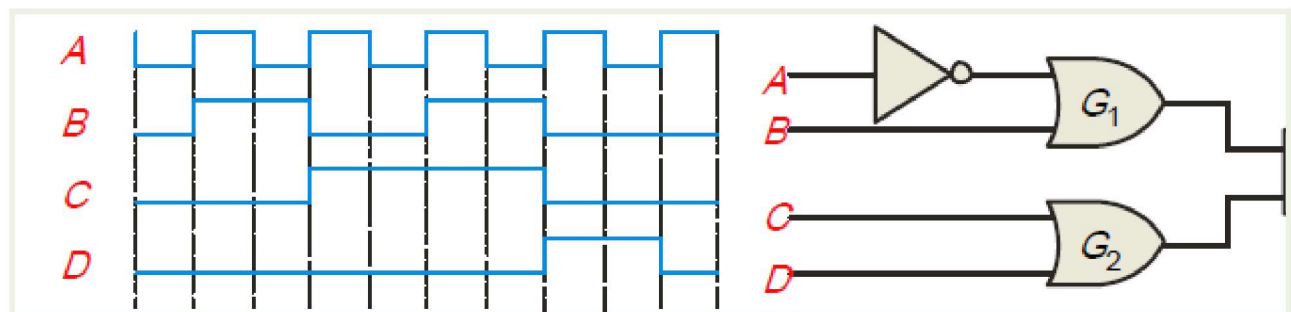
The number of full and half adders are required to add 16-bit number is

(4 Points)

- ☐ 8 half adders, 8 full adders
- ☒ 1 half adders, 15 full adders
- ☐ 16 half adders, 0 full adders
- ☐ 4 half adders, 12 full adders

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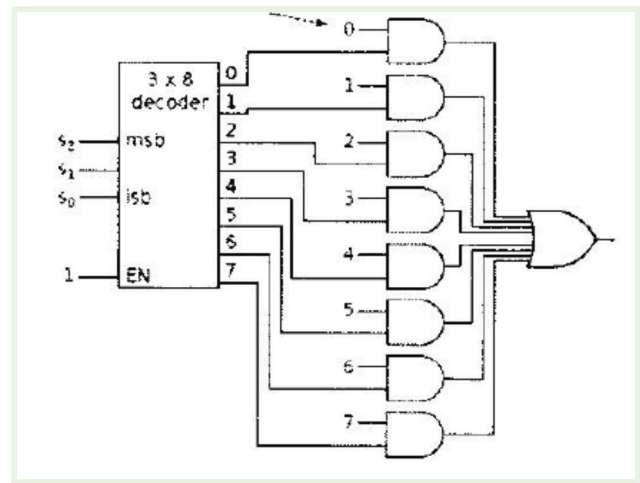
During the first three intervals for the pulsed circuit shown, the output of  
(4 Points)



- ☐ G1 is LOW and G2 is LOW
- ☐ G1 is LOW and G2 is HIGH
- ☒ G1 is HIGH and G2 is LOW
- ☐ G1 is HIGH and G2 is KIGH

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The logic circuit shown is the implementation of  
(4 Points)



- ☐ 3x8 decoder with enable
- ☒ 3x8 decoder with enable and basic logic gates
- ☐ eight-input mux using a decoder and logic gates
- ☐ None of the previous

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NAND and NOR gates are called  
(4 Points)

- ☐ high level logic gates
- ☐ unilateral gates
- ☒ universal gates
- ☐ bidirectional gates

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The four-variable K-map has \_\_\_\_ cells.  
(4 Points)

- ☐ 4

☐ 8

☒ 16

☐ 2

15

To minimize a Boolean expression using K-maps, it has to be in \_\_\_\_ form.  
(4 Points)

☐ binary

☐ decimal

☐ octal

☒ SOP

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The gate allows the output to be high, low or offers high output impedance is  
(4 Points)

☒ tri-state logic

☐ MUX

☐ NOR

☐ NAND

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The maximum number of inputs of several similar logic gates that any one gate output can drive is called  
(4 Points)

- ☐ fan-out
- ☐ noise margin
- ☐ noise immunity
- ☒ fan-in

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All logic operations can be obtained by means of  
(4 Points)

- ☐ AND and NAND operations
- ☐ OR and NOR operations
- ☐ OR and NOT operations
- ☒ NAND and NOR operations

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What is the minimum number of two-input NAND gates used to perform the function of two input OR gate ?  
(4 Points)

- ☐ 1
- ☐ 2
- ☒ 3
- ☐ 4



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Simplifying the following expression will give  
 $F = A \cdot C \cdot E + A \cdot C \cdot D' + A \cdot C \cdot E' + A \cdot B \cdot D' \cdot E + B \cdot C' \cdot E$   
(4 Points)

- ☐  $A \cdot C + B' \cdot C' \cdot E + A \cdot C \cdot D'$
- ☐  $A \cdot C + B \cdot C' \cdot E$
- ☐  $A \cdot C \cdot E + A \cdot C \cdot D'$
- ☒ None of the previous

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The multiplexer is an example of what type of logic circuit  
(4 Points)

- ☐ Sequential
- ☒ Combinational
- ☐ Moore machine
- ☐ Analog

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A movement of data from right (least significant bit) to left (most significant bit) is what type of shift:  
(4 Points)

- ☒ Right
- ☐ Lift
- ☐ Parallel

- ☐ Finite state machine

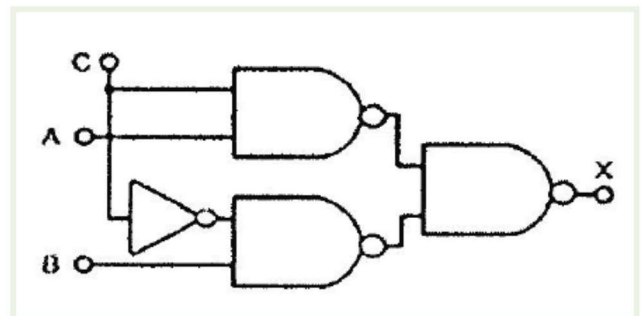
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The time interval between the application of an input pulse to a logic gate and the occurrence of the resultant output pulse is called \_\_\_\_\_.

(4 Points)

- ☐ Delay time
- ☐ turn-on time
- ☐ transition time
- ☒ propagation delay

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What type of a combinational circuit illustrated in the figure shown:  
(4 Points)

- ☐ Full Adder
- ☐ Equality Comparator
- ☒ Multiplexer
- ☐ DeMultiplexer

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De Morgan's second theorem states that the complement of a sum of variables is equal to the \_\_\_\_ of the complements of the variables.

(4 Points)

- ☐ complement
- ☐ complement sum
- ☒ product
- ☐ sum

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The complement of the following function in the simplest form is:

$$F = AB' + C + (A' + B)C' + (AB' + C)(A + B')C$$

(4 Points)

- ☐ 1
- ☒ 0
- ☐  $AB' + C + A' + B$
- ☐ None of the previous

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Negative numbers cannot be represented in:

(4 Points)

- ☐ Sign Magnitude
- ☐ 1's Complement
- ☐ Twos Complement

☒ None of the previous

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If P is a logical or Boolean variable such that P can take values '0' or '1', then  $P + P$  is equal  
(4 Points)

☐ 0

☐  $2P$

☐ 1

☒ P

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Simplifying the following expression will give  
 $A'(A+B) + (B+AA)(A+B')$   
(4 Points)

☐  $A \cdot B + A' \cdot B'$

☐  $A' + B'$

☒  $A+B$

☐ None of the previous

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Simplifying the following expression will give  
 $G = A \cdot B \cdot C \cdot D + A' \cdot E \cdot F + B' \cdot E \cdot F + C \cdot D \cdot E \cdot F$   
(4 Points)

☒  $A \cdot B \cdot C \cdot D + A' \cdot E \cdot F + B' \cdot E \cdot F$

- ☐  $A' \cdot E \cdot F + B' \cdot E \cdot F + C \cdot D \cdot E \cdot F$
- ☐  $A \cdot B \cdot C \cdot D + A' \cdot E \cdot F + B' \cdot D \cdot F$
- ☐ None of the previous

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A demultiplexer has  
(4 Points)

- ☒ One data input and a number of selection inputs, and they have several outputs.
- ☐ One input and one output
- ☐ Several inputs and several outputs
- ☐ Several inputs and one output

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A combinational logic circuit which sends a single data source to two or more separate  
(4 Points)

- ☐ Decoder
- ☐ Multiplexer
- ☐ Encoder
- ☒ Demultiplexer

