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Design and simulation of Two stage Miller OTA

Learning Objectives:

- Learn how to generate and use gm/ID design curves.
- Learn how to design a two-stage Miller OTA achieving given specifications.
- Learn how to simulate the open-loop characteristics of the two-stage Miller OTA.
- Learn how to simulate the closed-loop characteristics of the two-stage Miller OTA.

Contents

Analysis of Two stage OTA Miller :

Diff. Small signal Analysis:

$$A_{Vd} = [gm_{1,2} * (r_{o1}||r_{o2})] * [(gm_6 * (r_{o6}||r_{o7}))]$$

CM small signal Analysis:

$$CMRR = \frac{A_{VdSystem}}{A_{VcmSystem}} = \frac{[gm_{1,2} * (r_{o1}||r_{o2})] * [(gm_6 * (r_{o6}||r_{o7}))]}{[[2 * gm_{34} * R_{ss}]]^{-1} * [(gm_6 * (r_{o6}||r_{o7}))]}$$

The second stage doesn't contributes in the CMRR , it amplifies the CM-Gain that's a reason that we should have the gain of first stage is larger than the second stage

Stability and Phase Margin:

The stability of the system is more complicated than the single stage design so we should follow the design hints for compensation of the two stage OTAS

1- The topology has Two dominant poles so pole splitting is essential

$$\omega_{p1} = \frac{1}{R_{out1} * (Gm_2 * R_{out2}) * C_c}$$

$$\omega_{p2} = \frac{G_{m2}}{C_L + C_{int}}$$

Usually the internal pole (ω_{p1})is the dominant pole , so the BW is limited by the compensation capacitance Cc

2- $GBW = \frac{Gm_1}{C_c}$ For PM=76 we should design to achieve $\omega_{p2} = 4 * \omega_u$

$$4 * \frac{Gm_1}{C_c} = \frac{Gm_2}{C_L}$$

For good initial starting point We may pick $C_c = \frac{C_L}{2}$, we also should note that

$$Gm_2 \& C_C \text{ the two parameters that split the Two poles}$$

$$\frac{Gm_2}{G_{m1}} = 8$$

3- The compensation Capacitance Will introduce Feedforward Zero

- The Best solution to avoid instability is to place this zero at infinity by placing a resistance in series we Cc

$$R_Z = \frac{1}{G_{m2}}$$

4- The slew Rate of large input step is limited by the bias current of first stage and Cc

$$S_R = \frac{I_{B1}}{C_c}$$

Specs of the Design :

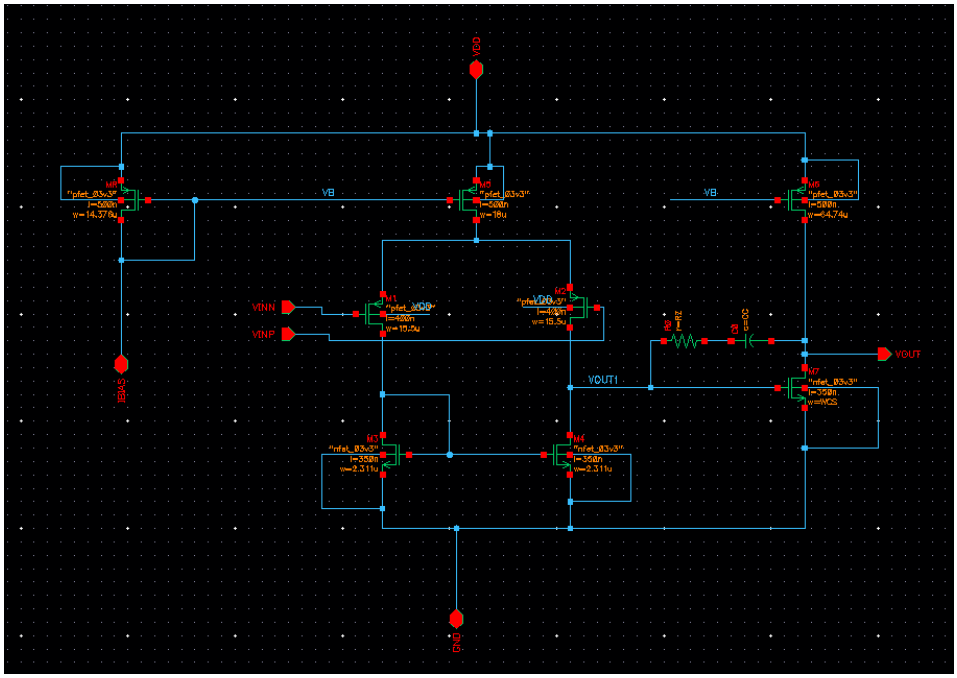
Technology	0.13um	0.18um
Supply voltage	1.2V	1.8V
Static gain error	<= 0.05%	<= 0.05%
CMRR @ DC	>= 74dB	>= 74dB
Phase margin (avoid pole-zero doublets)	>= 70°	>= 70°
OTA current consumption	<= 60uA	<= 60uA
CMIR – high	>= 0.6V	>= 1V
CMIR – low	<= 0.2V	<= 0.2V
Output swing	0.2 – 1V	0.2 – 1.6V
Load	5pF	5pF
Buffer closed loop rise time (10% to 90%)	<= 70ns	<= 70ns
Slew rate (SR)	$5V/\mu s$	$5V/\mu s$

Use an ideal external 10uA DC current source in your test bench (not included in the OTA current consumption spec), but design your own bias circuit (current mirrors)

Topology Selection:

$$V_{min} = 0.2v\,, V_{max} = 1v$$

The CMIR is closer to gnd than Vdd so we sill use PMOS Input stage



Design Decisions :

1- Open loop Gain :

$$\frac{1}{\beta * A_{OL}} \leq 0.05\%$$

$$A_{OL} \geq 2000$$

2- GBW :

$$t_{rise} \leq 70ns$$

10% → 90%

$$V_{out} = V_{max}\left(1 - e^{-\frac{t}{\tau}}\right) \text{ , } t_{rise} = t_2 - t_1 = 2.2\tau_{cl} = \frac{2.2 * A_{CL}}{\omega_u}$$

For unity gain buffer $A_{CL} = 1$, $f_u \geq 5MHz$

3- Compensation capacitance :

Assume $C_C = \frac{C_L}{2} = 2.5Pf$

$$S_R = \frac{I_{B1}}{C_C} \geq 5$$

$$I_{B1} \geq 12.5uA$$

Design for IB1=12.5uA

4- Interconnection between first and second stage :

$$V_{GS4} = V_{GS7}$$

As for the common mode input $V_{outdc} = V_{GS4}$, from swing spec

$$V^*_{7Max} = 0.2v \text{ , } \left(\frac{gm}{id}\right)_{Min_{activeLoad}} = 10$$

The Current mirror for the Two stages have the same V_{GS}

$$V_{GS5} = V_{GS6} = V_{GSMIRROR}$$

5- Gain Distribution :

As an initial Guess we can say that

$$\boldsymbol{A_{V1} = 65\,, A_{V2} = 30.77}$$

This Distribution could be chosen randomly making $A_{V1} > A_{V2}$

Design of the First Stage :

Design of Input pair :

$$A_{V1} = 65 = g_{m12} * \frac{r_o}{2}$$

Assume $r_{o1} = r_{o4}$ For simplicity

$$GBW = \frac{gm_1}{2 * \pi * C_c} = 5MHz$$

$$g_{m1} = 78.54uS$$

For our assumption for Current $I_{B1} = 12.5uA\,, I_{D1} = 6.25uA$

So we should use $\frac{gm}{id} = 12.57$

- ⇨ For the assumed gain :

  $$r_o = 1.655M\Omega, g_{ds} = 604.154nS$$

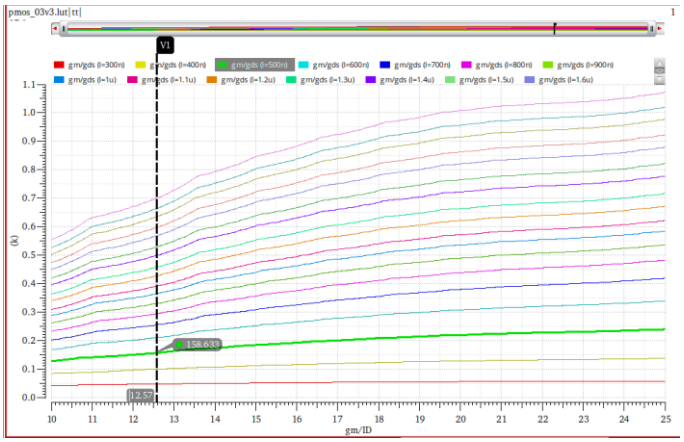
  Then we have condition on L :

  $$\frac{gm}{gds} > 130$$

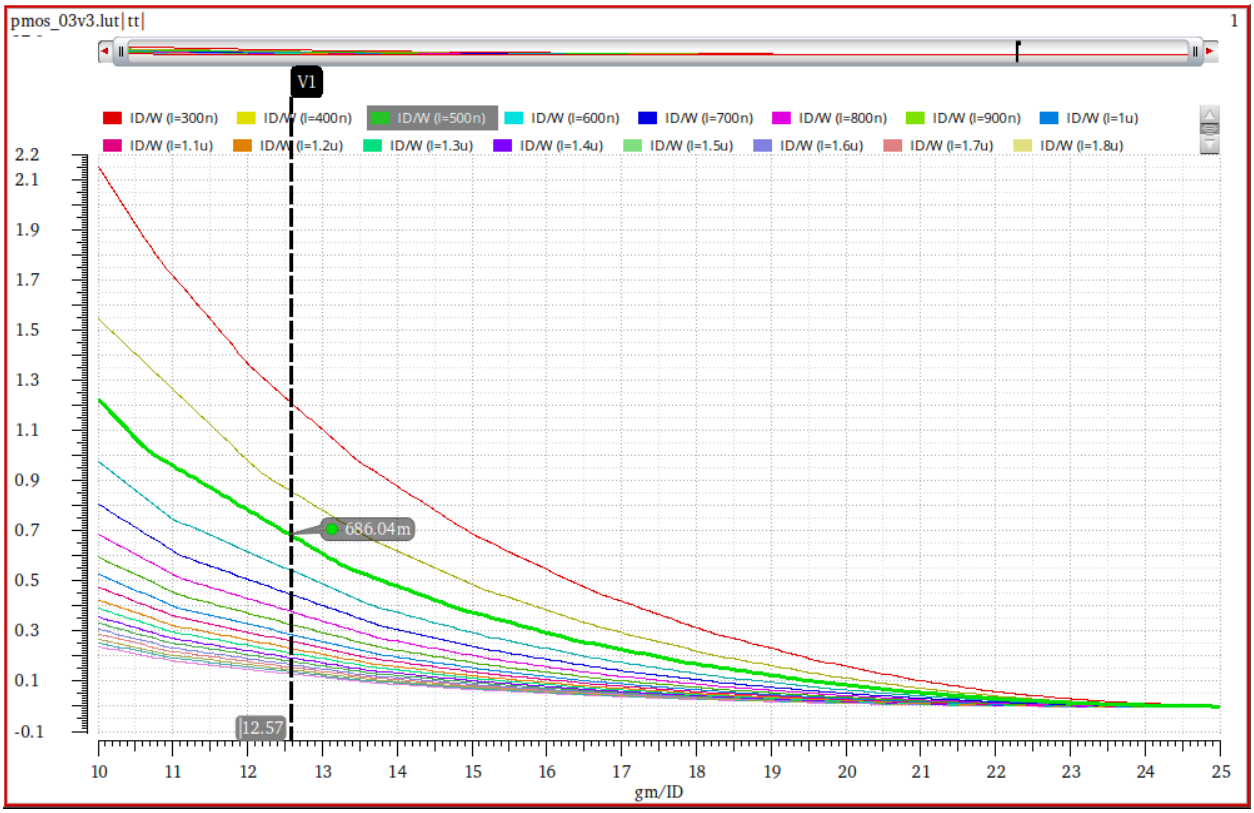
  Assume VDS =0.6 V, $\boldsymbol{V_{SB} = V_{DS} = V^* + Margin = 0.3}$
  From design charts we would pick other parameters:

- From the condition on L and gm/id we can pick L :

  $$L = 500nm$$



We know that the $I_{D1} = 6.25uA$ From ID/W we can get W:



$$W = 9.11um$$

⇨ Input pair Values M1 & M2 :

gm/id	12.57
W	9.11um
L	500n
V_{GS}	1.01v

⇨ Voltage estimation and check:

@ The CMIR high : $vincm = 1v$, $V_{DS_{TAIL}} = V_{DD} - (V_{INCM} + V_{GS_1})$

We have known that the minimum

$V^*_{max} = 0.2v \; and \; for \; 100mv \; margn \; we \; should \; have \; 0.3 \; at \; least \; to \; pass \; corners$

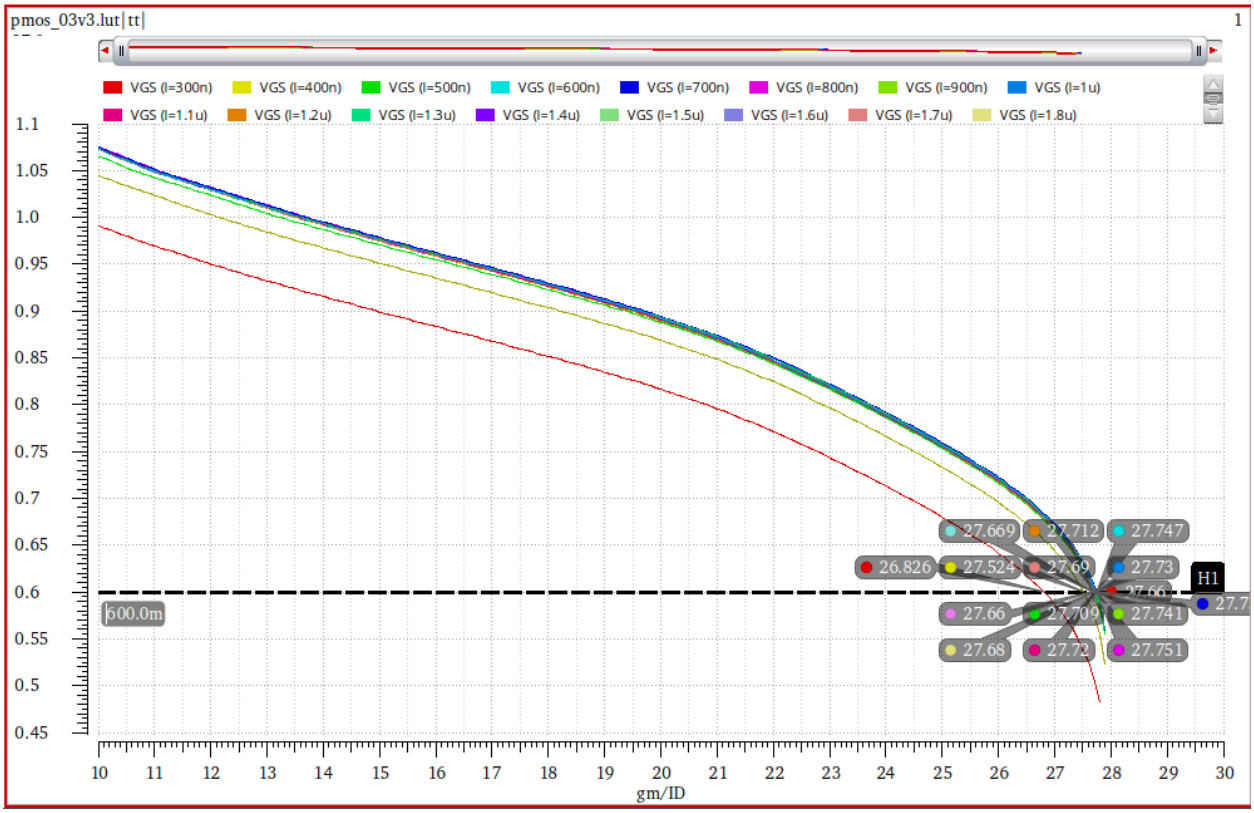
For $V_{incm} = 1v \rightarrow V_{DS} = -0.21$!! For this common mode

We have two choices :

1- Design For higher gm/id to have lower VGS
2- Violate the Common mode input range high

1- Design For higher gm/id to have lower VGS :

$$0.2 = 1.8 - (1 + V_{GS}) \rightarrow V_{GS} = 0.6 = 600mv$$



⇨ We can find that this VGS is not feasible for our technology GF_180nm as it has serious body effects when $VSB \neq 0$

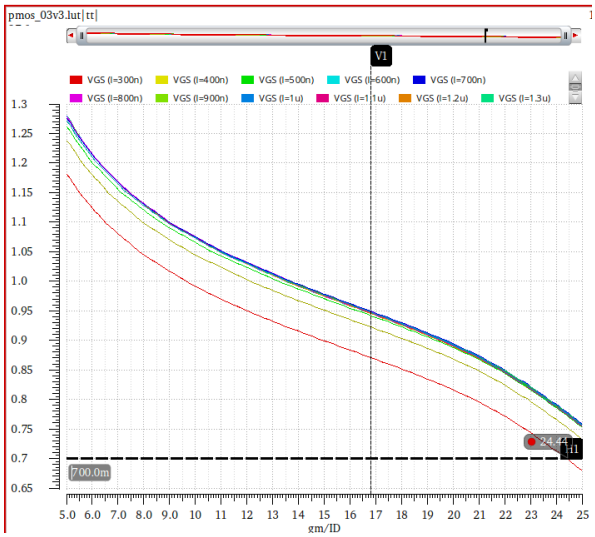
2- Violating the CMIR high:

$$V_{DS_{TAIL}} = V_{DD} - (V_{INCM} + V_{GS_1})$$

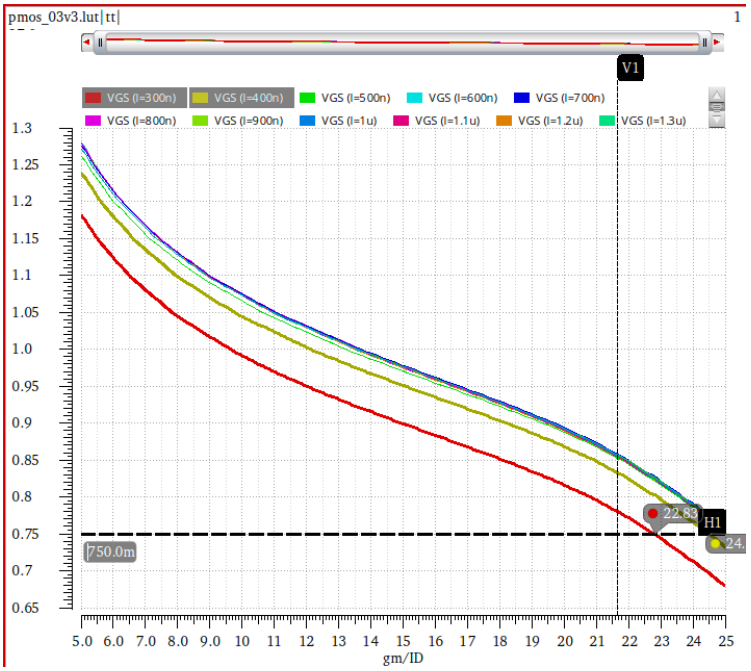
For Our VGS find the max feasible V_{incm}, we will

⇨ **<u>Iteration 1:</u>** Assume $V_{incmH} = 0.9V$, $V_{GS1} = 0.7V$

"Not Feasible In Moderate inversion
We should Bias in WI to achieve this
This will give us huge area for our Given Current"

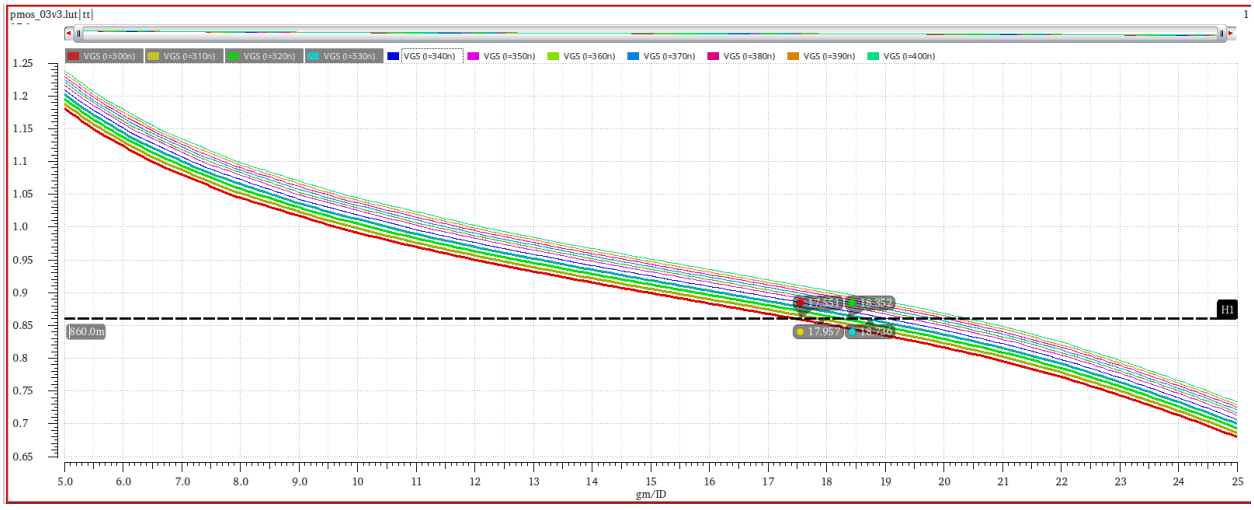


⇨ **Iteration 2:** Assume $V_{incmH} = 0.85V$, $V_{GS1} = 0.75v$



⇨ **Iteration 3:** Assume $V_{incmH} = 0.75V$, $V_{GS1} = 1.8 - 0.2 - 0.75 = 850mv$

We can find that our solution converge for L between 300n to 400n so we can sweep this range of L's to find a proper Bias point , we should note that changing this bias point will change the gain distribution



⇨ NEW CMIR: 0.2V - 0.74 V

⇨ For gm/id :17.6 to 18.7 For L : 300n to 330n

⇨ gm:110uS to 116.875uS

then the gain of the first stage must be within range of

GBW: 7MHz to 7.44MHz

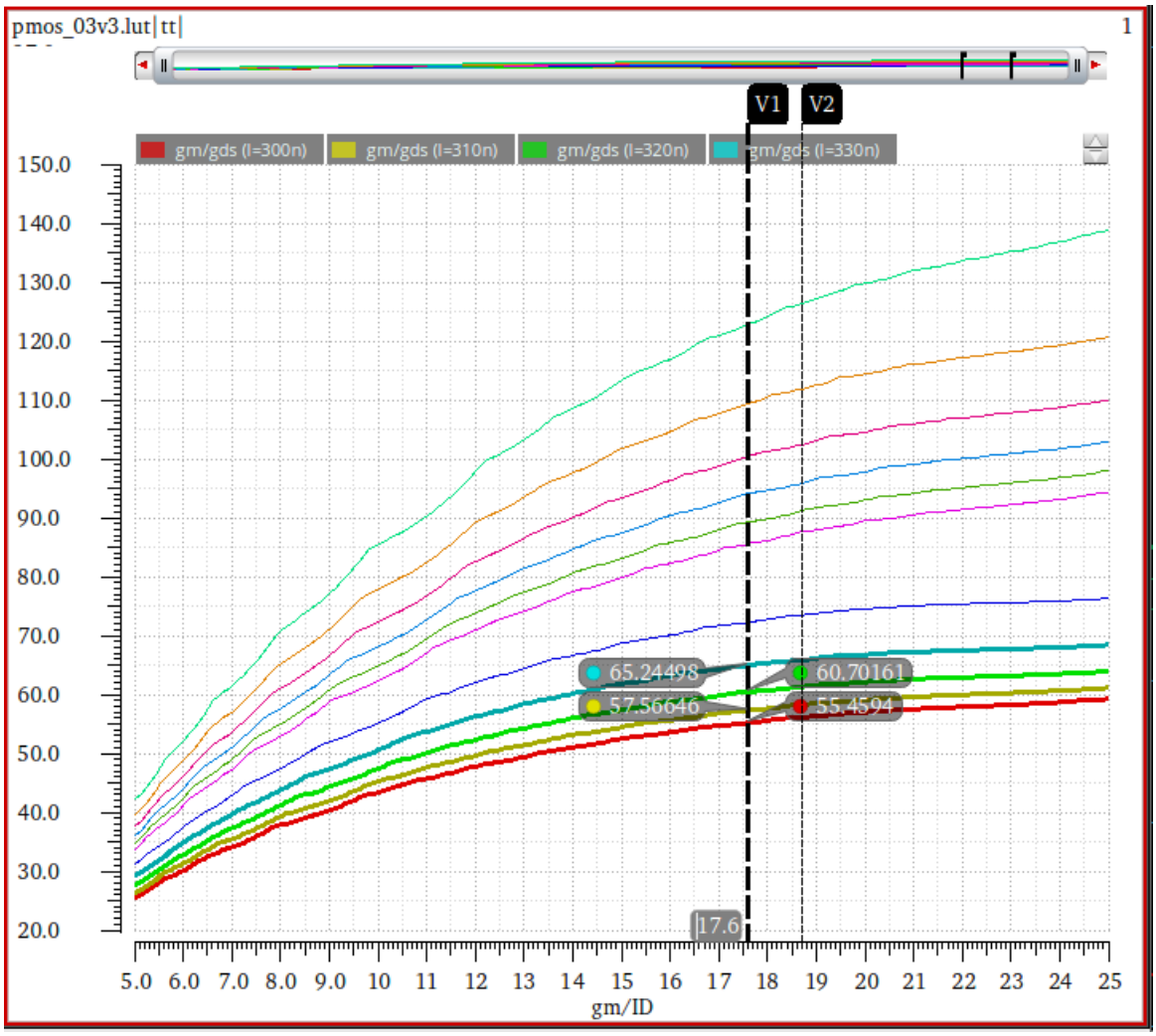
Assuming that we are keeping our gain distribution is constant

$$A_{V1} = 65\,, A_{V2} = 32\,, second\ stage\ higher\ gain\ for\ overspec$$

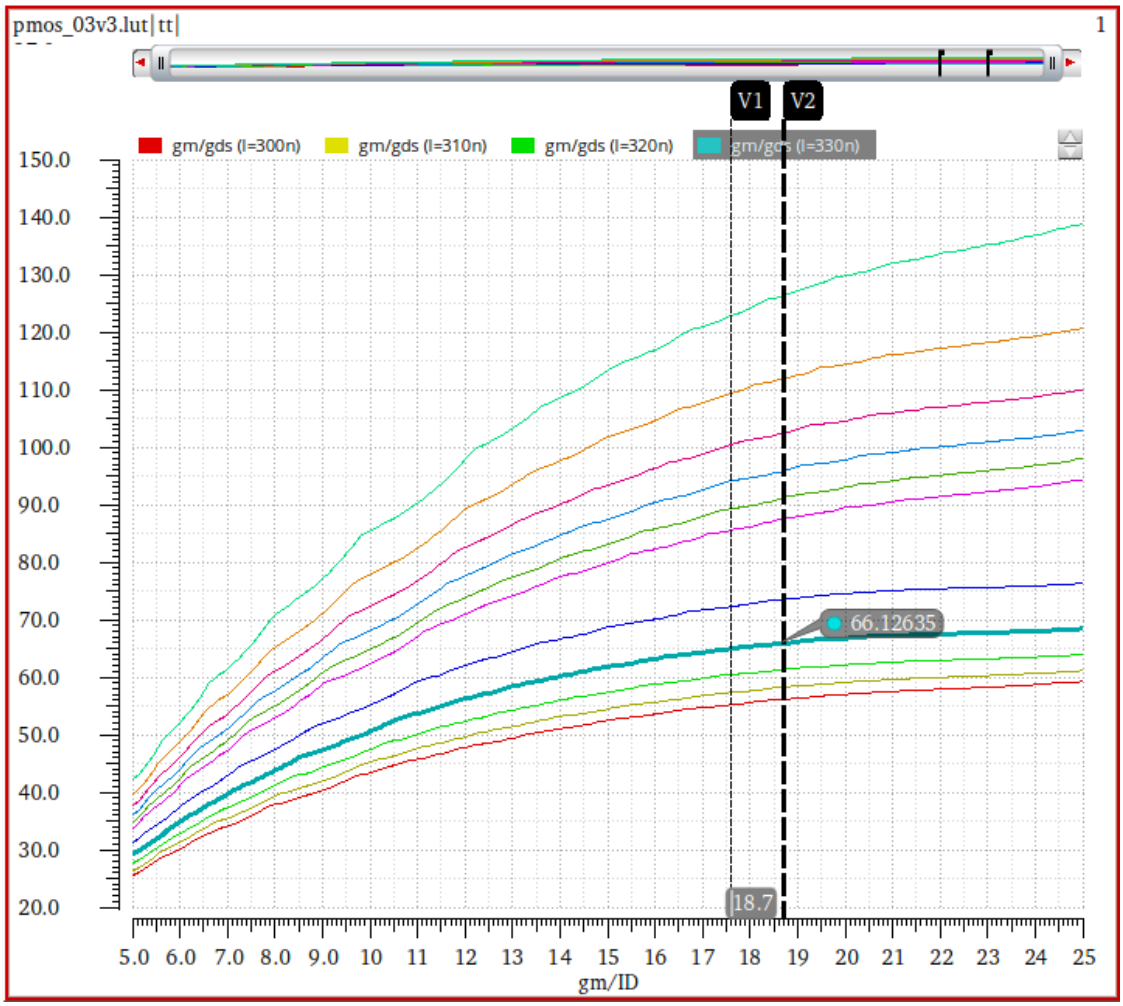
$$\boldsymbol{A_{V1} = gm_1 * \frac{r_o}{2} = 65}$$

gds: 846.15nS to 899nS

so we can find that this gain for first stage is not achievable for gm/id range



We can pick L=330n and gm/id =17.6 to Design the input pair at

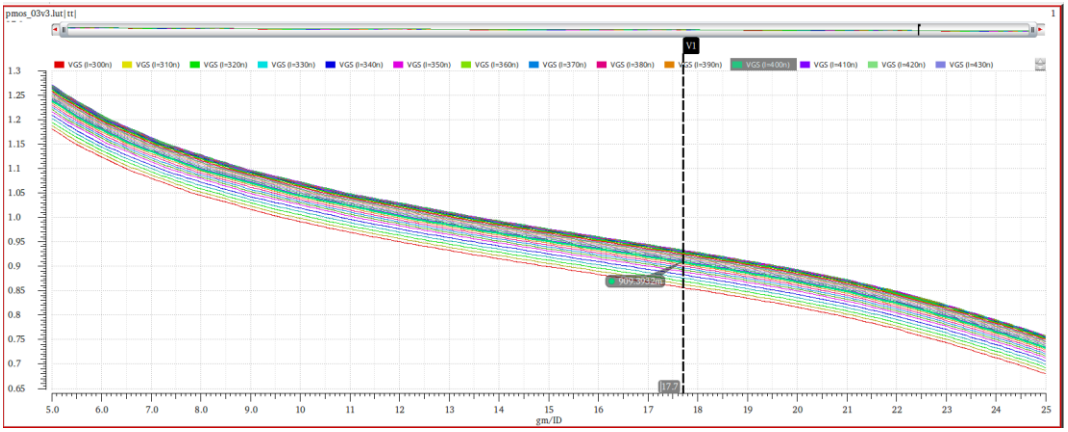


⇨ gm/gds<66.12635 and gm=110uS so we have gds=1.663uS

The gain of the first stage :

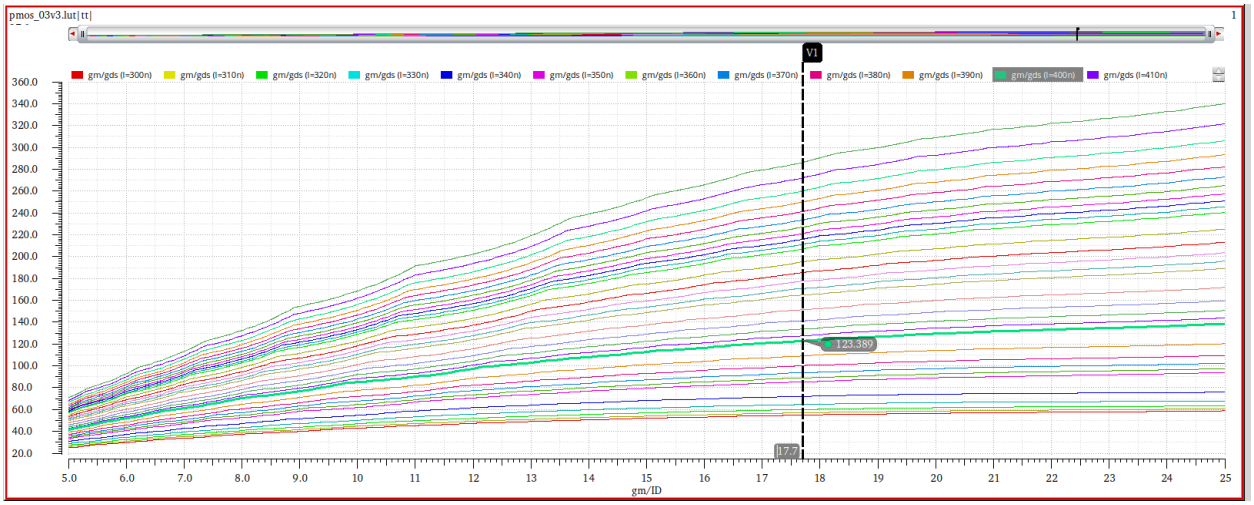
$A_{V1} = 33.1 < A_{V2}$ we need higher L for achieving the gain

⇨ **Iteration 4:** Assume $V_{incmH} = 0.7V$, $V_{GS1} = 1.8 - 0.2 - 0.7 = 900mv$



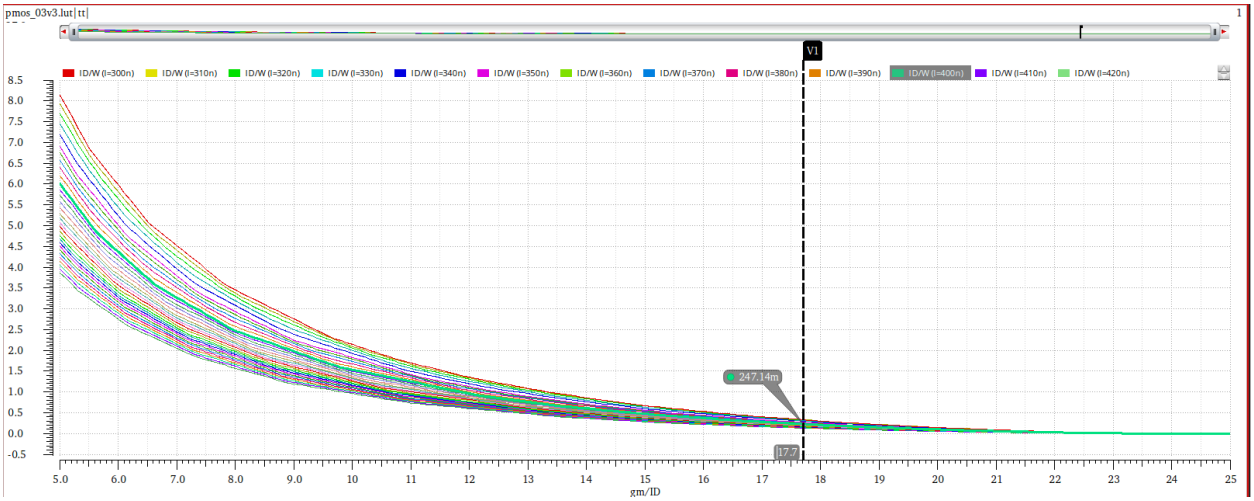
⇨ Pick L=400nm and gm/id=17.7

$$gm = 110.625uS$$



⇨ gm/gds =123.389 "Not a big deviation from our initial condition "

⇨ gds=896.55nS ➔ $A_{V1} = 61.695, A_{V2} = 33$



W=25.3um

Conclusions:

⇨ CMIR reduced for Initial Design to be 0.2 v – 0.7 v

⇨ **Final Design Point M1 & M2 :**

$\frac{gm}{id}$	17.7
gm	110.625uS
A_{V1}	61.695
ID	6.25uA
W	25.3um
L	400nm
V_{GS}	909.4m
gds	896.55nS

Design of Active load :

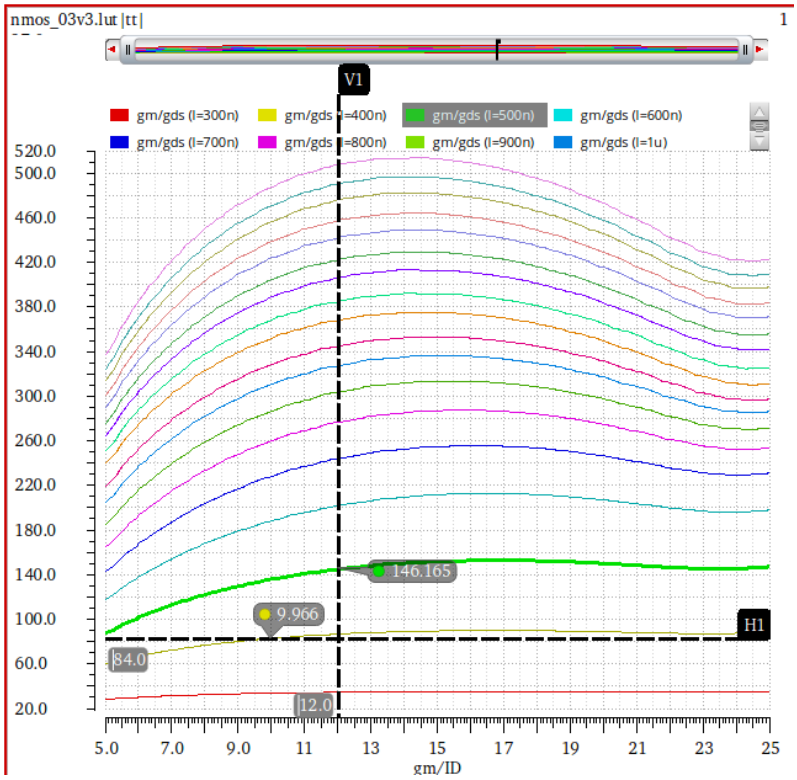
$$g_{ds} = 896.55nS$$

$$V_{DS} = 0.9v$$

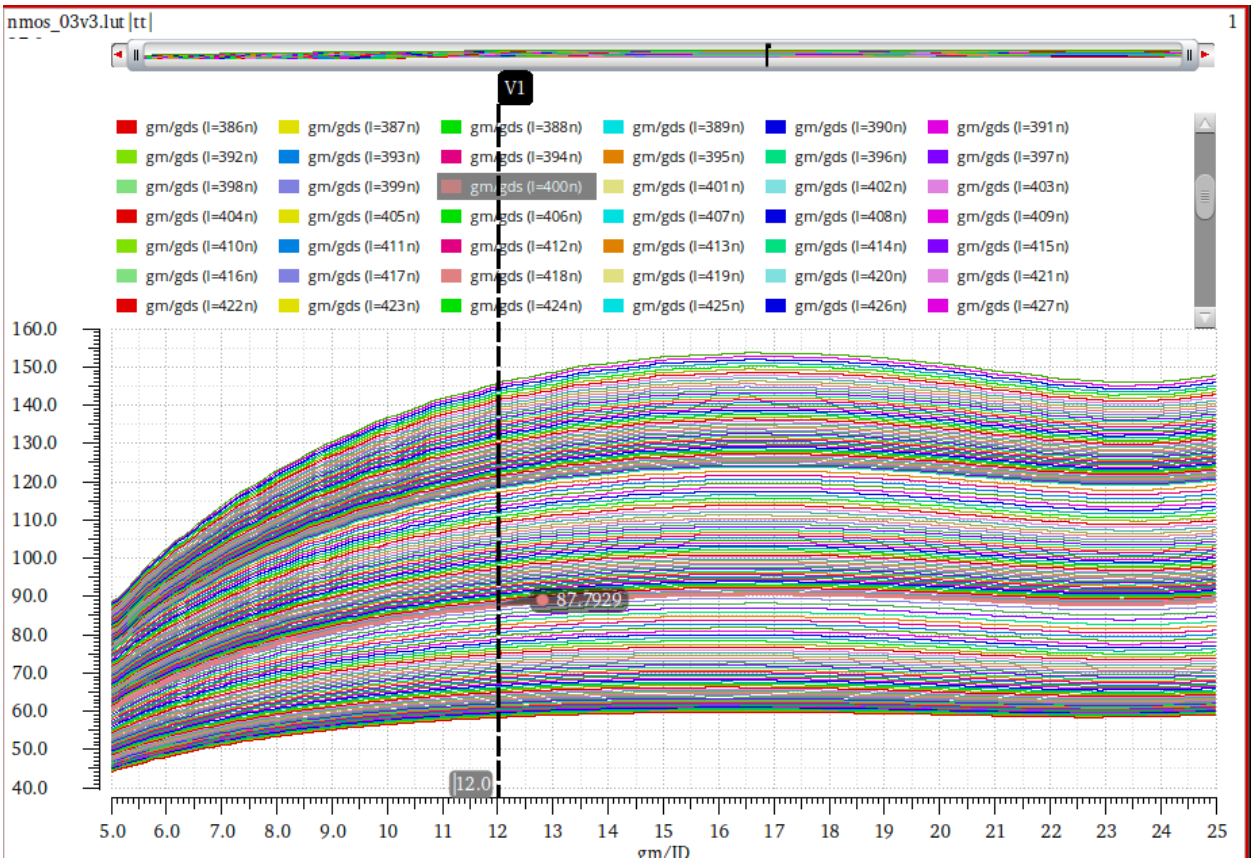
We have here

$V_{GS3} = V_{GS7}$ *so both TS have the same Bias point and* $V^*_{max} = 0.2V$ *, so* $\left(\frac{gm}{id}\right)_{min} = 10$

Assume gm/id =12 ➔ $gm_{3,4} = 75uS \rightarrow \frac{gm}{gds} > 83.65$



⇨ Our L is in range of L=350n to L=500n so we will sweep on this range with low step to get it

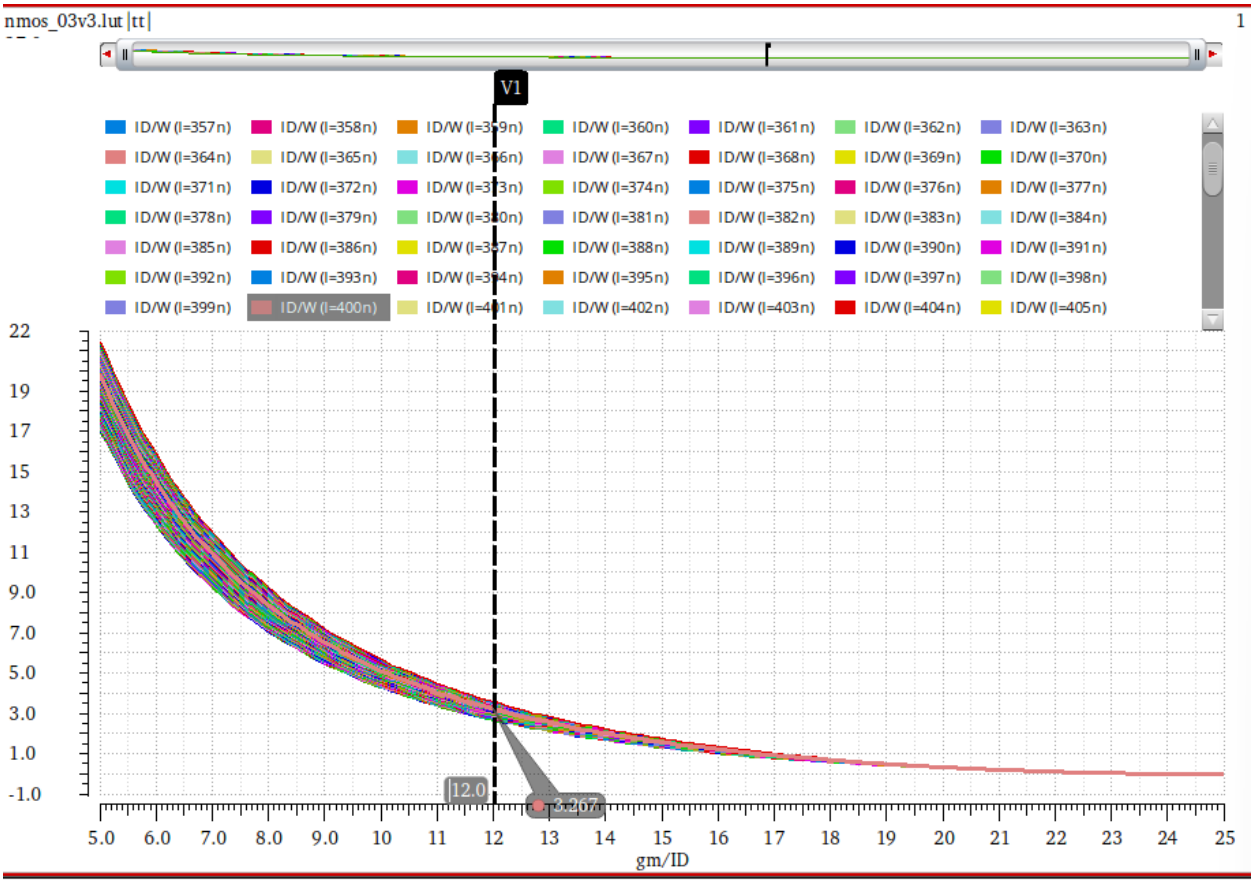


$L = 400nm$ $\frac{gm}{gds} = 87.8$ keeping same current ID=6.25u

For our $gm = 6.25uA * 12 = 75uS$ we have:

$g_{dsNew} = 854.21nS$ ➔ So the gain of the first stage is Modified we need to calculate a new gain distribution

$$A_{V1} = r_{o1}||r_{o4} * gm_1 = 63.187\,, A_{V2} = 32$$



$$W = 1.913um$$

⇨ **Final Design point M3 & M4**

$\frac{gm}{id}$	12
gm	75uS
A_{V1}	63.187
ID	6.25uA
W	1.913um
L	400nm
V_{GS}	781.551m
gds	854.21nS

Design of Tail CS :

$$V_{DS} = 0.3\,V\,, I_{B1} = 12.5uA$$

CMRR=> $74dB > 5012 = \frac{A_{Vd}}{A_{Vcm}} = \frac{63.2}{??} \rightarrow A_{VCM} == \frac{1}{2*g_{m3,4}*r_{o5}}$

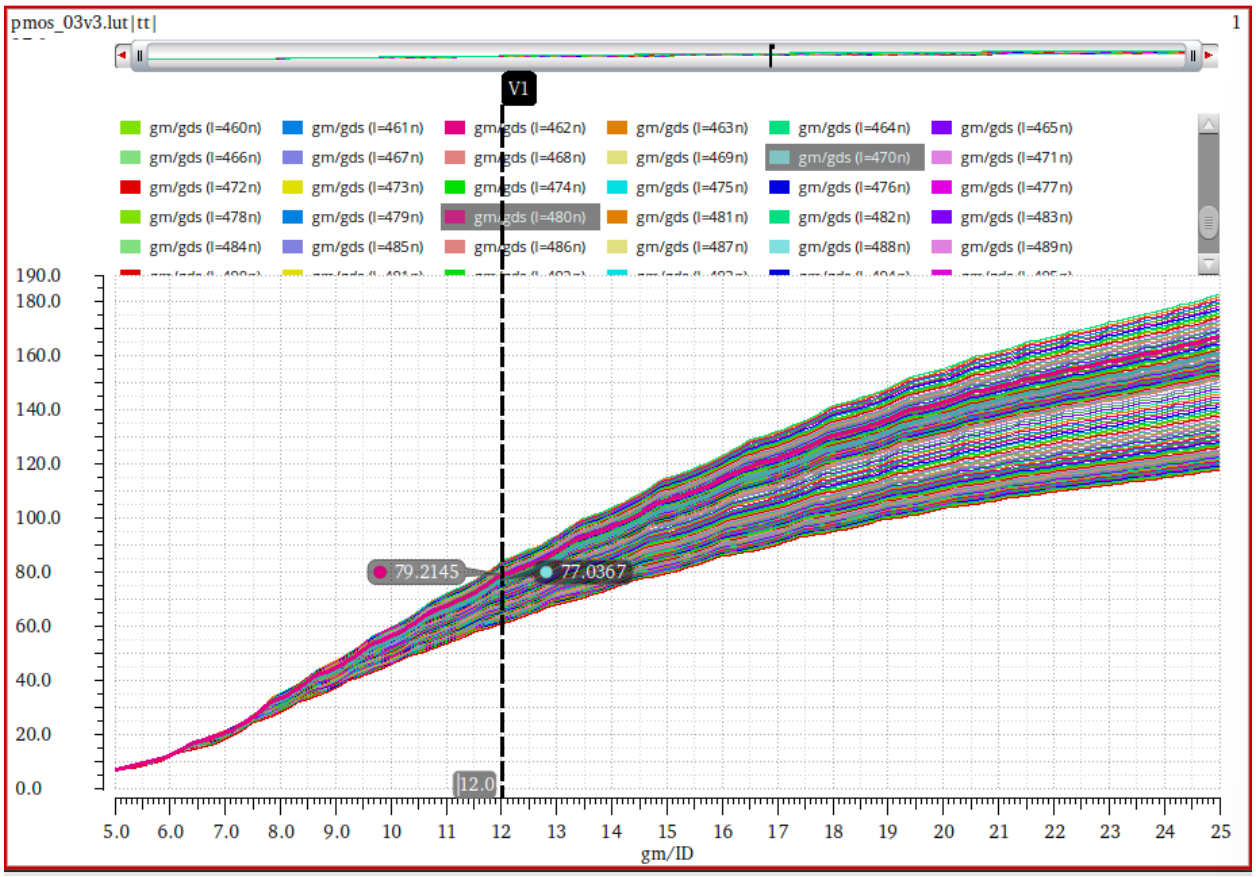
$$\therefore \frac{1}{2 * gm_{3,4} * r_{o5}} = 0.0157$$

$$gm_{3,4} = 75uS \rightarrow g_{ds5} = 1.891uS$$

For The Active Load we have $\left(\frac{gm}{id}\right)_{min} = 10$ we can pick $\frac{gm}{id} = 12$

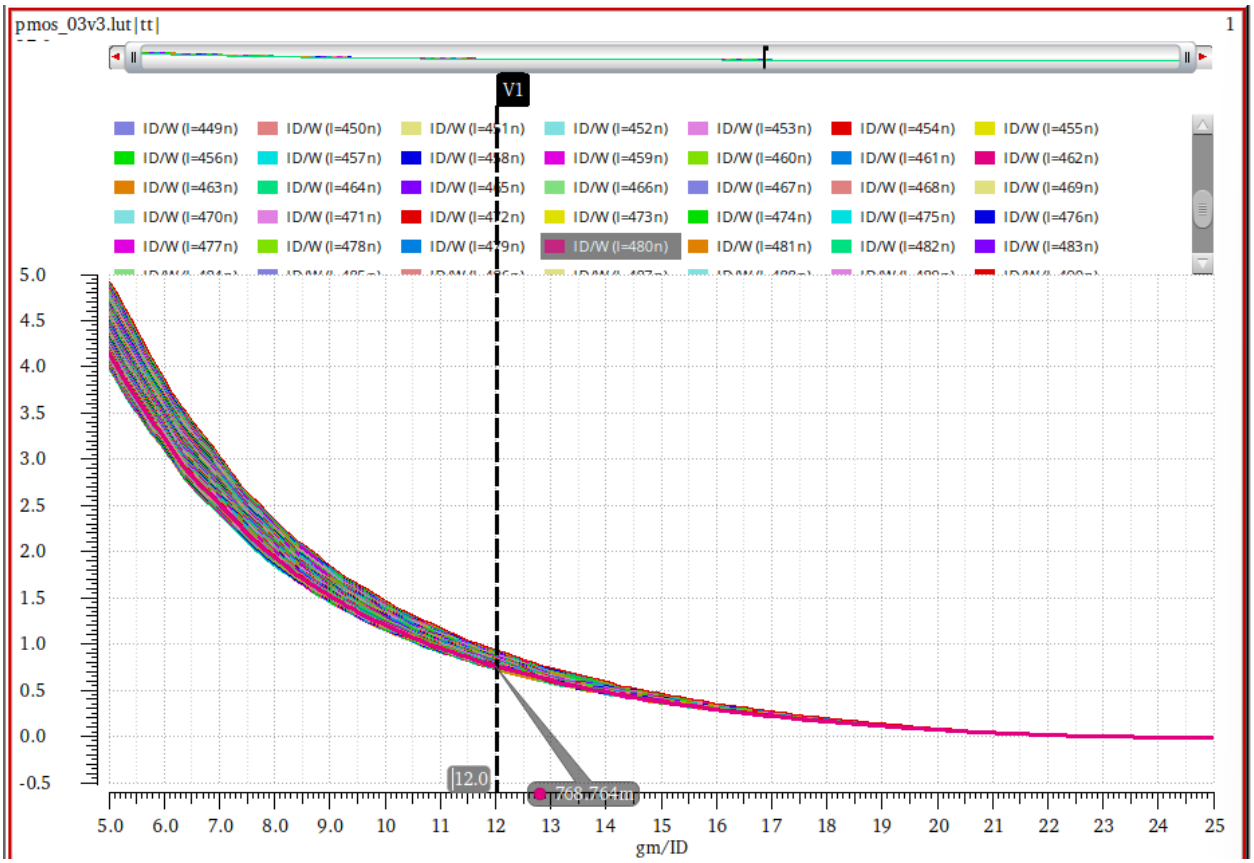
$$gm_t = 150uS$$

⇨ gm/gds > 79.323



$$L = 480n$$

$$g_{ds_{new}} = 1.894uS$$



$$W = 16.26um$$

⇨ **Final Design Point of M5:**

$\frac{gm}{id}$	12
gm	150uS
A_{V1}	63.2
ID	12.5uA
W	16.26um
L	480nm
V_{GS}	898.664m
gds	1.894uS

Tail CS of the second stage :

- ⇨ For Good mirroring we must have same L=480n As M5 and we must have same VGS

$$V_{GS} = 898.664mv$$

$$\frac{gm}{id} = 12$$

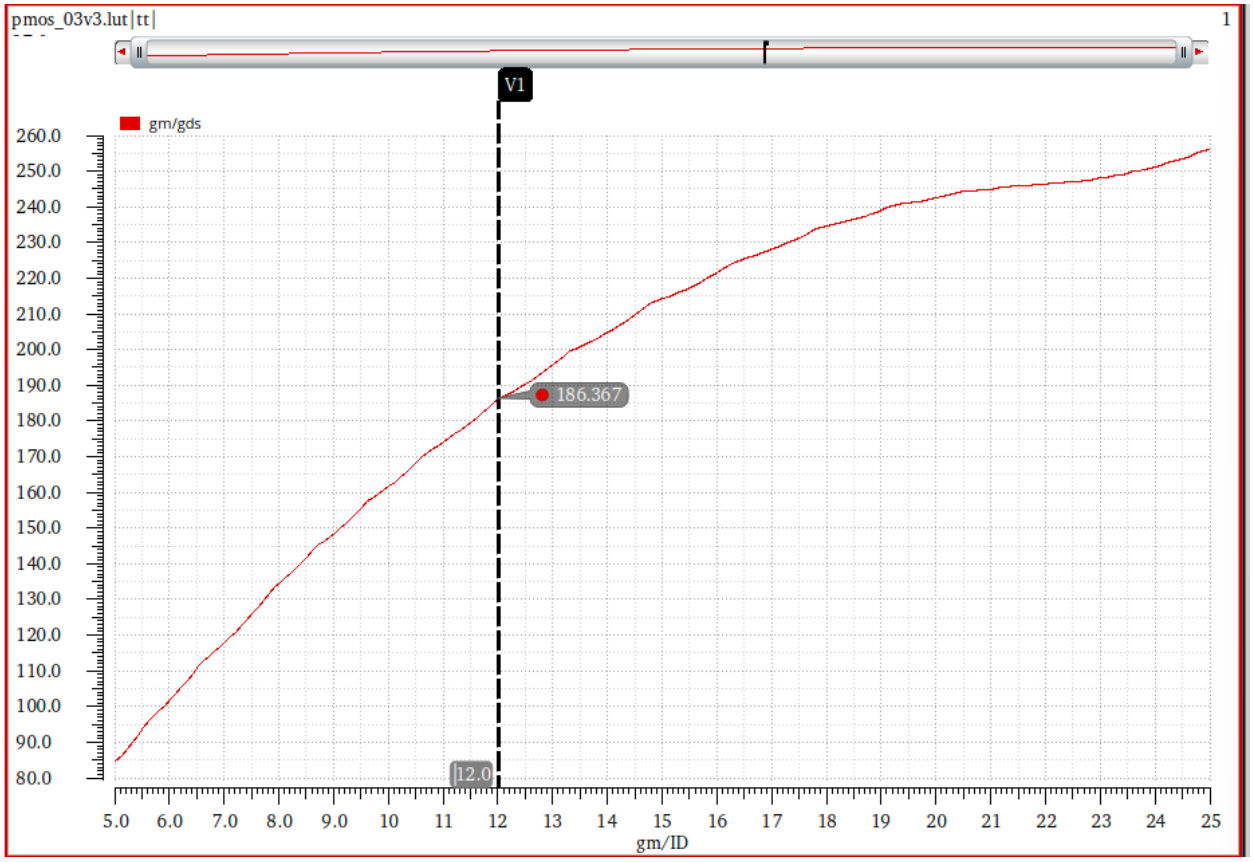
We have used 12.5uA in the first stage

In order to keep the same current Budget we need $I_{B2} < 47.5uA$, $I_{B2} = 45uA$

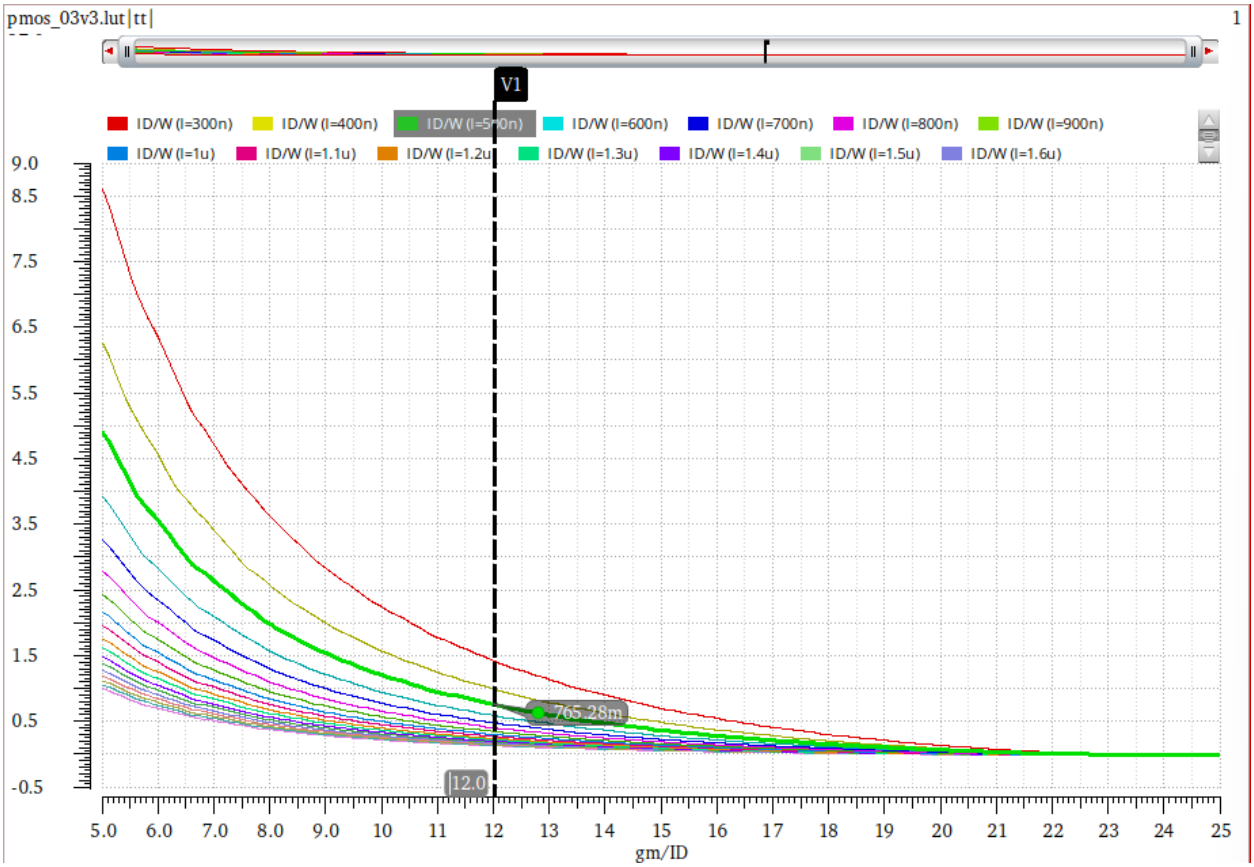
- ⇨ To achieve PM>76 we need Higher current in the second stage $I_{B2} = 73.5uA$ or higher gm_7

VDS= 0.9V

- ⇨ $g_{m6} = 540uS$



$$g_{ds6} = 2.898uS$$



$$W = 55.71um$$

⇨ **Final Design Point of M6 :**

$\frac{gm}{id}$	12
gm	540uS
A_{V1}	63.2
ID	45uA
W	55.71um
L	480nm
V_{GS}	898.664m
gds	2.898uS

Design of Current mirror:

$$I_{IN} = 10uA \rightarrow \frac{W_{ref}}{W} = \frac{I_{ref}}{I}$$

For first stage we have $W = 16.26um$ ➔ $W_{ref} = 13um$

For second stage we have W=55.71um ➔ $W_{ref} = 13um$

Same L=480nm Will be tuned after simulation

Design of CS stage:

$$V_{GS3} = V_{GS7} = \mathbf{781.551m}$$

⇨ To reduce the offset voltage we need to make both of them have the same bias point

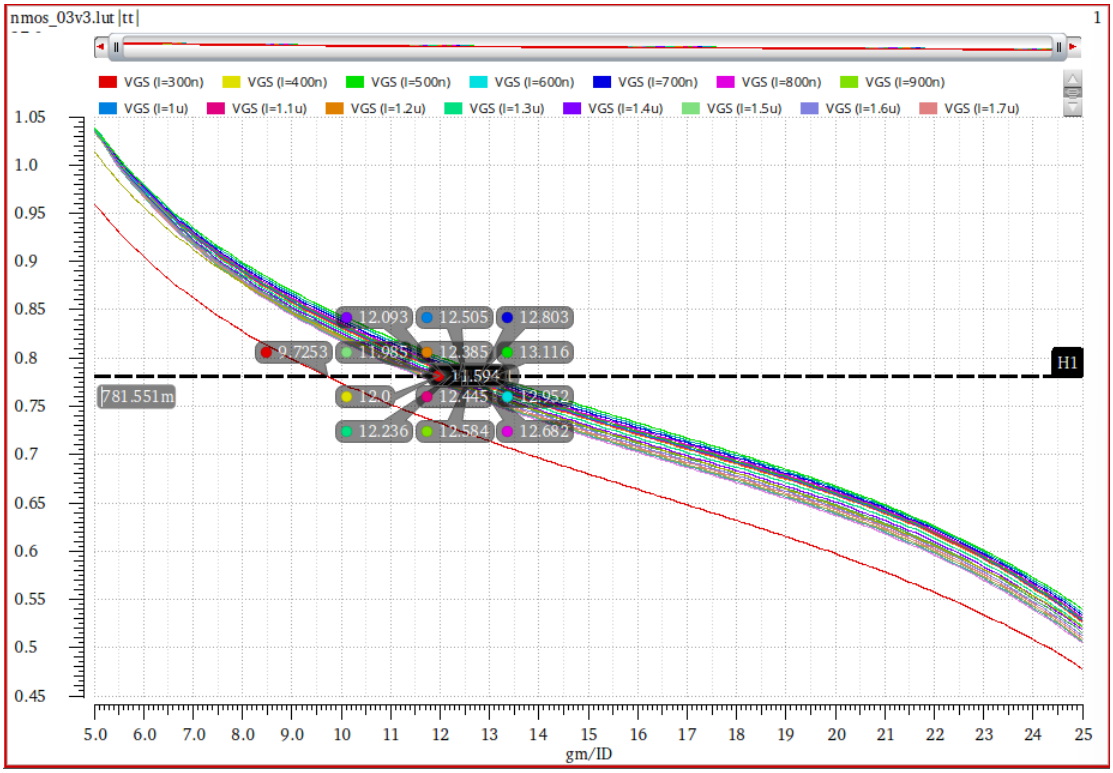
$$A_{V2} = 26 = gm_7 * (r_{o6} || r_{o7})$$

$$r_{o6} = 156.54k\Omega$$

$$\underline{\boldsymbol{V_{DS} = 0.9}}$$

Minimum gm/id=10 from output swing spec

we must keep VGS=781.551mv



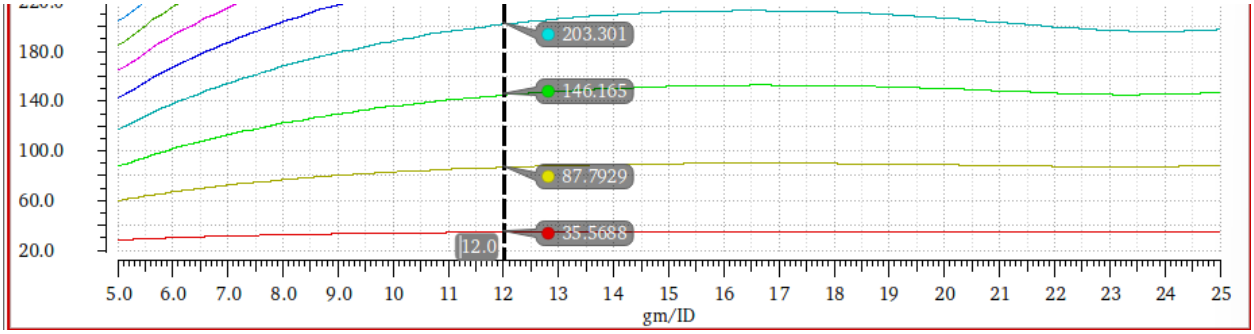
⇨ For zero offset minimum gm/id=12

⇨ We can see from the plot the points that can achieve this requirement from L=400n to L=2u

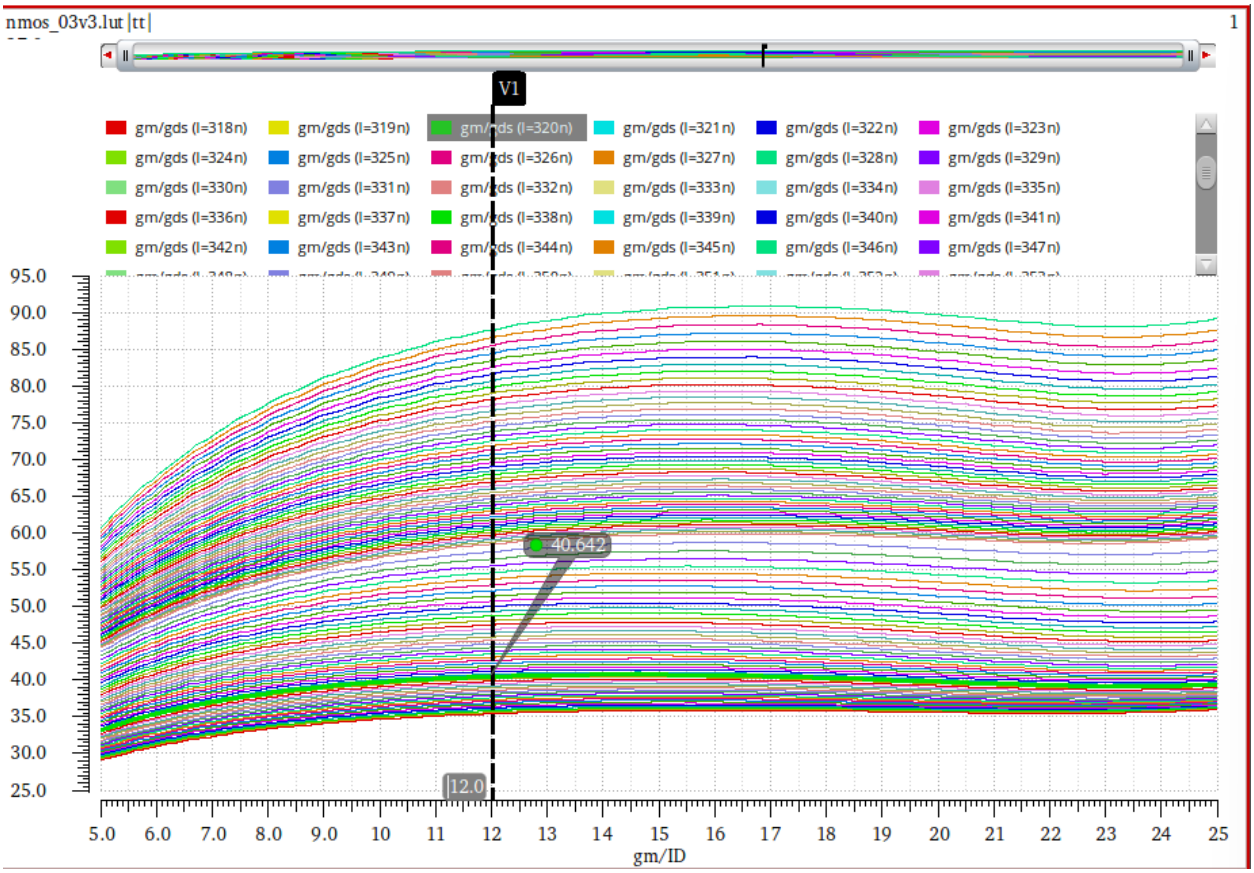
Iteration1: Assume gm/id=12➔ $g_m = 540uS$

For our gain spec $A_{V1} = 32 = g_m * \frac{1}{g_{ds6}+g_{ds7}}$ ➔ $g_{ds7} = 13.977uS$

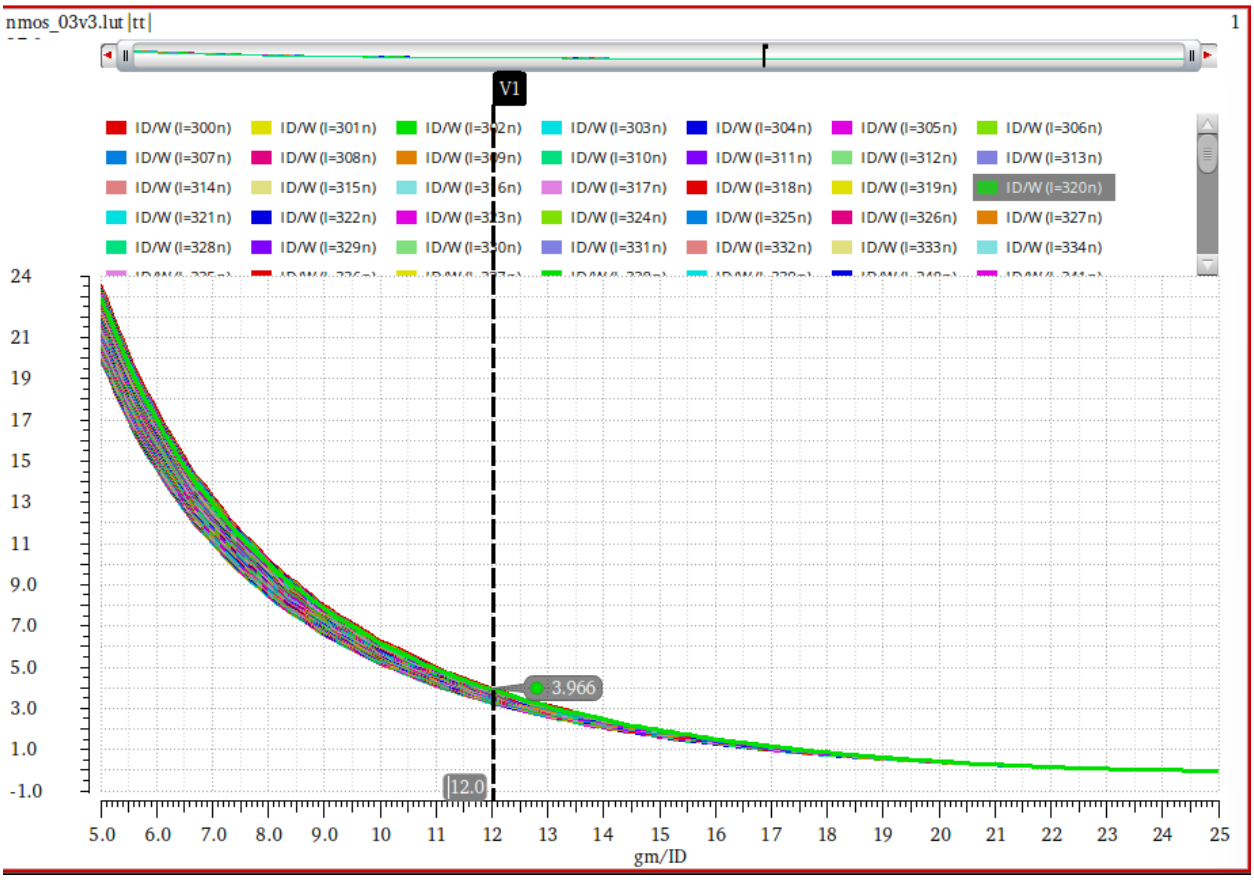
$$\frac{g_m}{gds} = 40.3$$



⇨ We can find our L in range od L=300n to L=400n



$$L = 320nm$$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12.0
5.0 6.0 7.0 8.0 9.0 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25
gm/ID

$$W = 11.35um$$

Sizing Summary :

- **Input pair M1 &M2 :**

$\frac{gm}{id}$	17.7
gm	110.625uS
A_{V1}	61.695
ID	6.25uA
W	25.3um
L	400nm
V_{GS}	909.4m
gds	896.55nS
V_{DSAT}	890.6m
V_{OV}	18.8m
V^*	114.1m

- **Active Load M3&M4 :**

$\frac{gm}{id}$	12
gm	75uS
A_{V1}	63.187
ID	6.25uA
W	1.913um
L	400nm
V_{GS}	781.551m
gds	854.21nS
V_{DSAT}	137.3m
V_{OV}	88.4m
V^*	167.7m

- **Tail CS M5;**

$\frac{gm}{id}$	12
gm	150uS
A_{V1}	63.2
ID	12.5uA
W	16.26um
L	480nm
V_{GS}	898.664m
gds	1.894uS
V_{DSAT}	141.8m
V_{OV}	113.76
V^*	167m

- **Active load of second stage:**

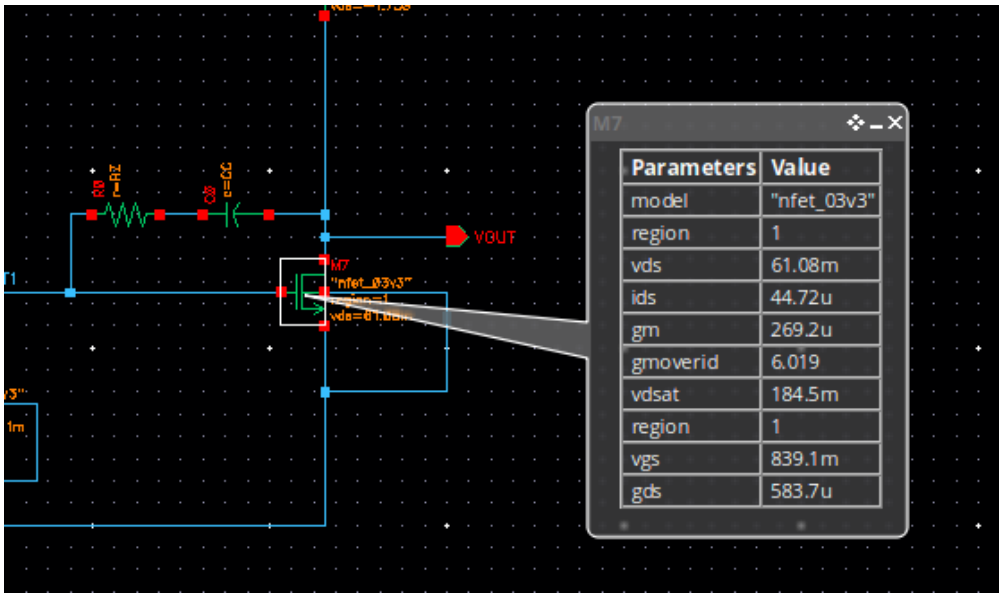
$\frac{gm}{id}$	12
gm	540uS
A_{V1}	63.2
ID	45uA
W	55.71um
L	480nm
V_{GS}	898.664m
gds	2.898uS
V_{DSAT}	142.2m
V_{OV}	114.5m
V^*	167m

- **Common Source Amplifier:**

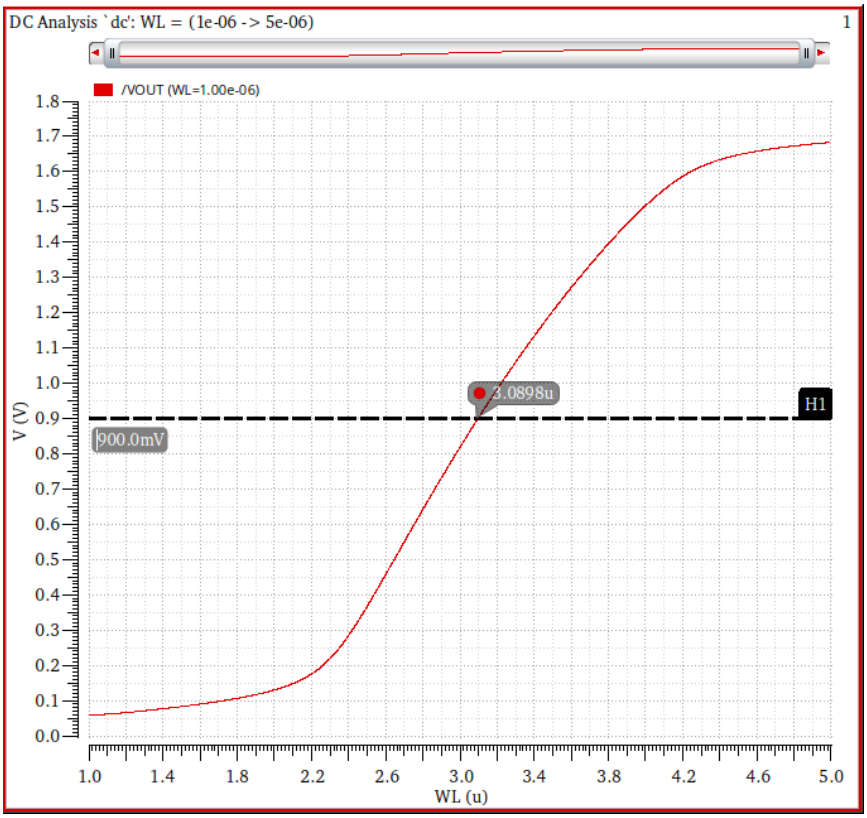
$\frac{gm}{id}$	12
gm	540uS
A_{V1}	78.7
ID	45uA
W	11.35um
L	320nm
V_{GS}	781.551m
gds	13.997uS
V_{DSAT}	129.9m
V_{OV}	117.95m
V^*	0.167

OP Results Debugging :

- ⇨ The output is latched to the gnd so we need to sweep W for the Active load and pick W for VDS to be 0.9v



- ⇨ WL=3.0898um

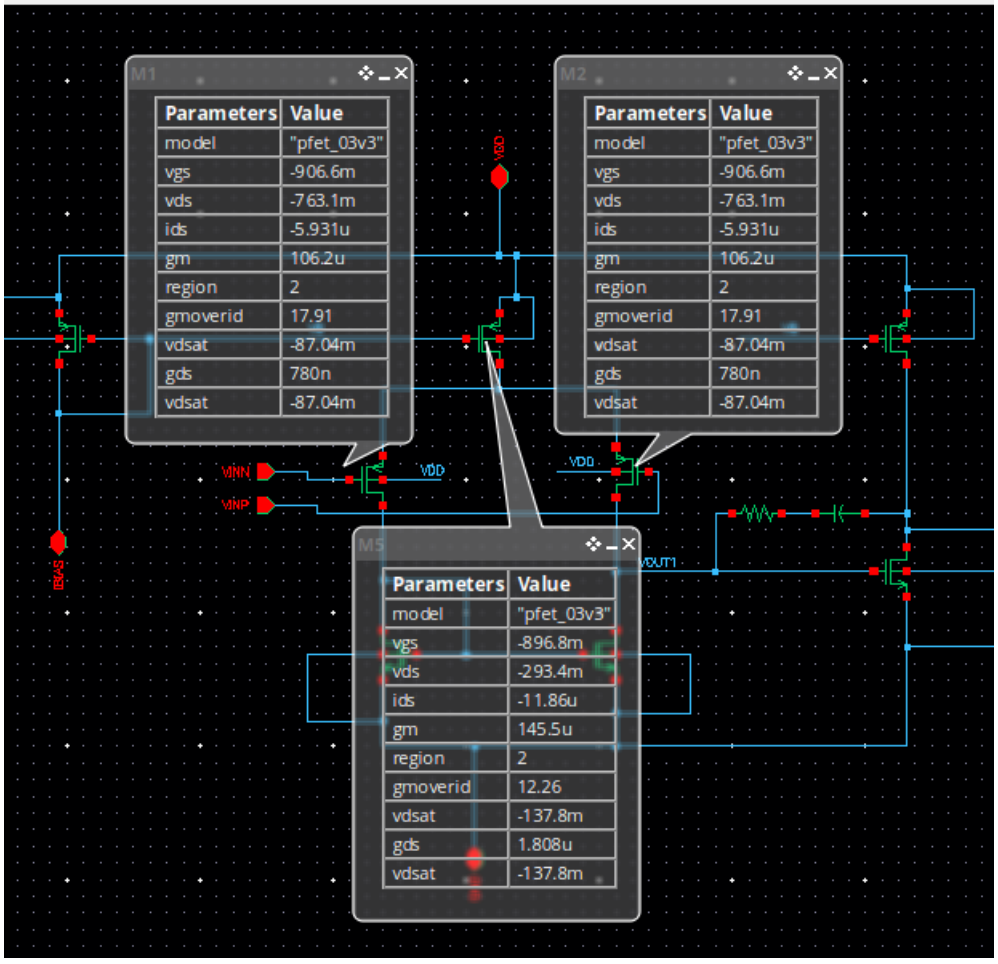


- **For input pair and Tail CS :**

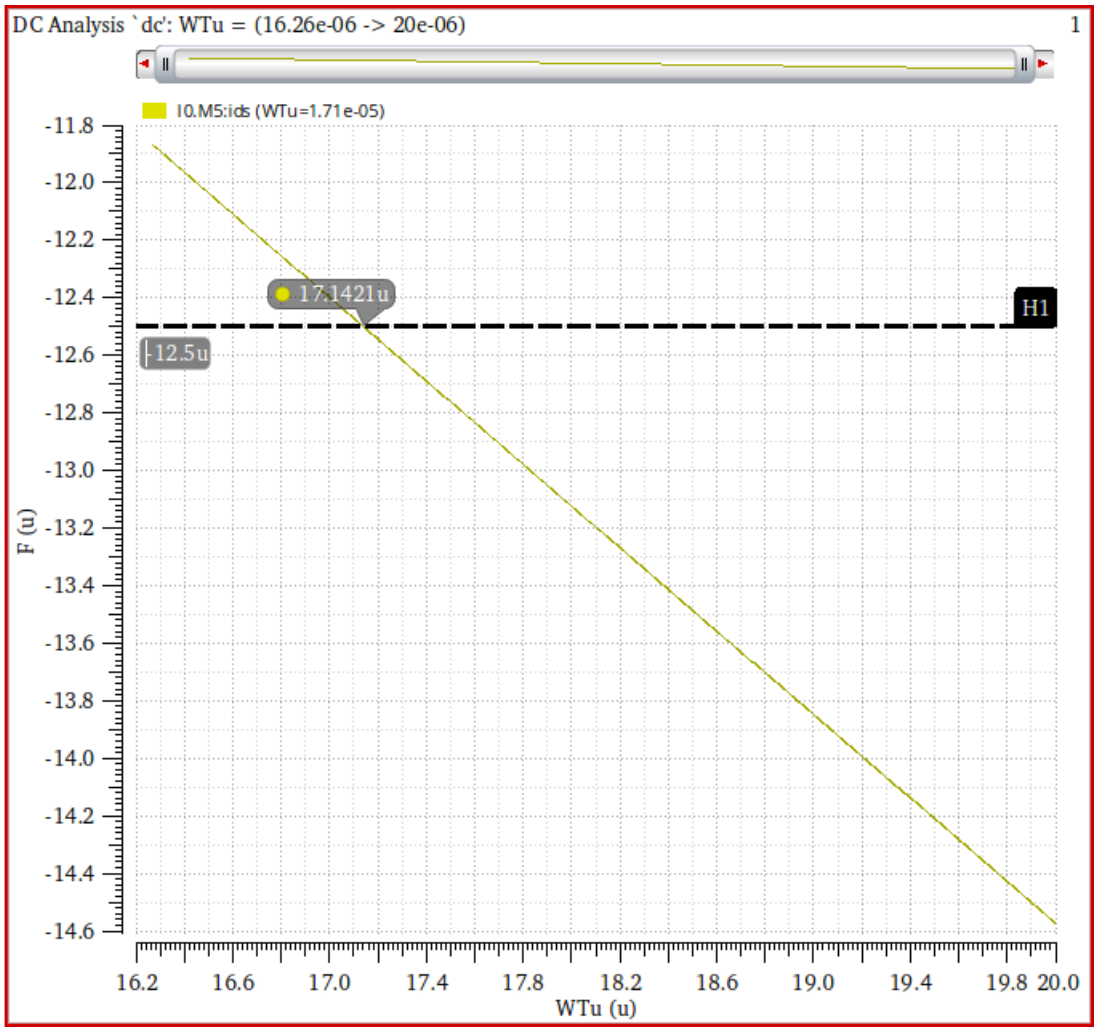
⇨ **Input pair M1 & M2 :** ➔ **Tail CS M5 :**

$\frac{gm}{id}$	17.7
gm	110.625uS
A_{V1}	61.695
ID	6.25uA
W	25.3um
L	400nm
V_{GS}	909.4m
gds	896.55nS
V_{DSAT}	890.6m
V_{OV}	18.8m
V^*	114.1m

$\frac{gm}{id}$	12
gm	75uS
A_{V1}	63.187
ID	6.25uA
W	1.913um
L	400nm
V_{GS}	781.551m
gds	854.21nS
V_{DSAT}	137.3m
V_{OV}	88.4m
V^*	167.7m



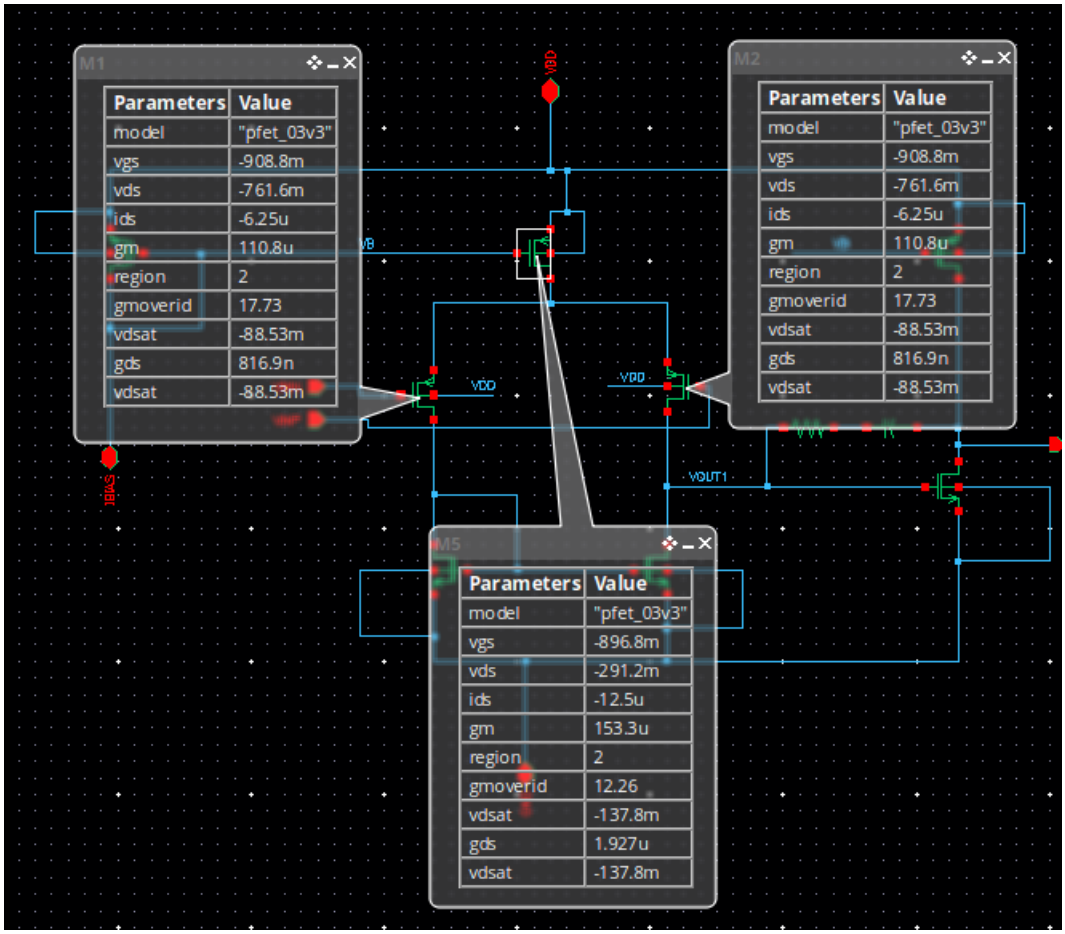
⇨ We should notice that current of the Tail is not 12.5uA so we need to sweep W to be increased to have current in tail is 12.5uA



⇨ We need W=17.14um

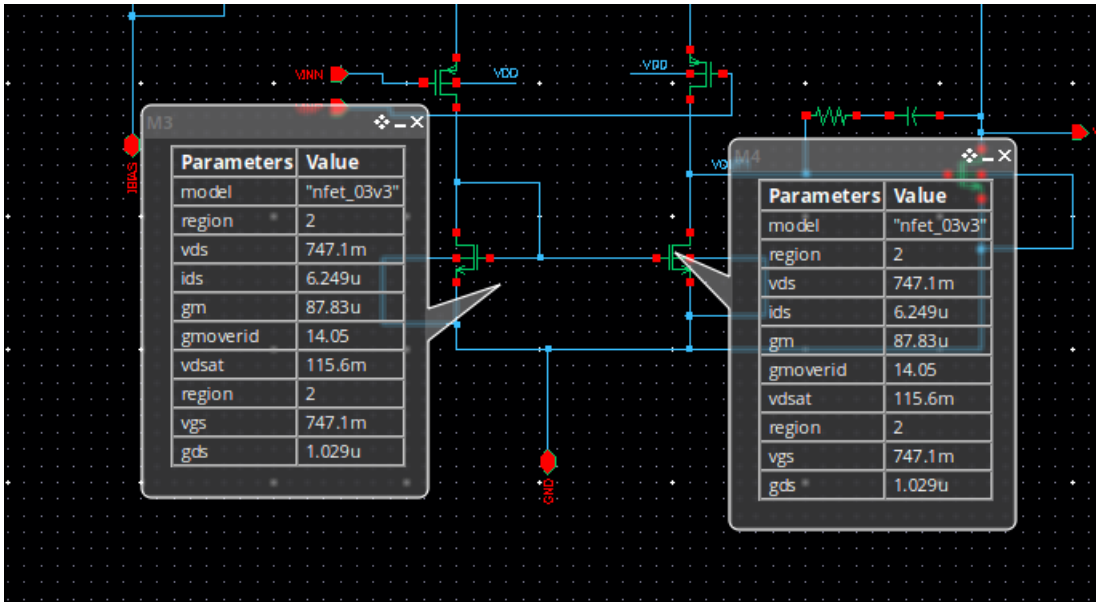
⇨ A better way to Design is to get the mirror parameters and use Multipliers

⇨ Results After sweeping:



⇨ **For the Active load:**

$\frac{gm}{id}$	12
gm	75uS
A_{V1}	63.187
ID	6.25uA
W	1.913um
L	400nm
V_{GS}	781.551m
gds	854.21nS
V_{DSAT}	137.3m
V_{OV}	88.4m
V^*	167.7m



⇨ We should notice the change between The results and the Design values after Tunning W of the input pair

We Tuned W of The current mirror load and not for CS stage ?

Latching The output to ground means that there is mismatch offset voltage between the two stages

Was negative as the CS entered the Triode which means that

$V_{GSCS} > V_{GSCM}$ as we see the one whose current is higher will enter Triode

This negative offset multiplied by the gain which latches the output to ground , as the VGS of the CS is determined by the DC output voltage of the First stage at Common mode so the output1 will follow the mirror node which is VGS of the mirror

$$V_{GS}\ of\ CS\ determined\ By\ V_{GS}\ of\ the\ current\ mirror\ load$$

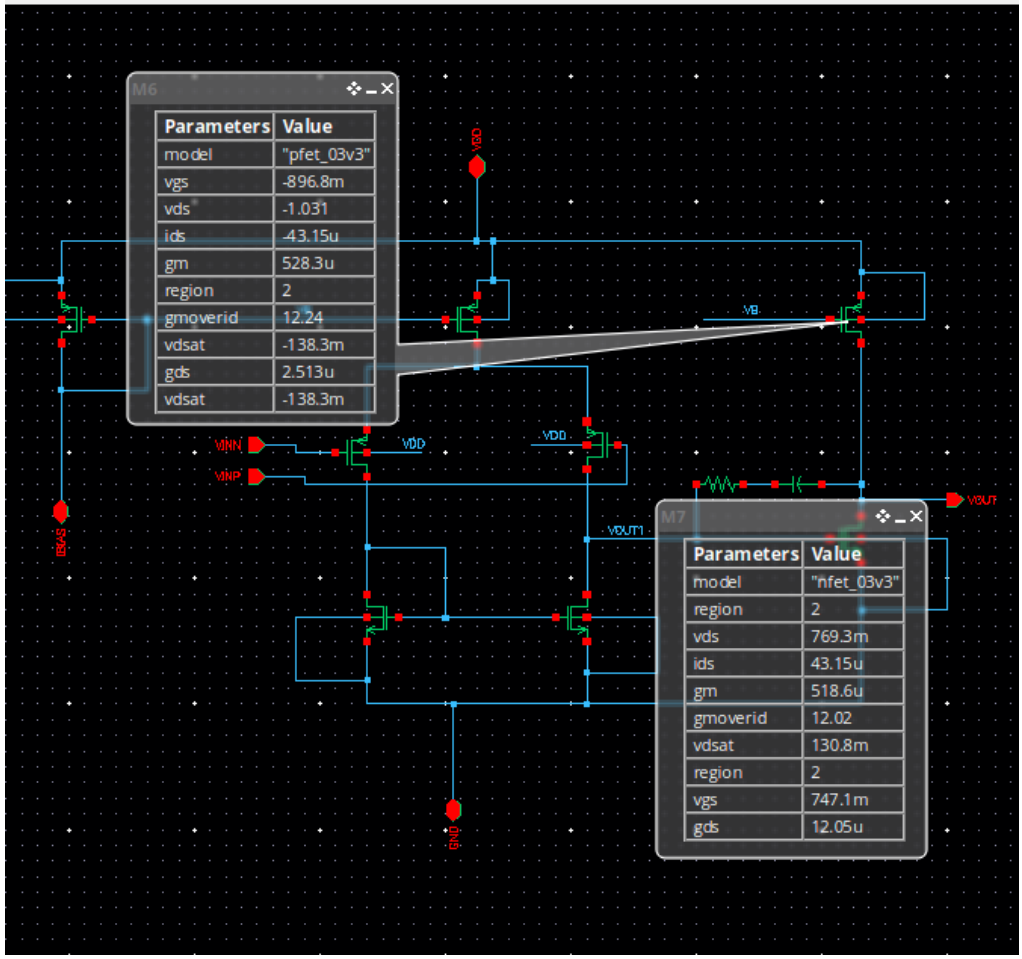
⇨ **Second stage :**

Tail CS:

$\frac{gm}{id}$	12
gm	540uS
A_{V1}	63.2
ID	45uA
W	55.71um
L	480nm
V_{GS}	898.664m
gds	2.898uS
V_{DSAT}	142.2m
V_{OV}	114.5m
V^*	167m

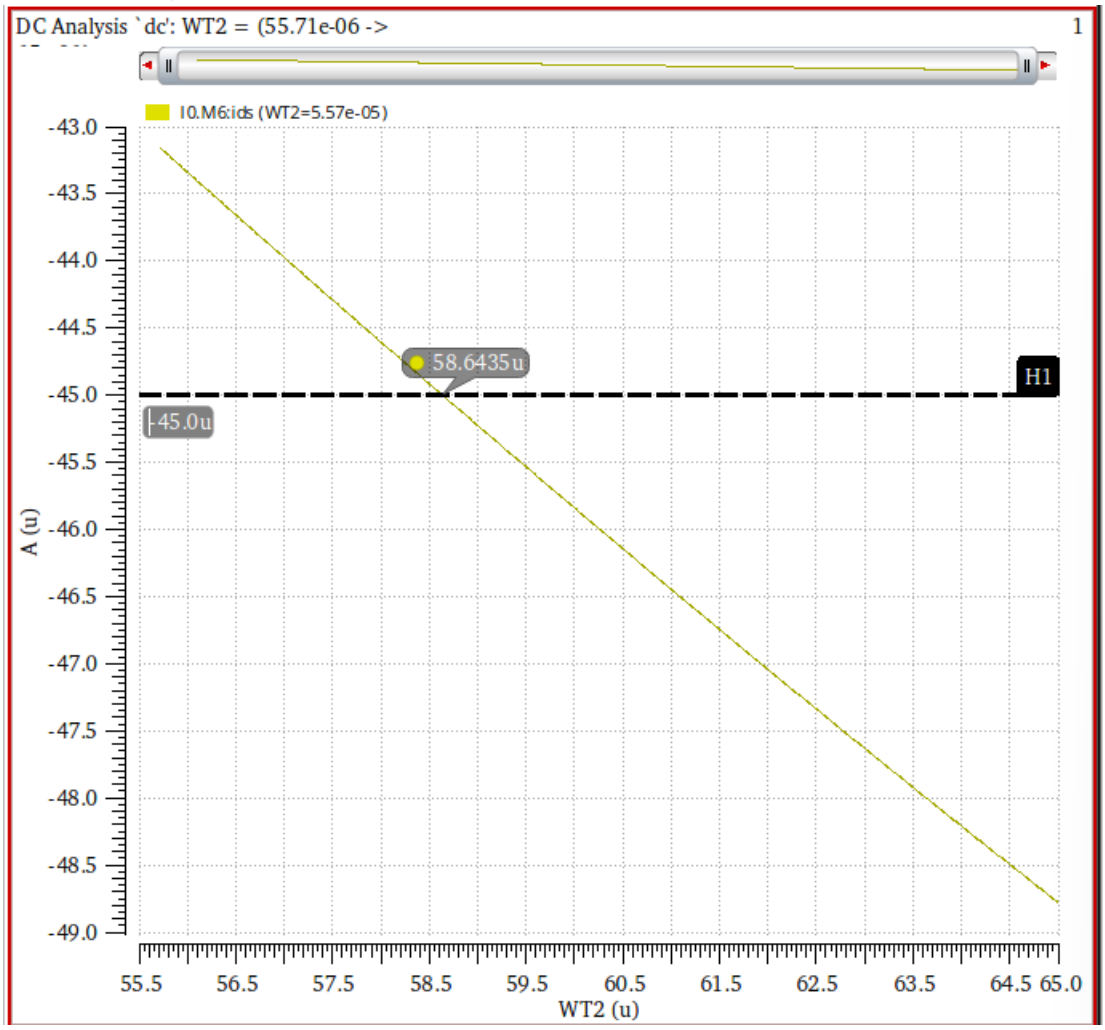
CS Input stage :

$\frac{gm}{id}$	12
gm	540uS
A_{V1}	78.7
ID	45uA
W	11.35um
L	320nm
V_{GS}	781.551m
gds	13.997uS
V_{DSAT}	129.9m
V_{OV}	117.95m
V^*	0.167



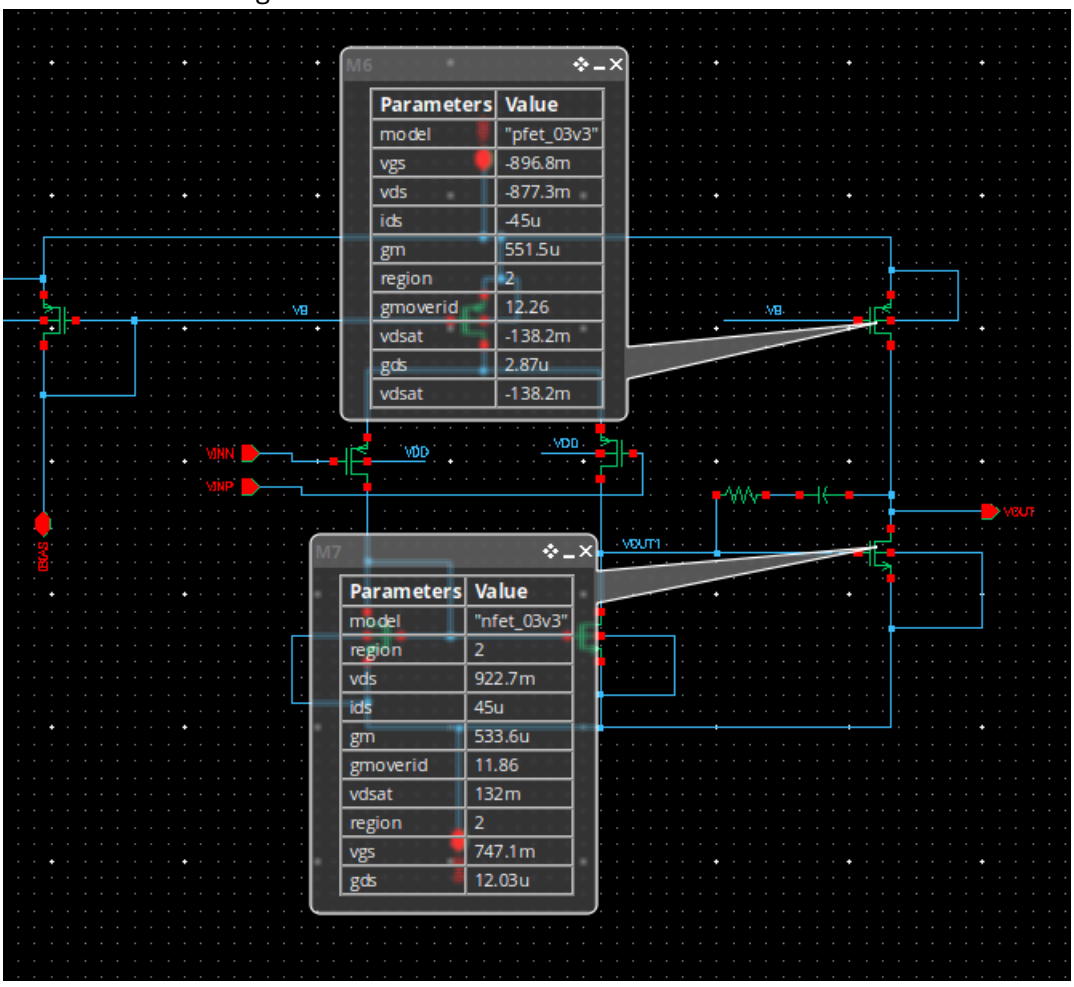
⇨ We should notice that The current of Second stage is less than 45uA

⇨ We can sweep W of the Active load to achieve current of 45uA



$$W = 58.64um$$

⇨ Results After Tunning :



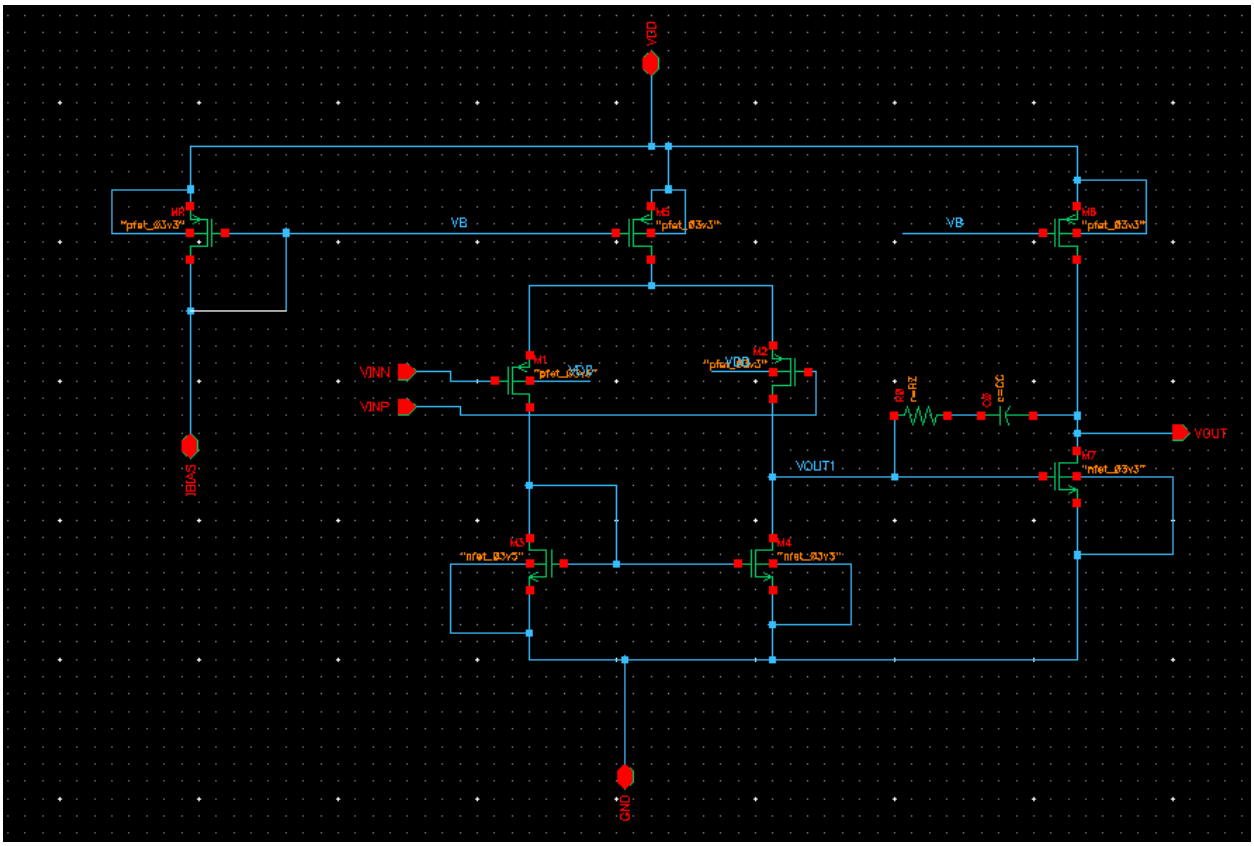
⇨ We can notice the improvement in VDS out closes to 900mv also gm results converged

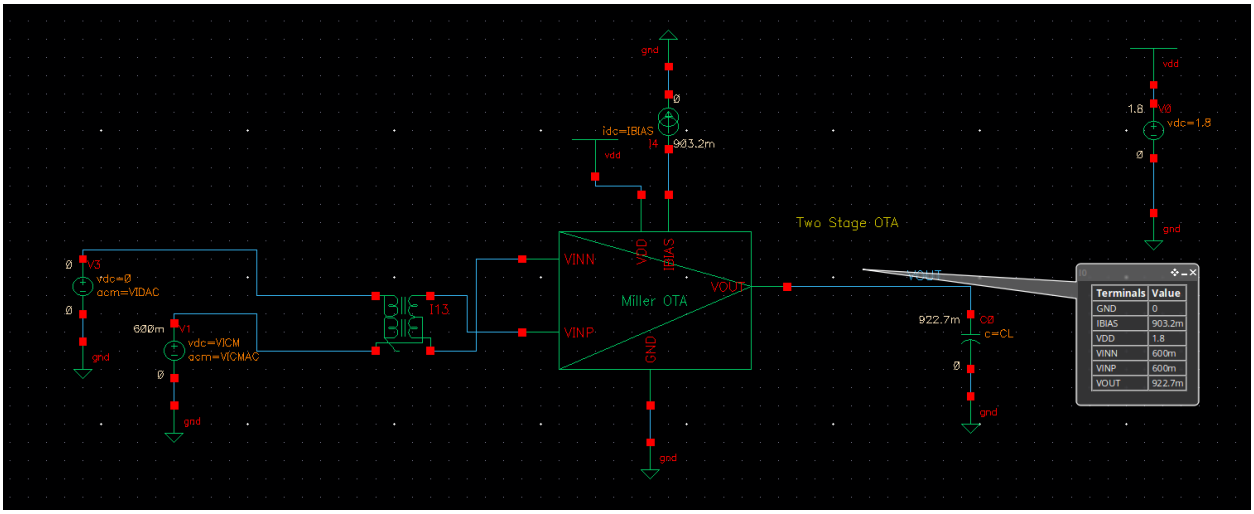
$$R_Z = \frac{1}{g_{m7}} = 1.874K\Omega$$

Open-loop OTA Simulations:

Schematic and DC-Bias point:

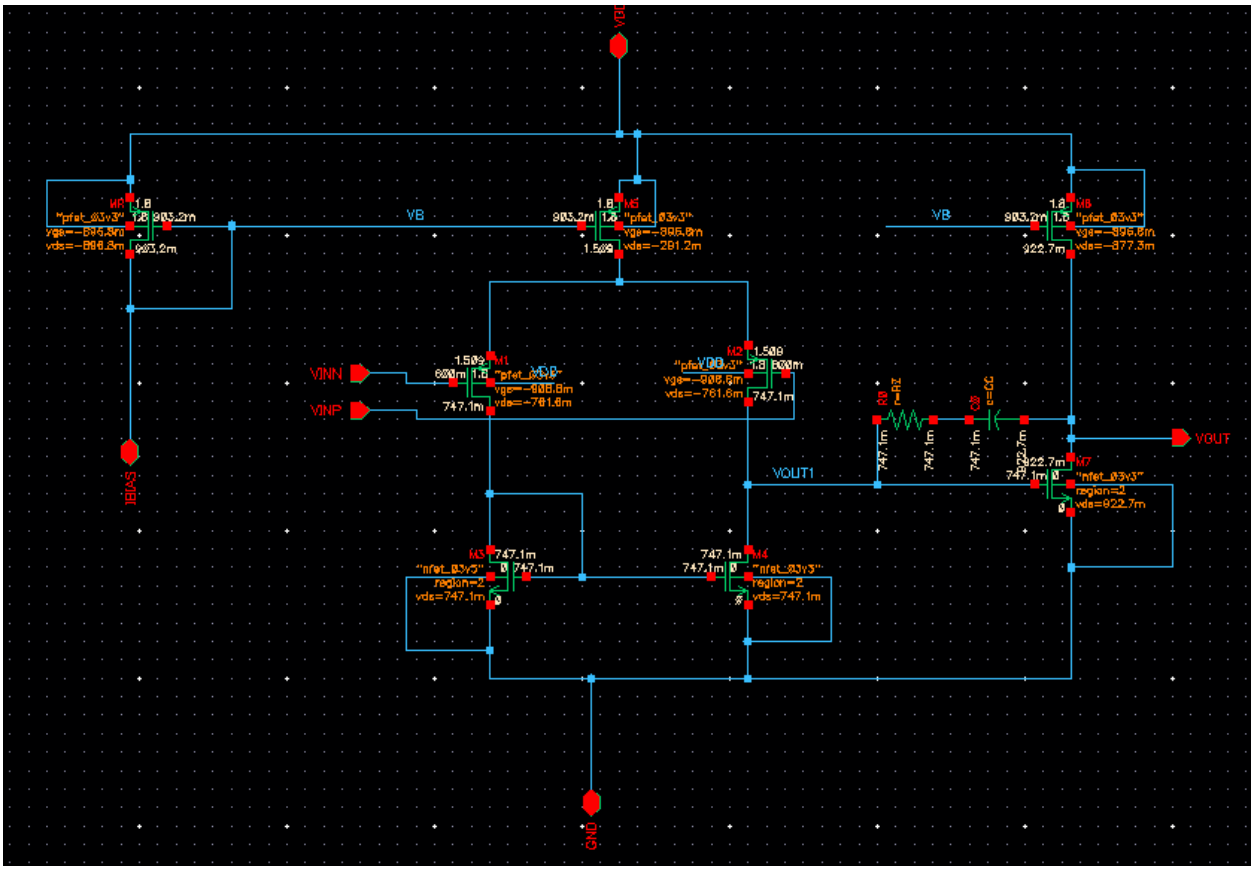
⇨ **Schematic**





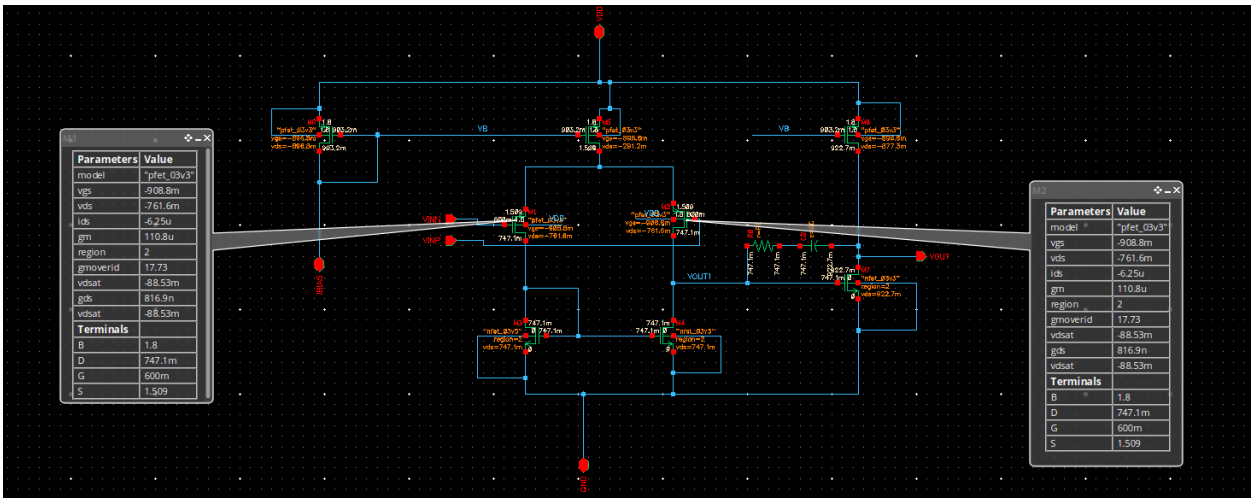
⇨ **Vout,dc=922.7mv**

⇨ **DC-Voltages Annotated :**



Is the current (and gm) in the input pair exactly equal?

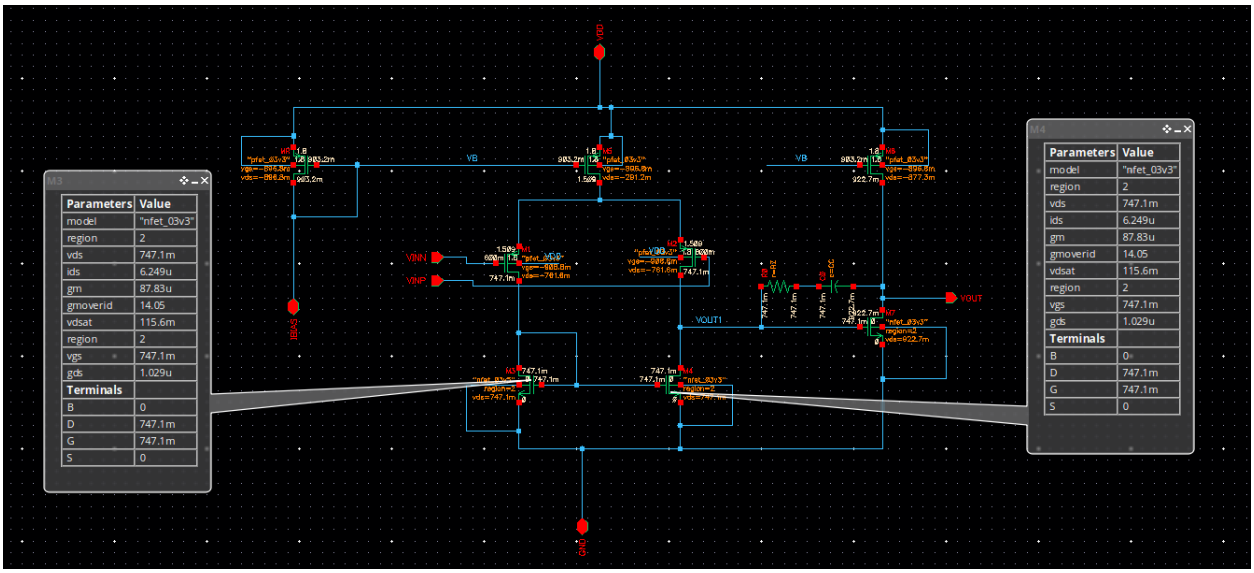
Yes, the currents and gm of input pair are exactly the same after the DC-point Debugging



What is DC voltage at the output of the first stage? Why?

$$V_{OUT1} = V_{GS3} = 747.1m$$

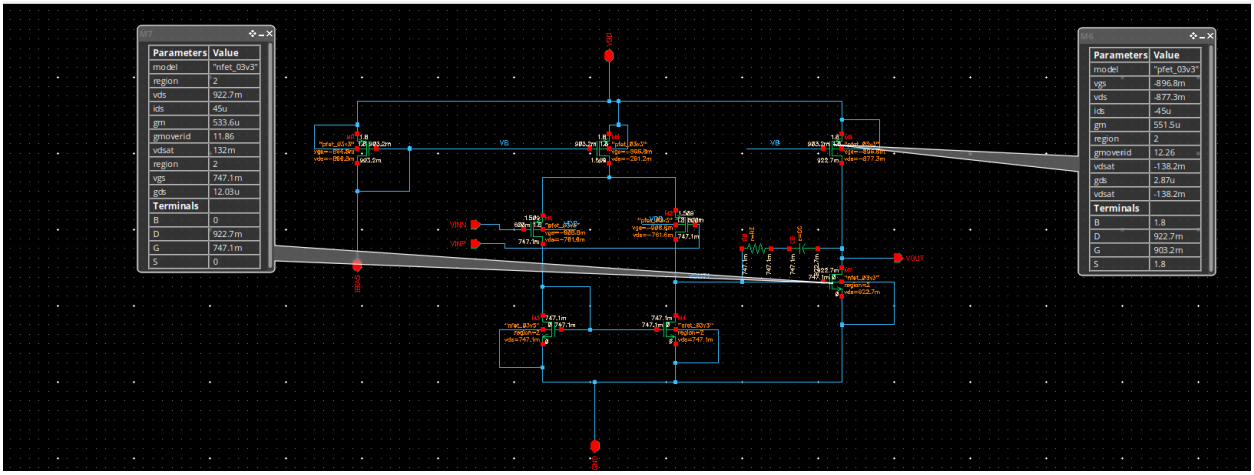
As at the common mode input V_{OUT1} follow the mirror node



What is DC voltage at the output of the second stage? Why?

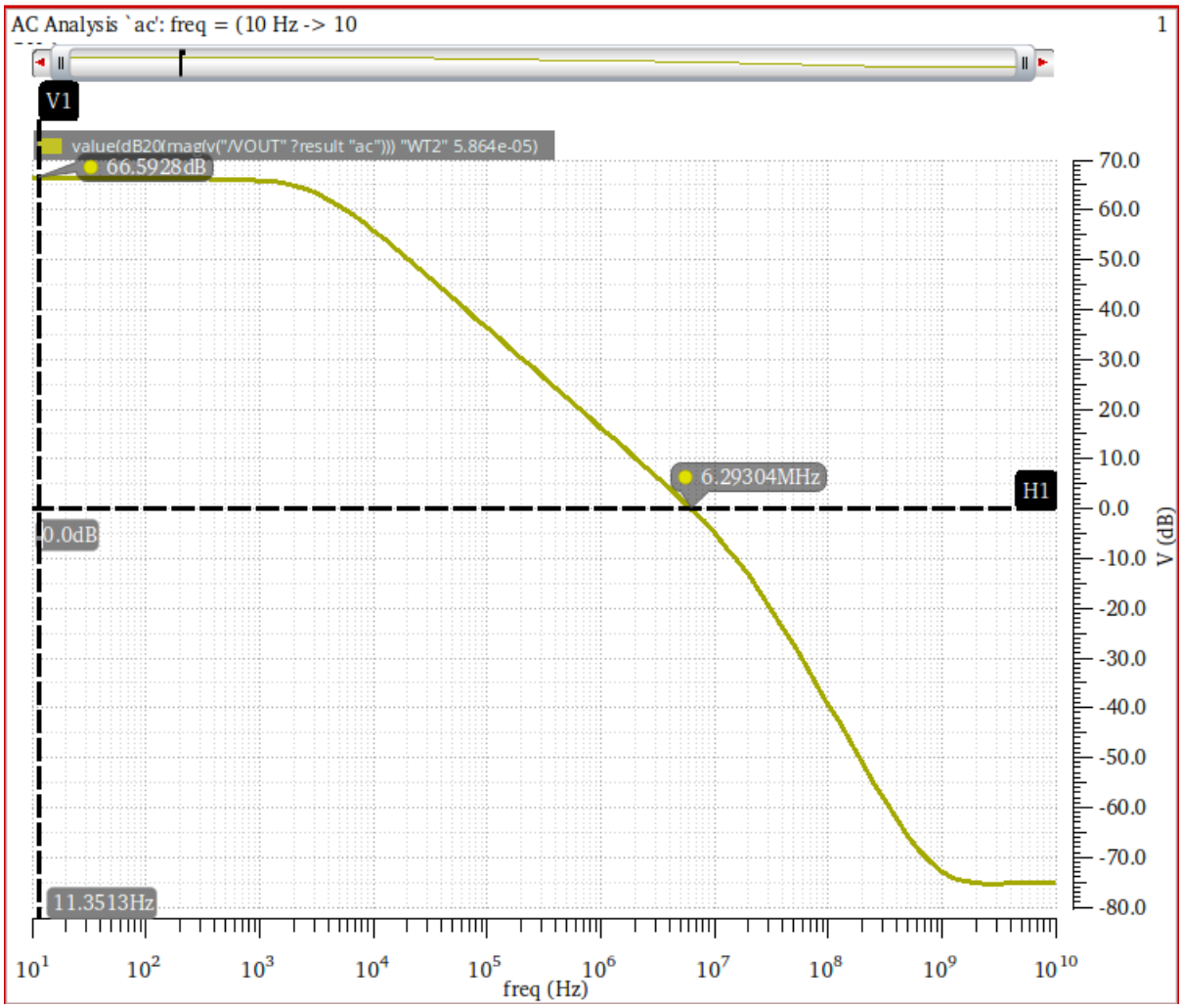
$$V_{OUT2} = V_{DS7} = 922.7m$$

As the Offset voltage between the two stages is zero , so V_{GS7} is determined by The first stage with the currents IB2 both define the Vout , it's designed to Maximize the swing and make it symmetrical



Diff small Signal ccs:

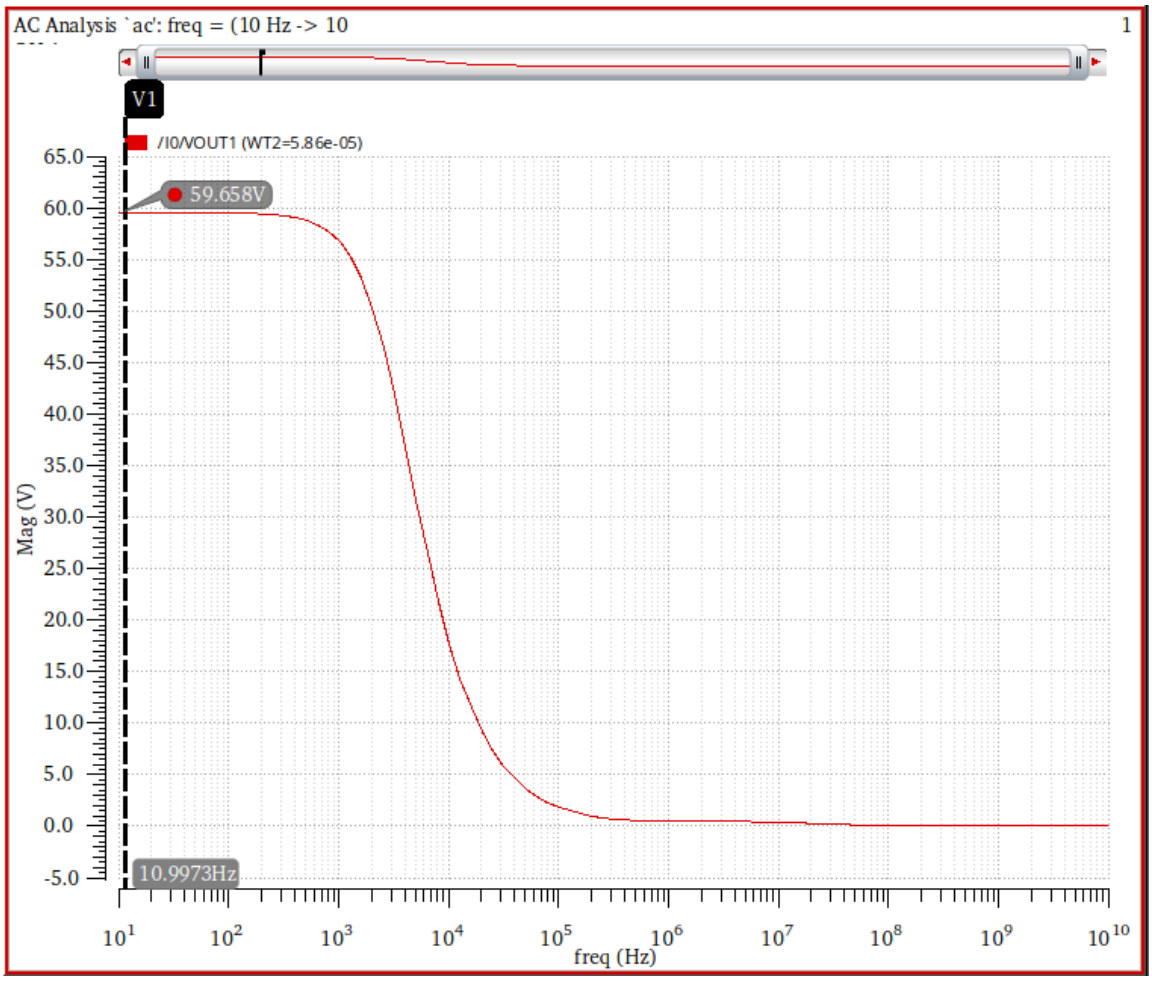
- **Diff gain in dB vs frequency :**



- **Results:**

5T_OTA:Two_stage_miller_Tb:1	AO	2.136k
5T_OTA:Two_stage_miller_Tb:1	AO_dB	66.59
5T_OTA:Two_stage_miller_Tb:1	BW	3.135k
5T_OTA:Two_stage_miller_Tb:1	UGF	6.295M
5T_OTA:Two_stage_miller_Tb:1	GBW	6.698M

⇨ **First stage gain Vs Second Stage gain:**



$$A_{V1} = 59.66\,, A_{V2} = 35.8$$

⇨ **Hand Analysis :**

$$A_{Vd} = [(gm_{1,2} + g_{mb}) * (r_{o1}||r_{o2})] * [(gm_6 * (r_{o6}||r_{o7}))]$$

$$A_{Vd} = 60.025 * 35.812 = 2.149K$$

$$R_{out1} = 541.741K\Omega\,, R_{out2} = 67.114K\Omega$$

$$f_{p1} = \frac{1}{R_{out1} * 2 * \pi * (Gm_2 * R_{out2}) * C_c} = 3.281K\text{Hz}$$

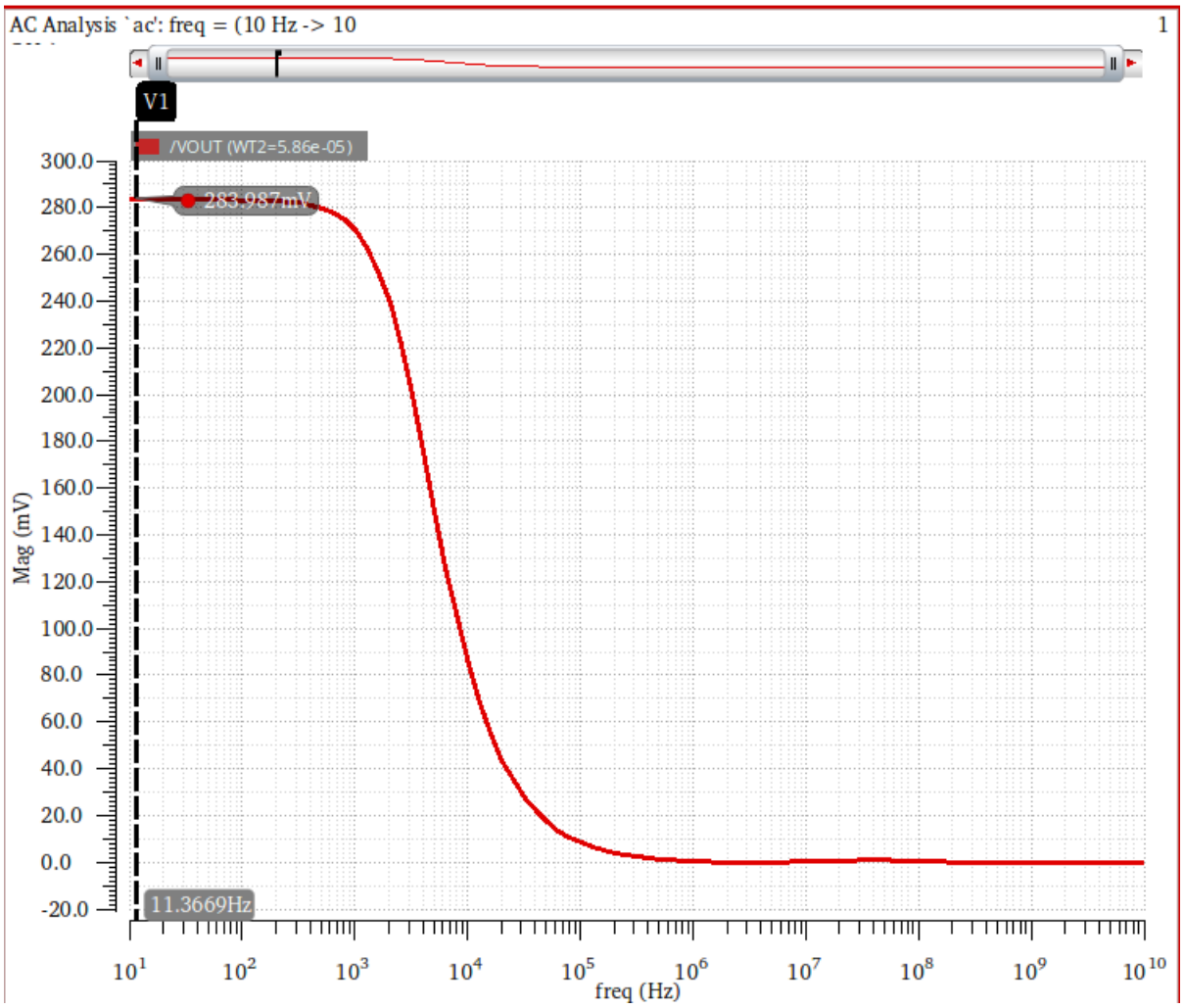
$$GBW = 7.05MHz$$

⇨ **Compare Hand Analysis with Simulation Results:**

	GBW	f_{p1}	A_{Vd}
Hand Analysis	**7.05MHz**	**3.281KHz**	**2.149K**
Simulation	**6.698MHz**	**3.135KHz**	**2.136K**

CM Small signal CCS:

⇨ ***CM gain in dB vs Frequency*** **:**



⇨ **Hand Analysis:**

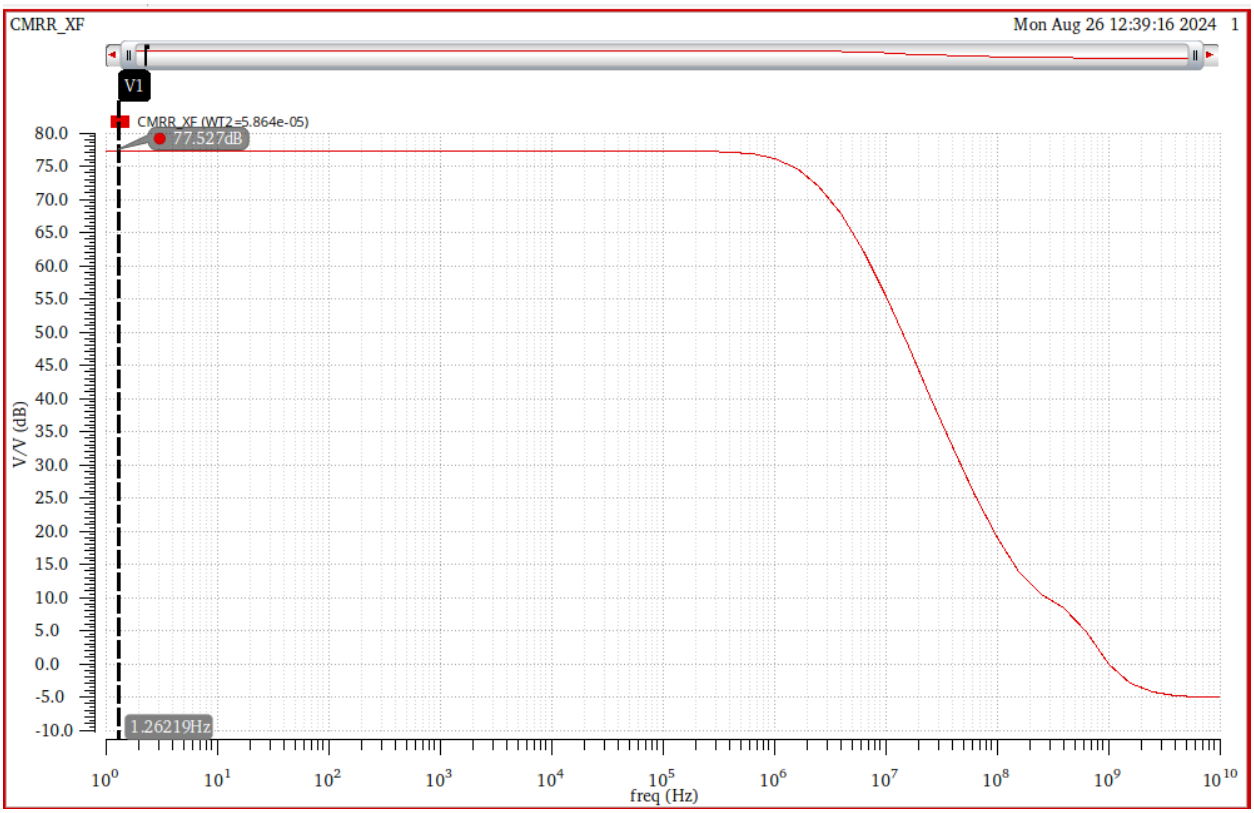
$$A_{VCM} = \frac{1}{2 * g_{m34} * r_{o5}} * g_{m7} * (r_{o6} || r_{o7}) = 392.72m$$

⇨ **Comparison Between Hand Analysis and Simulation Results:**

	A_{Vcm}
Hand Analysis	**392.72m**
Simulation	**283.987m**

CMRR:

CMRR Vs frequency :



Hand Analysis:

$$CMRR = \frac{A_{VdSystem}}{A_{VcmSystem}} = \frac{[gm_{1,2} * (r_{o1}||r_{o2})] * [(gm_6 * (r_{o6}||r_{o7}))]}{[[2 * gm_{34} * R_{ss}]]^{-1} * [(gm_6 * (r_{o6}||r_{o7}))]}$$
$$= g_{m1,2} * (r_{o1}||r_{o2}) * 2 * g_{m3,4} * r_{o5}$$

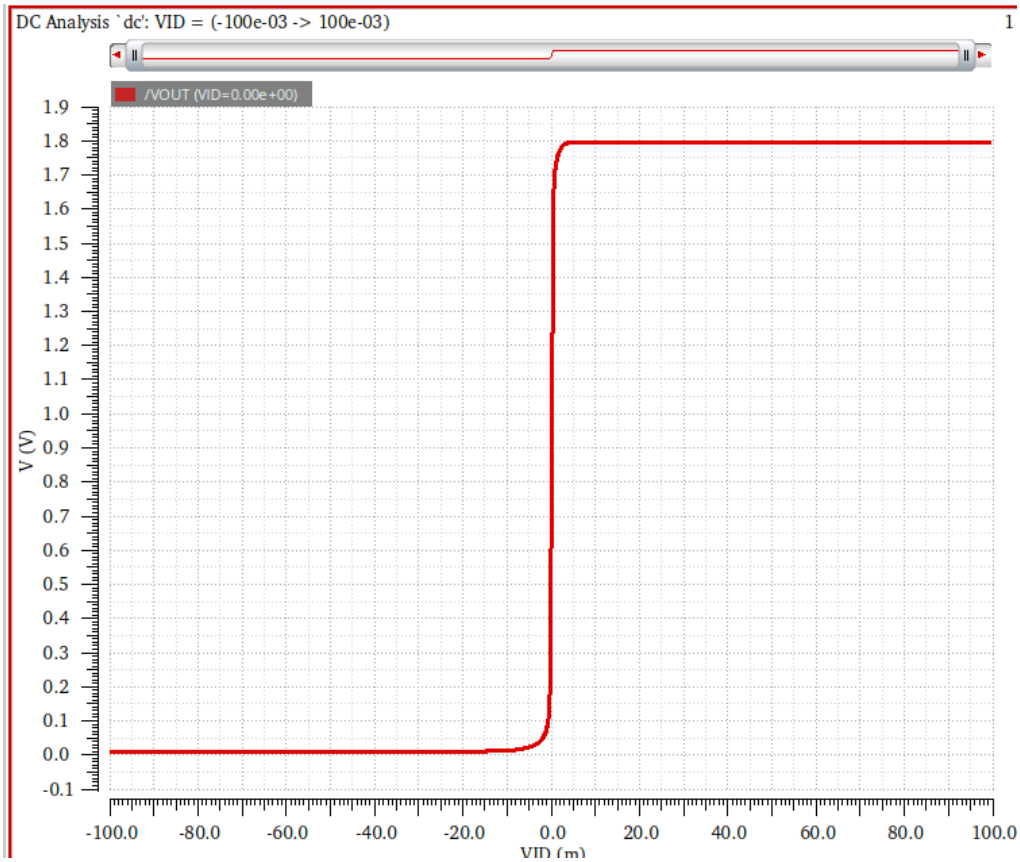
$$CMRR = 5438.552 = 74.71dB$$

Comparison Between Hand Analysis and Simulation:

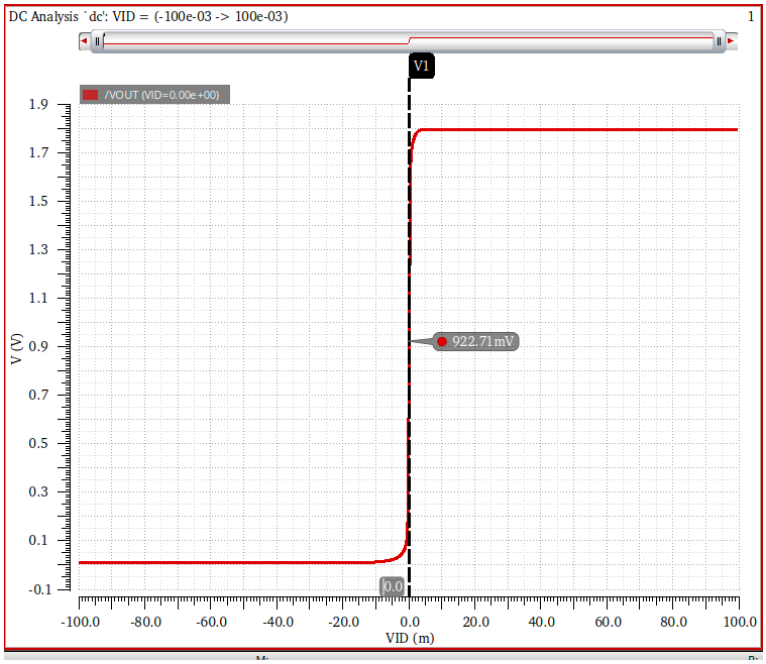
	$CMRR$
Hand Analysis	**74.71dB**
Simulation	**77.53dB**

Diff large signal CCS:

⇨ VOUT VS VID:



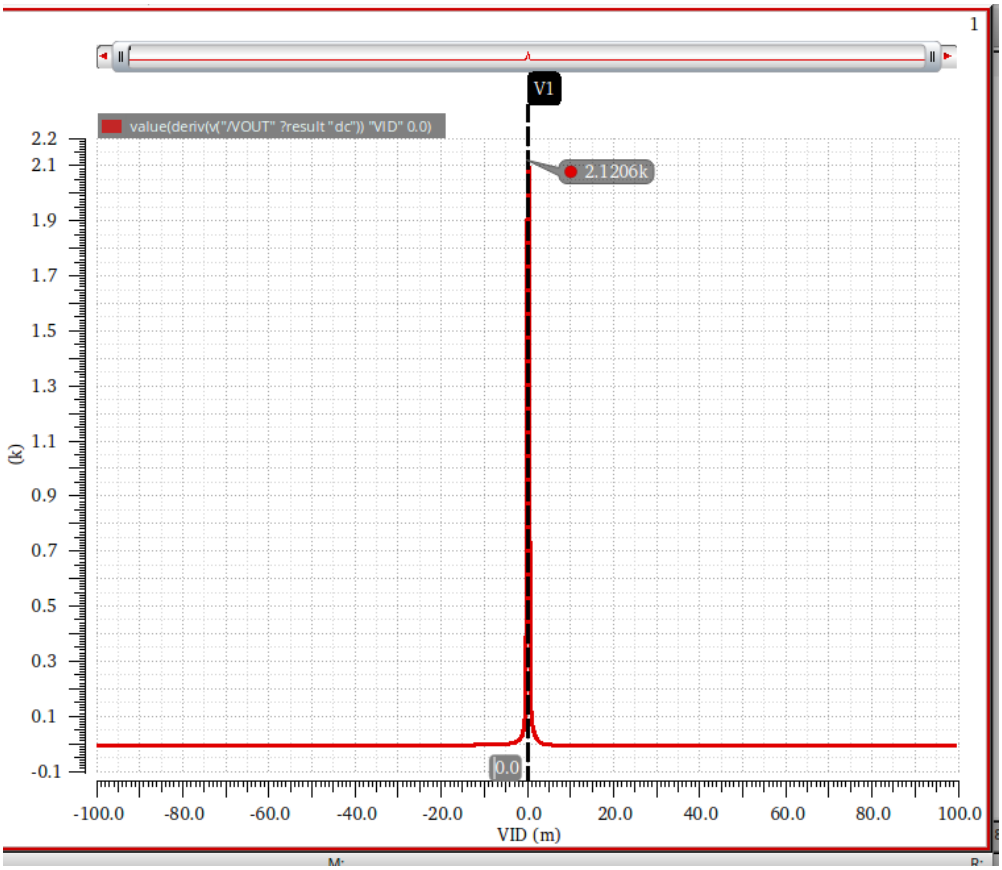
⇨ Value @ VID=0



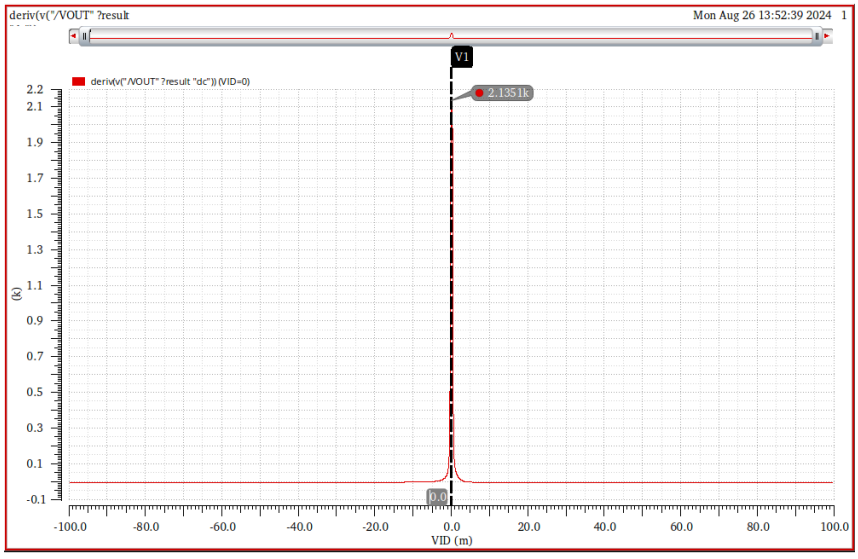
The value @ VID=0 is the DC output Voltage

Vout @ VID=0	$V_{OUT_{dc}}$
922.71mV	922.7mV

⇨ **Deriv of Vout Vs VID:** With step size =0.1m



⇨ With step size = 0.01m



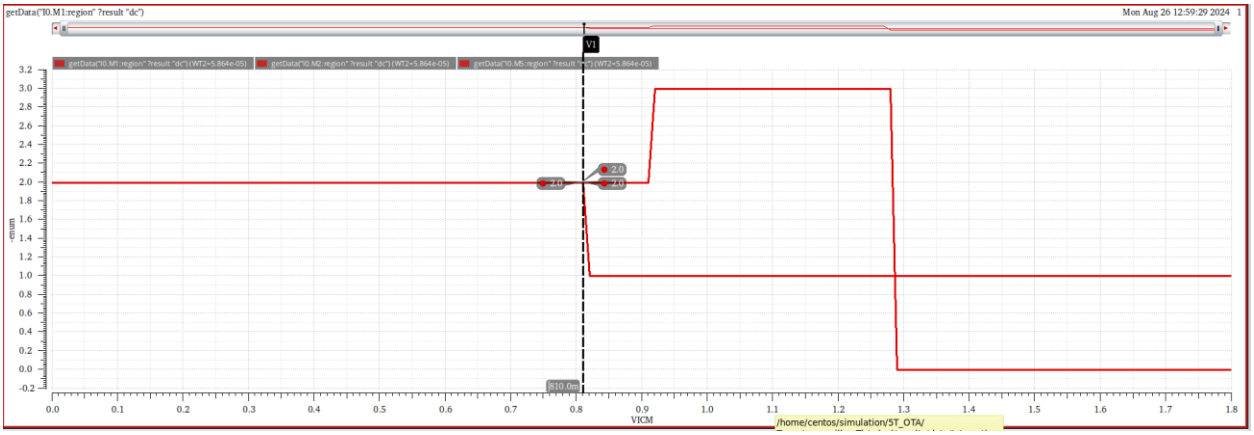
Is the peak less than the value of Avd obtained from ac analysis ?

Yes , the peak is less than the A_{vd} obtained from the ac analysis due to simulation accuracy and as the step size decreases , the gain converges to the gain obtained from ac analysis.

⇨ **Ac analysis uses linear models so it gives results from the linearized Model**

CM Large signal CCS:

Region parameter plotted:



- ⇨ CMIR: 0.2 V to 0.81 V
- ⇨ **Hand Analysis:**

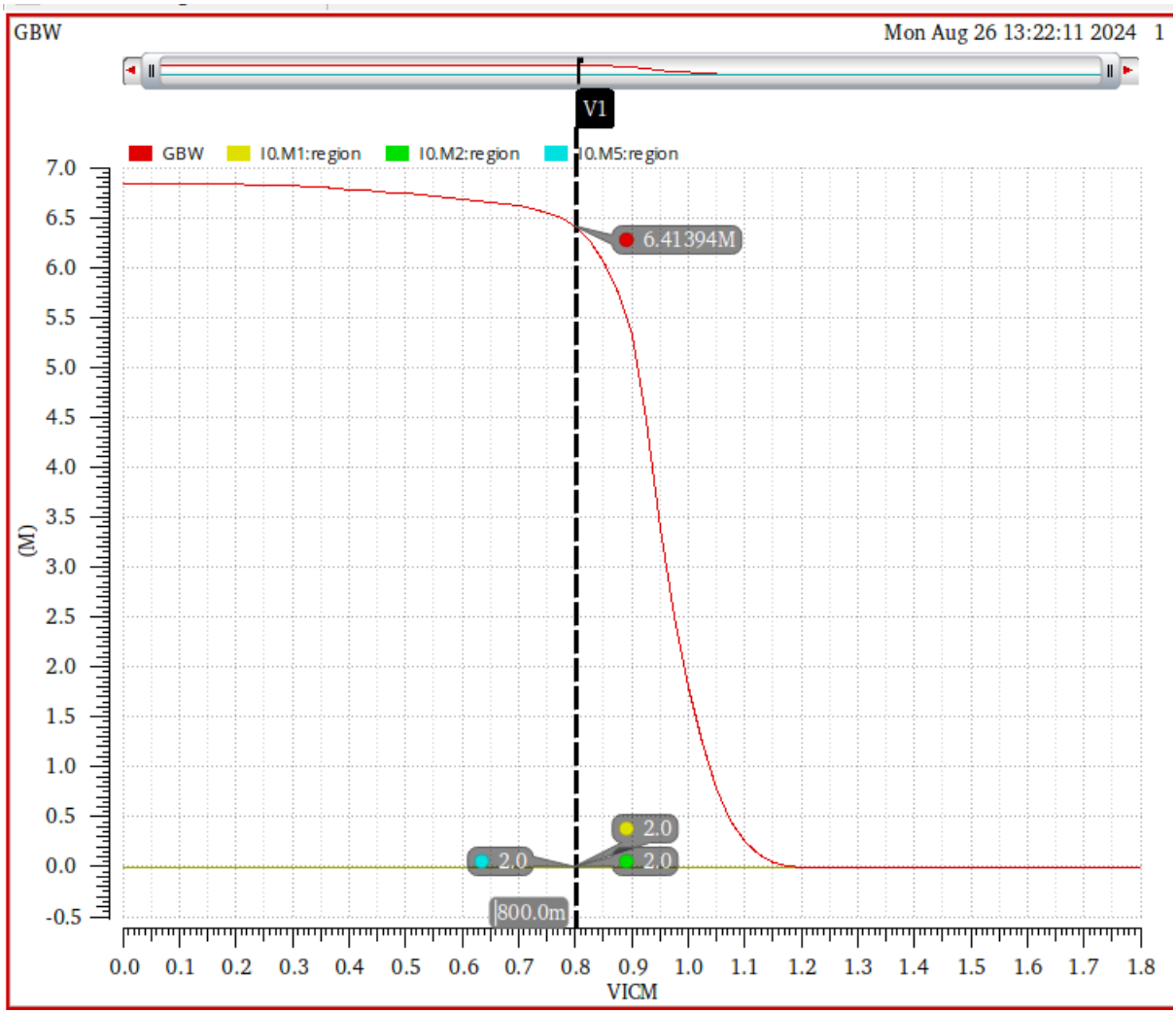
Assume $V_{incmH} = 0.75V$, $V_{GS1} = 1.8 - 0.2 - 0.75 = 850mv$

CMIR: 0.2V TO 0.75V

- ⇨ **Compare the analysis with Simulation Results:**

	CMIR Low	CMIR High
Hand Analysis	0.2V	0.75V
Simulation	< 0 V	0.81V

GBW Vs VICM:



⇨ CMIR: 0V TO 0.8V

If you are using PMOS input pair, body effect may cause CMIR to extend till GND (why?)

For Pmos Input pair

$$V_{INCM} \geq V_{SGMirror} - V_{th}, V_{INCM} \geq V_{ov} - 2 * V_{th}$$

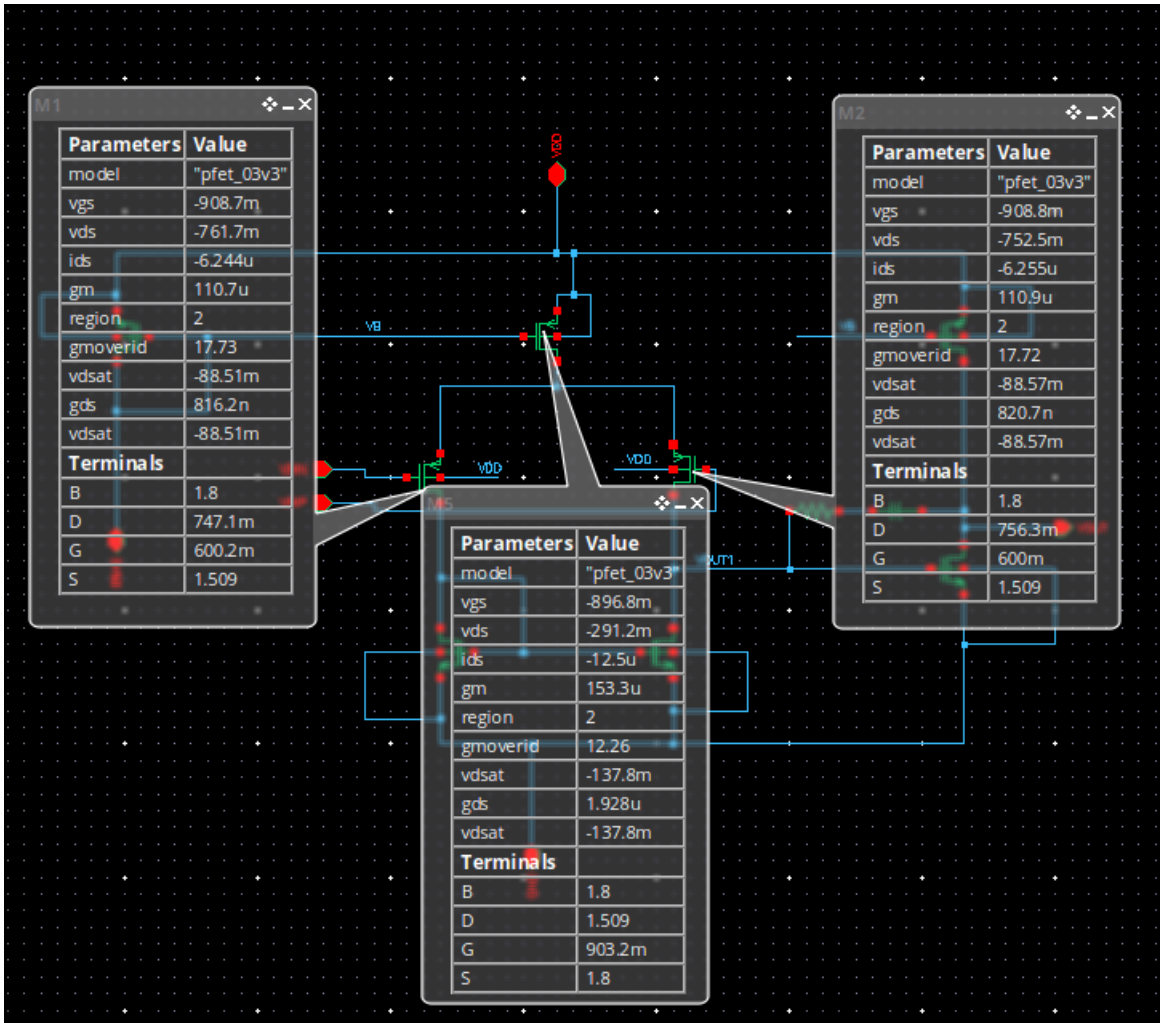
Body effect may causes V_{th} to be greater than 2*$V_{OV}(V^*)$ So the minimum range may extend to ground even more may accept negative range

Closed Loop simulation:

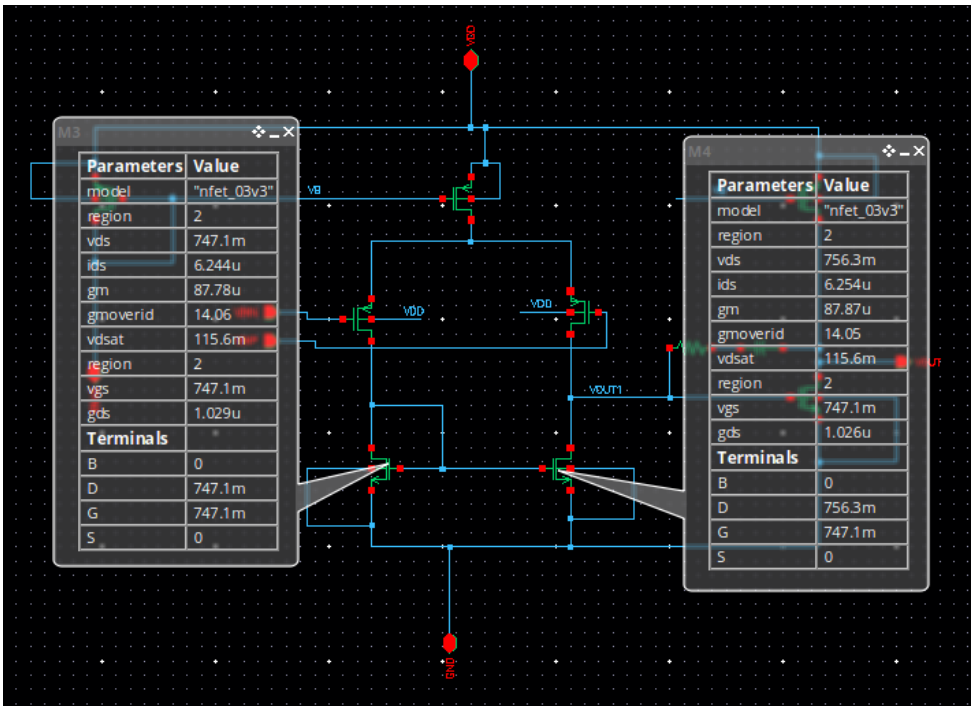
- ⇨ Closing the loop changes the Operation of The circuit

OP Results Debugging:

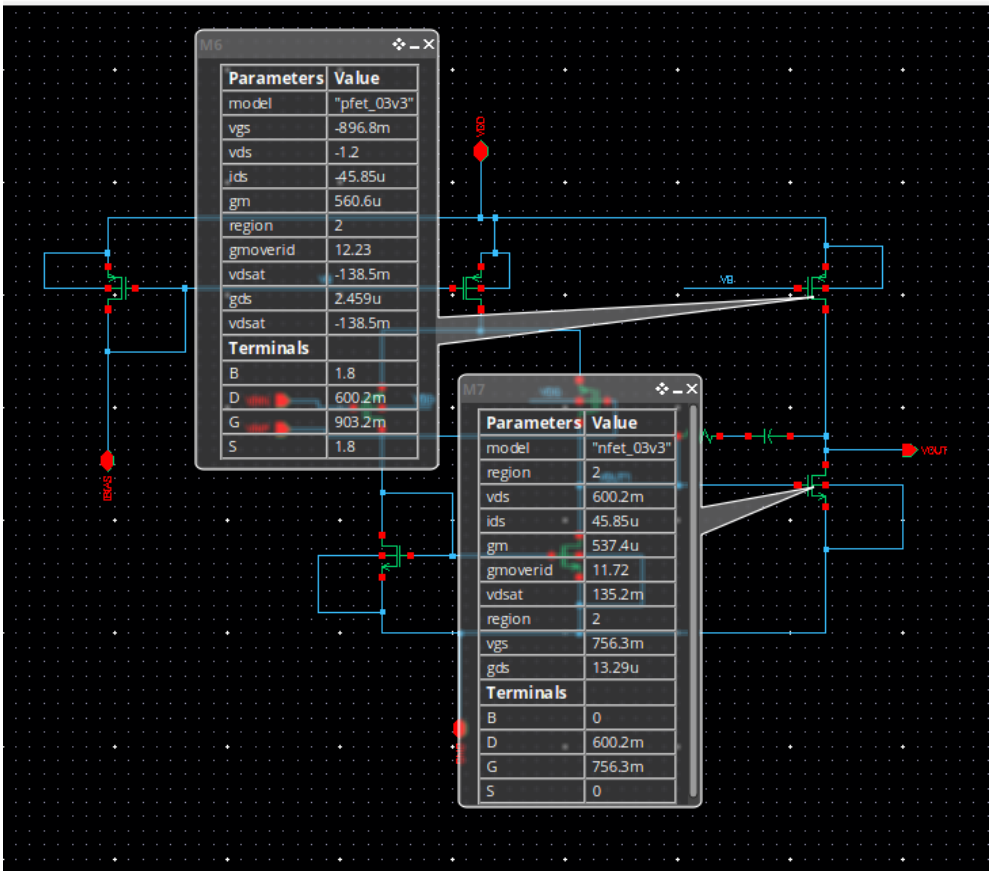
- ⇨ For input Pair and Tail CS:



⇨ For the Current Mirror load:



⇨ For The second stage :



Are the DC voltages at the input terminals of the op-amp exactly equal? Why?

$$V_{IN}^{-} = V_G^{-} = 600.2mv$$

$$V_{IN}^{+} = V_G^{+} = 600mv$$

No , there is error signal between the input pair

$$V_{err} = |V^{-} - V^{+}| = 0.2mv$$

This error voltage due to the mismatch between the two halves furthermore the feedback operation changes the open loop where the open loop gain is finite not ideal

Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?

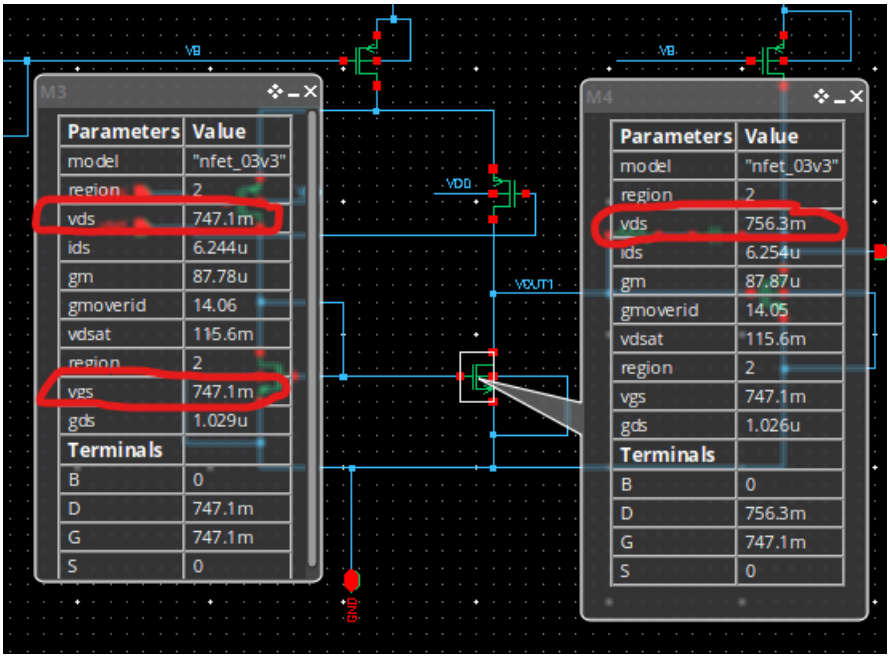
No,

$$V_{OUT1} = V_{DS4} = 756.3mv$$

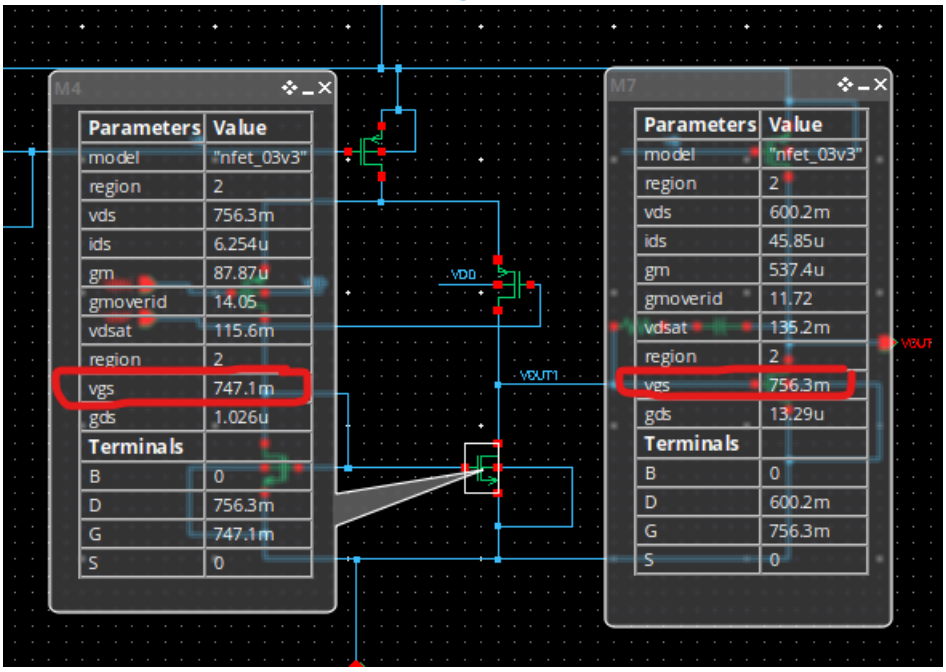
For the open loop it was

$$V_{OUT1_{OL}} = 747.1mv$$

As the feedback introduces mismatch between the two pairs so the V_{OUT1} Doesn't follow the mirror node as in OL which made $V_{GS3} \neq V_{DS4}$



⇨ **This mismatch causes offset voltage to increases :**

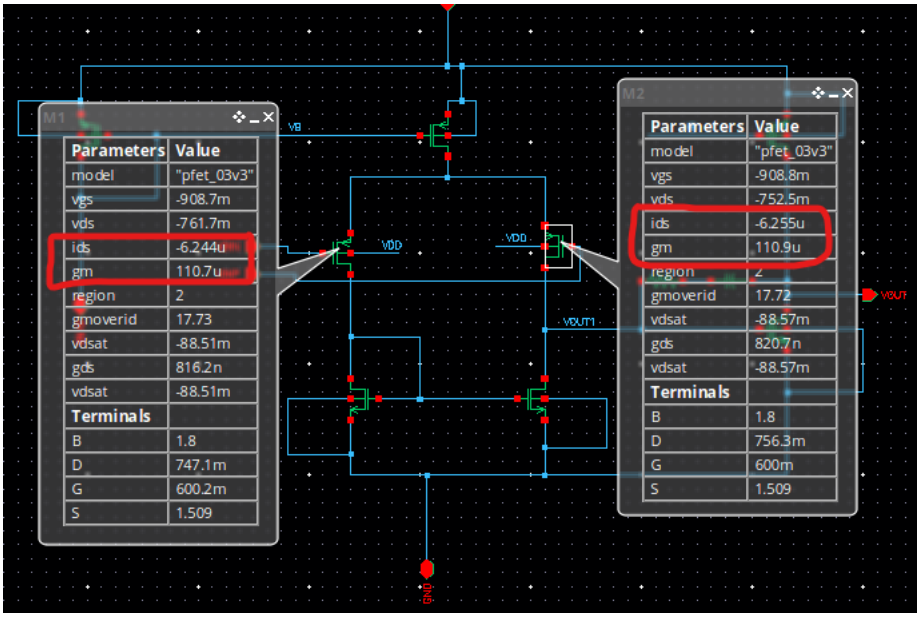


Is the current (and gm) in the input pair exactly equal? Why?

No, there is mismatch between the pair in gm introduced by the feedback which changes M1 than M2

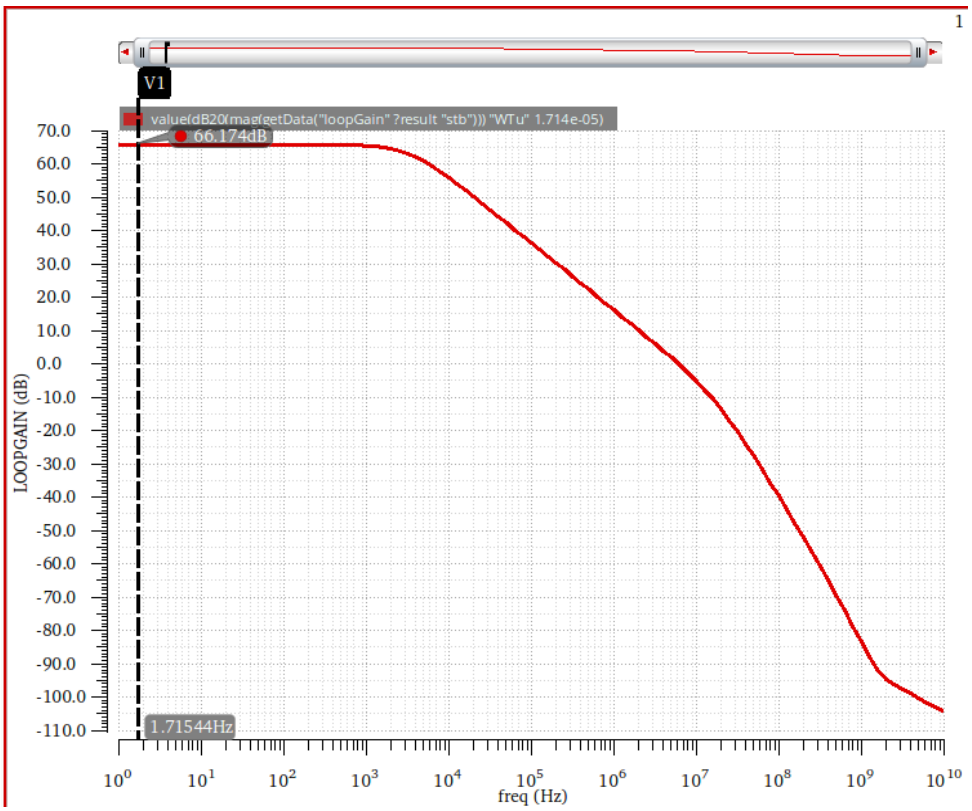
$$\delta g_m = 110.9 - 110.7 = 0.2uS$$

$$\delta I_d = 6.255 - 6.244 = 0.011uS$$

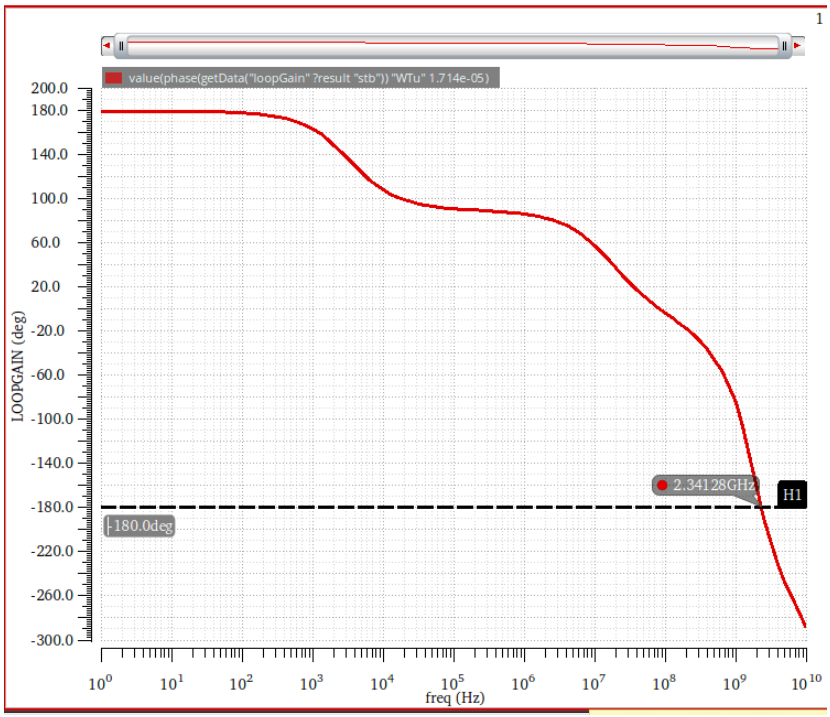


Loop Gain:

- **Loop Gain in dB:**



- **Phase Vs frequency :**



⇨ **DC-gain, fu, GBW for Open loop and Closed Loop:**

⇨ **Closed LOOP Parameters:**

Test	Output	Nominal
5T_OTA:Two_stage_miller_TbCL:1	LGo	2.036k
5T_OTA:Two_stage_miller_TbCL:1	LG_dB	66.17
5T_OTA:Two_stage_miller_TbCL:1	bwcl	9.507M
5T_OTA:Two_stage_miller_TbCL:1	UGFLG	6.291M
5T_OTA:Two_stage_miller_TbCL:1	BWLG	3.293k
5T_OTA:Two_stage_miller_TbCL:1	GBWLG	6.703M

⇨ **Open Loop Parameters:**

5T_OTA:Two_stage_miller_Tb:1	AO	2.136k
5T_OTA:Two_stage_miller_Tb:1	AO_dB	66.59
5T_OTA:Two_stage_miller_Tb:1	BW	3.135k
5T_OTA:Two_stage_miller_Tb:1	UGF	6.295M
5T_OTA:Two_stage_miller_Tb:1	GBW	6.698M

Observations:

1- **The DC-gain decreased as the loop closed due to the mismatch in input pair**
2- **BW of the loop gain increases slightly to Keep same GBW constant as $\beta = 1$**

⇨ **Phase Margin :**

Test	Output	Nominal
5T_OTA:Two_stage_miller_TbCL:1	PM	68.85

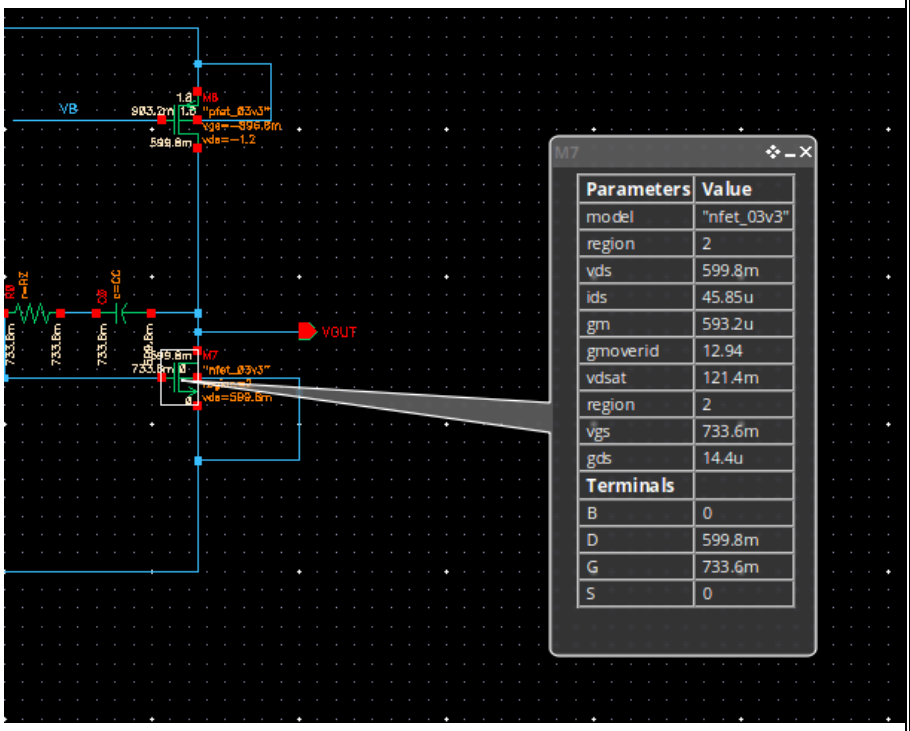
- Phase margin is lower than 70° so we can increase W of the Common source to increase the Phase margin a little
- $\omega_{p1} = \frac{1}{R_{out1}*(Gm_2*R_{out2})*C_c}$
- $\omega_{p2} = \frac{G_{m2}}{C_L+C_{int}}$

Increasing gm2 will causes pole splitting which will improve PM , we can increases gm2 by increasing the W of the Common source

After Modifying W we need to get the new gm and put the new zero at infinity

$$W = 11.35um \rightarrow 15um$$

⇨ **After modification The common source**



PM=70.39°

5T_OTA:Two_stage_miller_TbCL:1	PM	70.39
5T_OTA:Two_stage_miller_TbCL:1	LGo	2.098k
5T_OTA:Two_stage_miller_TbCL:1	LG_dB	66.44
5T_OTA:Two_stage_miller_TbCL:1	bwcl	9.403M
5T_OTA:Two_stage_miller_TbCL:1	UGFLG	6.357M
5T_OTA:Two_stage_miller_TbCL:1	BWLG	3.19k
5T_OTA:Two_stage_miller_TbCL:1	GBWLG	6.693M
5T_OTA:Two_stage_miller_TbCL:1	mag(getData("loopGain" ?result ...	

⇨ **Hand Calculations :**

$$\boldsymbol{PM = 90 - tan^{-1}\left(\frac{\omega_u}{\omega_{p2}}\right) = 90}$$

$$\boldsymbol{\omega_{p2} = \frac{g_{m7}}{C_L} = \frac{593.2M}{5P} = 118.64\frac{Mr}{s}}$$

$$\boldsymbol{PM = 70.48}$$

$$\boldsymbol{LG_o = \beta A_{OL} = 1 * [(gm_{1,2} + g_{mb}) * (r_{o1}||r_{o2})] * [(gm_6 * (r_{o6}||r_{o7}))] = 2.047K}$$

$$f_{p1} = \frac{1}{R_{out1} * 2 * \pi * (Gm_2 * R_{out2}) * C_c} = 3.443K\text{Hz}$$

$$\boldsymbol{f_{pcl} = (1 + \beta * A_{ol}) * f_{p1} = 7.051MHz}$$

$$UGF = LG_o * BW_{LGo} = 7.045MHz$$

⇨ **Comparison between Hand Calculations And Simulation results:**

	PM	UGF	LGo	BWLG
Hand Analysis	$70.5°$	**7.051MHz**	**2.047K**	**7MHz**
Simulation	$70.4°$	**6.291MHz**	**2.039K**	**6.301MHz**

⇨ **Comments:**

There is small difference between the Hand Analysis due to assuming that the phase @ ω_{p1} Is exactly 90°

Slew Rate:

$$S_R = \frac{I_{B1}}{C_C}$$

5T_OTA:Two_stage_miller_TbCL:1	SR	4.189M	

⇨ Low SR , we need to increase the current of the first stage a little to improve the SR so we will try to increase the W of the Tail Current source of the First stage without violating the Current Budget Spec

$$W = 17.64um$$

Cannot be increased more than this to keep PM>70

We can decreases Cc by a factor and increase the gm2 by the same factor to keep PM and increase SR

5T_OTA:Two_stage_miller_TbCL:1	SR	4.744M

After Modifications we need to check the specs :

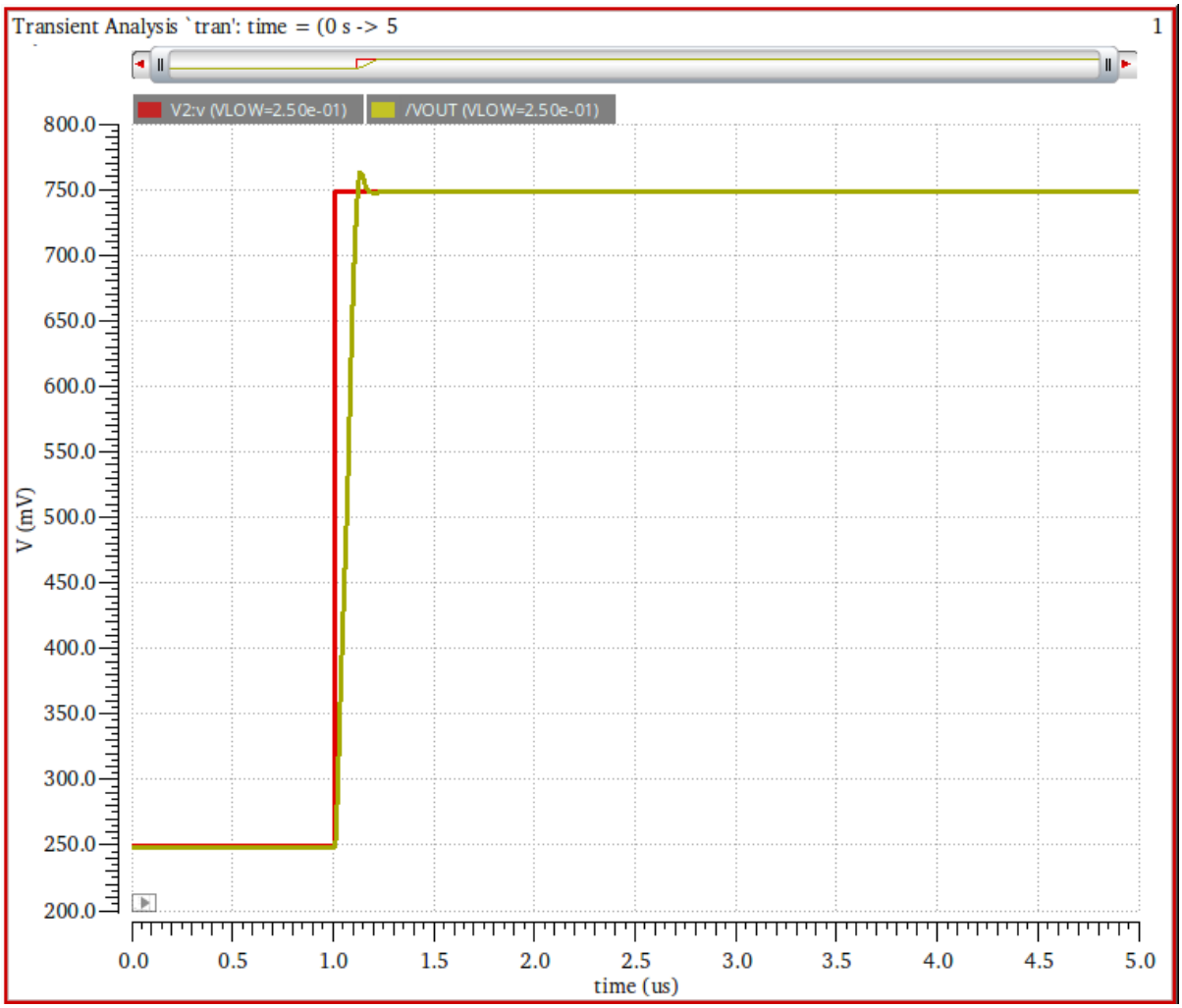
Test	Output	Nominal
5T_OTA:Two_stage_miller_TbCL:1	PM	70.33
5T_OTA:Two_stage_miller_TbCL:1	LGo	2.139k
5T_OTA:Two_stage_miller_TbCL:1	LG_dB	66.61
5T_OTA:Two_stage_miller_TbCL:1	bwd	10.46M
5T_OTA:Two_stage_miller_TbCL:1	UGFLG	7.173M
5T_OTA:Two_stage_miller_TbCL:1	BWLG	3.514k
5T_OTA:Two_stage_miller_TbCL:1	GBWLG	7.517M

- ⇨ We can fine Tune For lower GBW by decreasing the W of the input pair to be 20um
- ⇨ After this Tune we could decrease Cc to achieve higher SR
- ⇨ **After This tuning the final results will be :**

5T_OTA:Two_stage_miller_TbCL:1	SR	4.908M

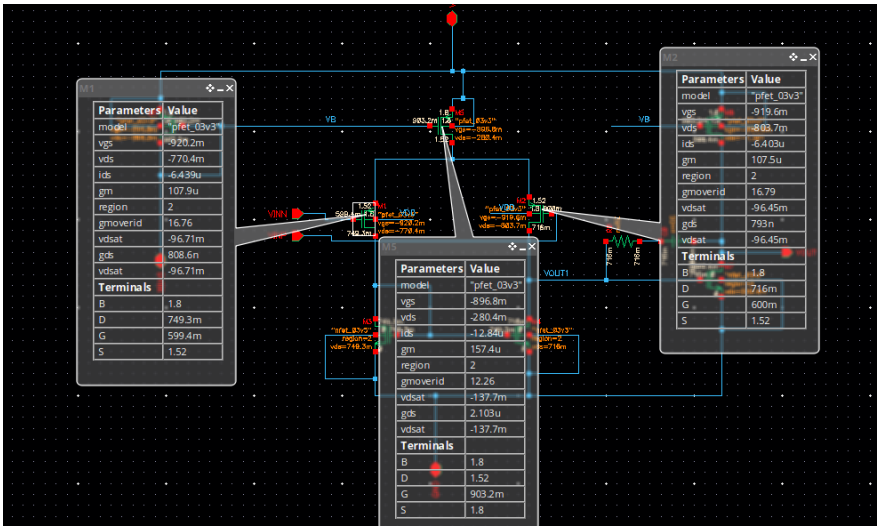
Test	Output	Nominal
5T_OTA:Two_stage_miller_TbCL:1	PM	70.58
5T_OTA:Two_stage_miller_TbCL:1	LGo	2.068k
5T_OTA:Two_stage_miller_TbCL:1	LG_dB	66.31
5T_OTA:Two_stage_miller_TbCL:1	bwd	10.36M
5T_OTA:Two_stage_miller_TbCL:1	UGFLG	7.134M
5T_OTA:Two_stage_miller_TbCL:1	BWLG	3.611k
5T_OTA:Two_stage_miller_TbCL:1	GBWLG	7.468M

⇨ **Vin vs Vout Overlaid:**



⇨ **Hand calculations:**

- **We can see that the deviation happened from our initial design points is not huge just few Tuning to specs**



$$S_R = \frac{I_{B1}}{C_C} = \frac{12.84u}{2.18P} = 5.89MV/us$$

⇨ **Comparison :**

	S_R
Hand Analysis	**5.89MV/us**
Simulation	**4.91MV/us**

Settling Time:

5T_OTA:Two_stage_miller_TbCL:1	risetime	44.8n

$$RiseTime < 70ns\ , T_{rise} = 44.8ns$$

⇨ **Hand Calculation:**

$$V_{out} = V_{max}\left(1 - e^{-\frac{t}{\tau}}\right)\ , t_{rise} = t_2 - t_1 = 2.2\tau_{cl} = \frac{2.2 * A_{CL}}{\omega_u}$$

$$t_{rise} = 2.2 * \frac{1}{GBW * 2\pi} = 46.9ns$$

⇨ **Comparison between Hand analysis and simulation results:**

	t_{rise}
Hand Analysis	**46.9ns**
Simulation	**44.8ns**

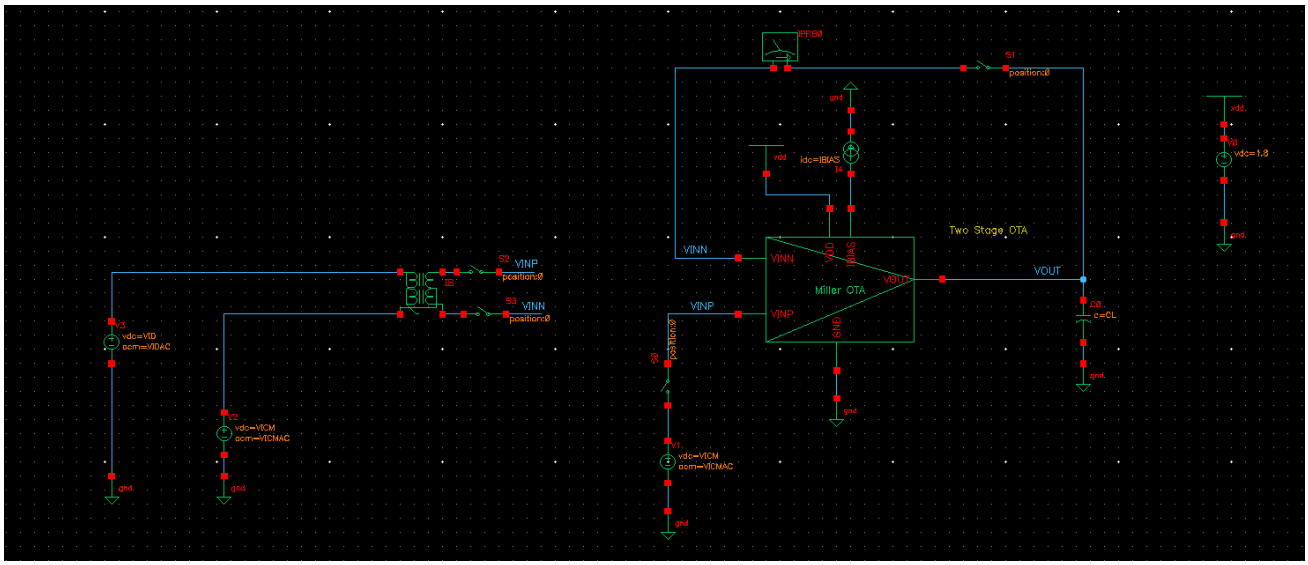
Do you see any ringing? Why?

there is little overshoot as the system is second order system but still have overshoots , as the PM<76

⇨ **designing for higher PM with Body effects make the Design very challenging and consume a lot of time**

DC Closed Loop AC Open-Loop OTA simulation :

- ⇨ Schematic :



- ⇨ From this schematic we simulate AC for the Open Loop Circuit while Closed loop for DC OP
- ⇨ We expect the results will be better as the there is no mismatch introduced For the Ac gain
- ⇨ Here is comparison between the Diff small signal analysis for this TB and the previous Part

Diff small signal CCS:

Test	Output	Nominal
5T_OTA:Two_stage_miller_TbCL_OL:1	AO_dB	66.23
5T_OTA:Two_stage_miller_TbCL_OL:1	AO	2.048k
5T_OTA:Two_stage_miller_TbCL_OL:1	BW	3.271k
5T_OTA:Two_stage_miller_TbCL_OL:1	UGF	6.277M
5T_OTA:Two_stage_miller_TbCL_OL:1	GBW	6.7M

⇨ **Previous TB from DC-Gain:**

Test	Output	Nominal
5T_OTA:Two_stage_miller_TbCL:1	LGo	2.036k
5T_OTA:Two_stage_miller_TbCL:1	LG_dB	66.17
5T_OTA:Two_stage_miller_TbCL:1	bwcl	9.507M
5T_OTA:Two_stage_miller_TbCL:1	UGFLG	6.291M
5T_OTA:Two_stage_miller_TbCL:1	BWLG	3.293k
5T_OTA:Two_stage_miller_TbCL:1	GBWLG	6.703M

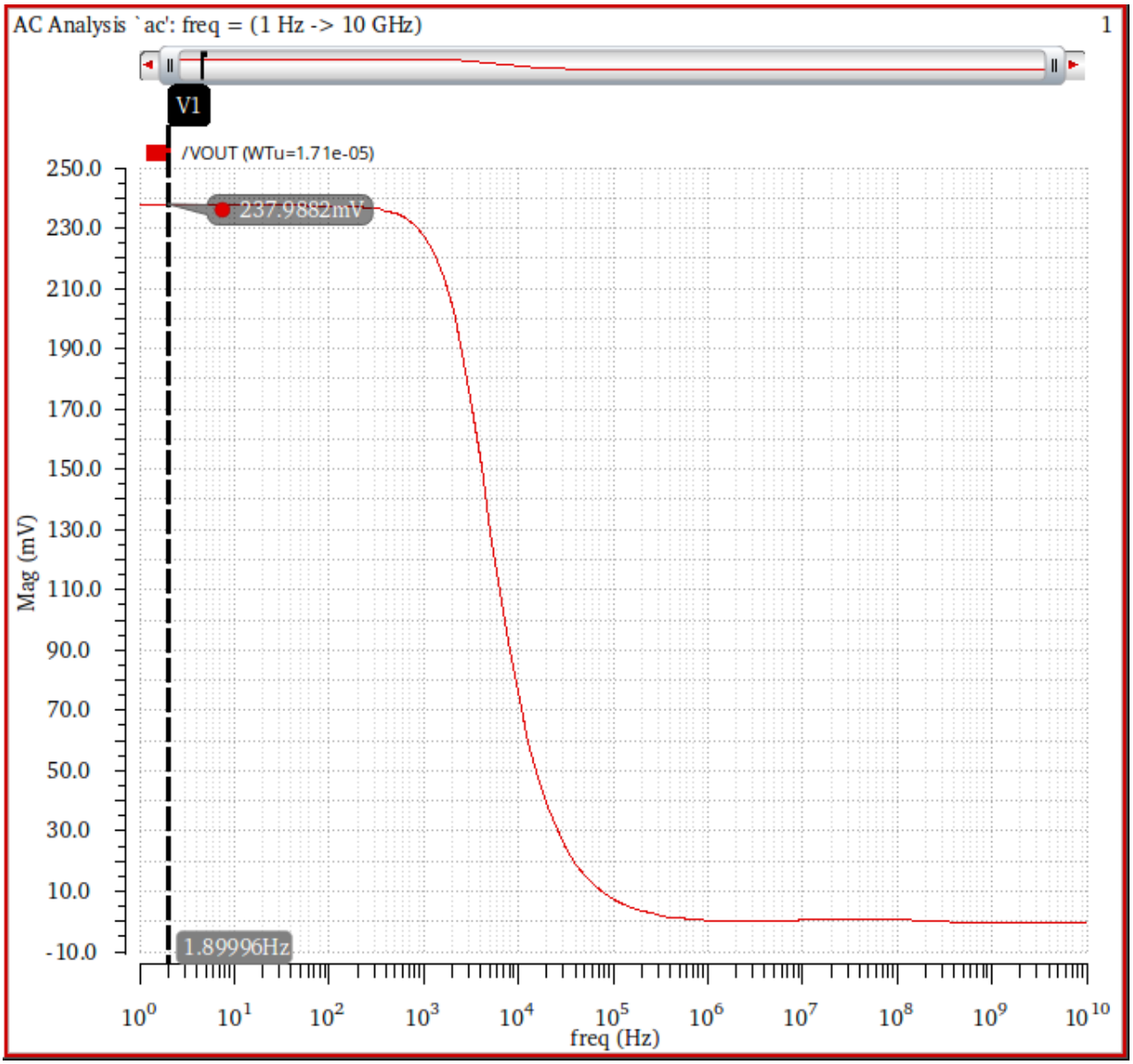
⇨ **The results Closes from the Results obtained from closed loop As the in Ac Analysis spectre runs Dc first and then Run**

AC using the values obtained from the DC , the DC Circuit is the closed loop circuit so the results like the Results from the Closed loop

⇨ **Using trise = 2.2τ is based on first-order model. Is second-order system faster?**

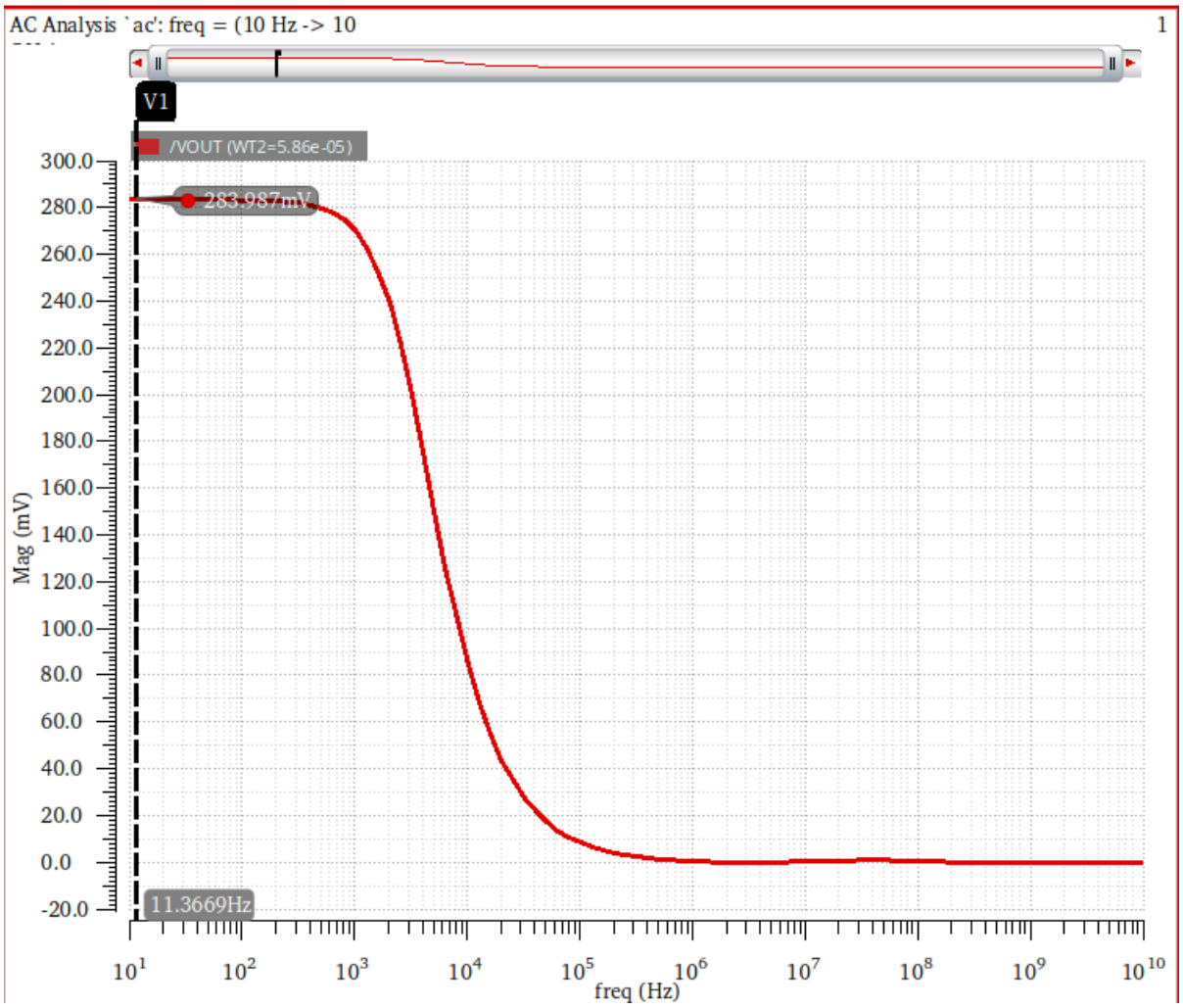
Second order system with optimum phase Margin is faster than the first order system as the first order system is overdamped while the second order system with optimum phase margin is critical or about to be critical

CM Small Signal CCS:



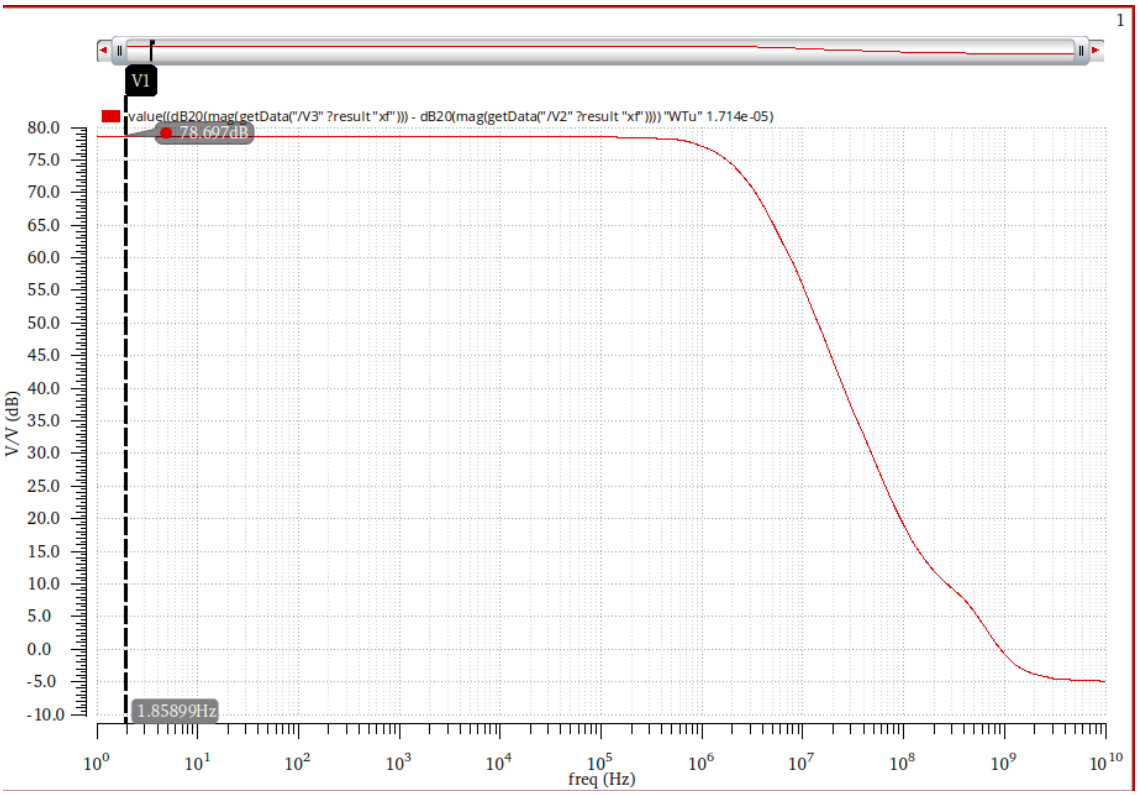
Test	Output	Nominal
5T_OTA:Two_stage_miller_TbCL_OL:1	AO_dB	-12.47
5T_OTA:Two_stage_miller_TbCL_OL:1	AO	238m
5T_OTA:Two_stage_miller_TbCL_OL:1	BW	3.271k
5T_OTA:Two_stage_miller_TbCL_OL:1	GBW	778.4

⇨ **The previous TB Results :**

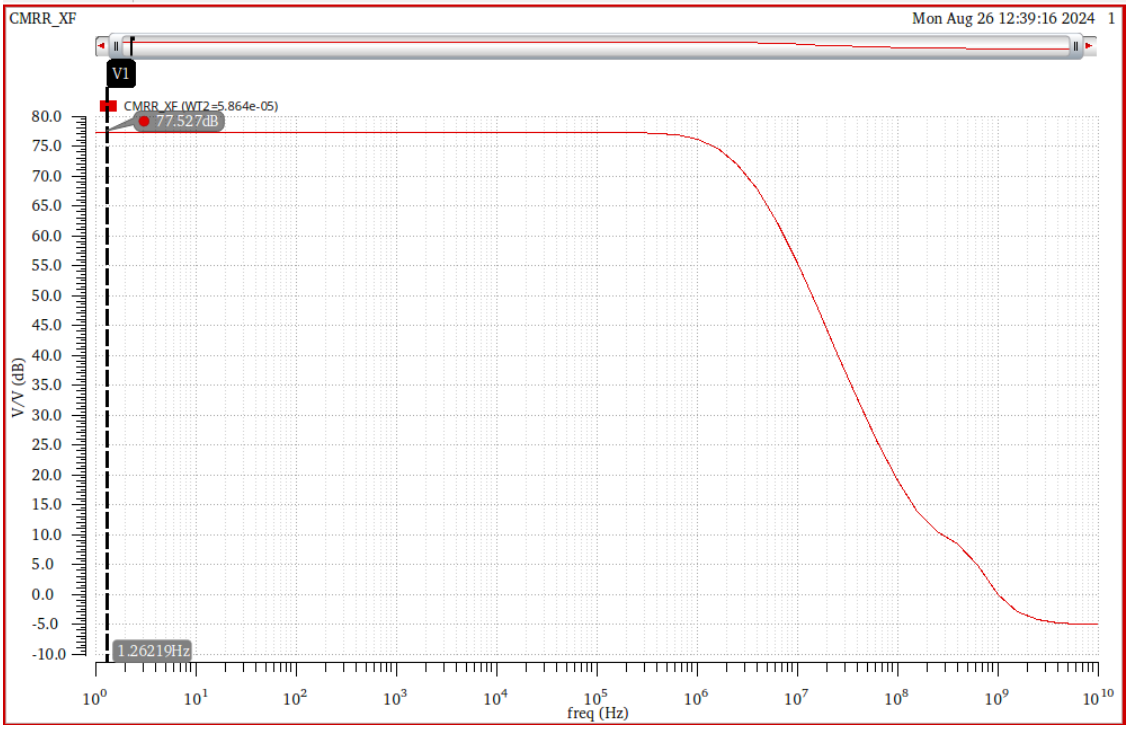


⇨ **Common mode gain is reduced**

CMRR:

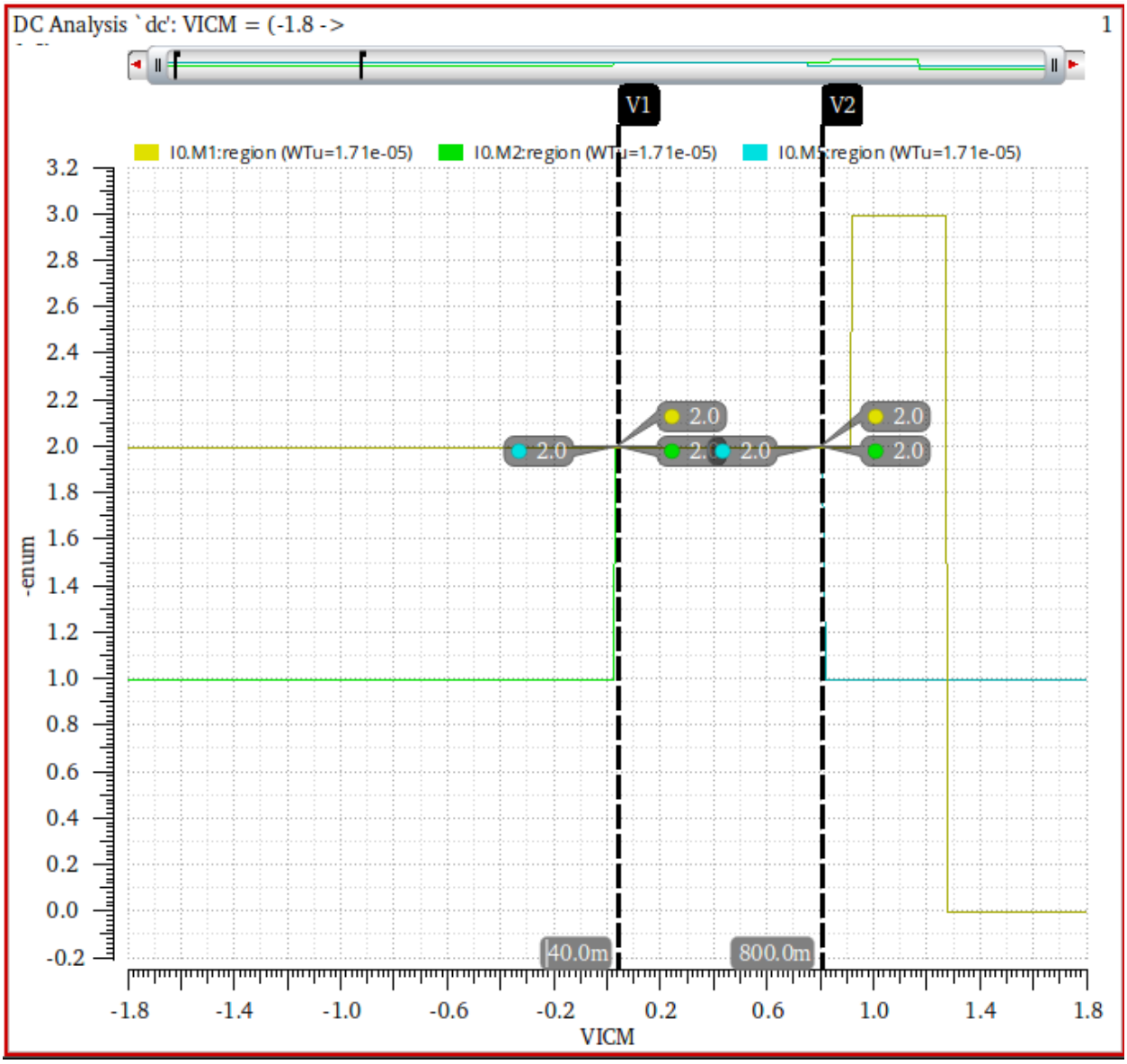


⇨ **For Part 3 CMRR**



CM Large Signal Analysis:

CMIR: 40mv To 800mV



⇨ Total Area:

$$Area = \sum W_i * L_i$$

$$= 2 * 3.089u * 400n + 58.64u * 480n + 17.14u * 480n + 11.35u * 320n + 25.3u * 400n * 2 + 13u * 480n = 99.32pm^2$$

Summary of Design:

Technology	0.13um	0.18um
Supply voltage	1.2V	1.8V
Static gain error	<= 0.05%	<= 0.05%
CMRR @ DC	>= 74dB	>= 74dB
Phase margin (avoid pole-zero doublets)	>= 70°	>= 70°
OTA current consumption	<= 60uA	<= 60uA
CMIR – high	>= 0.6V	>= 1V
CMIR – low	<= 0.2V	<= 0.2V
Output swing	0.2 – 1V	0.2 – 1.6V
Load	5pF	5pF
Buffer closed loop rise time (10% to 90%)	<= 70ns	<= 70ns
Slew rate (SR)	$5V/\mu s$	$5V/\mu s$

	Specs	Achieved
Supply Voltage	1.8v	1.8v
Static gain error	<=0.05%	0.048%
CMRR @ DC	>=74dB	77.53dB
Phase Margin	>=70°	70.58
OTA Current Consumption	<=60uA	57.5uA
CMIR-High	>=1	0.8v
CMIR-Low	<=0.2	0.04V
Output swing	0.2-1.6	0.168V - 1.64V
Load	5pF	5PF
Buffer Closed loop rise time	<=70ns	44.8n
Slew Rate	5V/us	4.901V/us