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Milestone 2 Report

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Technical Summary

In Milestone 2, we created a new data path for a single cycle processor to handle the 40 RV32I instructions. Also, basic test cases covering all supported instructions were included. We assume that we have two separated memories, one for instructions and the other one is data memory. We implemented verilog modules for each component in our datapath. Then, using a top module called “Single_cycle_processor”, we instantiated all modules and gave them the appropriate inputs. We also wrote a testbench to simulate the clock. We handle the EBREAK instruction as a halting instruction that ends the execution of any program, preventing the program counter from being updated anymore. However, the ECALL and FENCE instructions were implemented as unconditional jumping instructions jumping to address zero.

The Data path [modified single cycle processor]

Below is the data path we used to implement the 40 instructions in the single cycle RISC V processor.

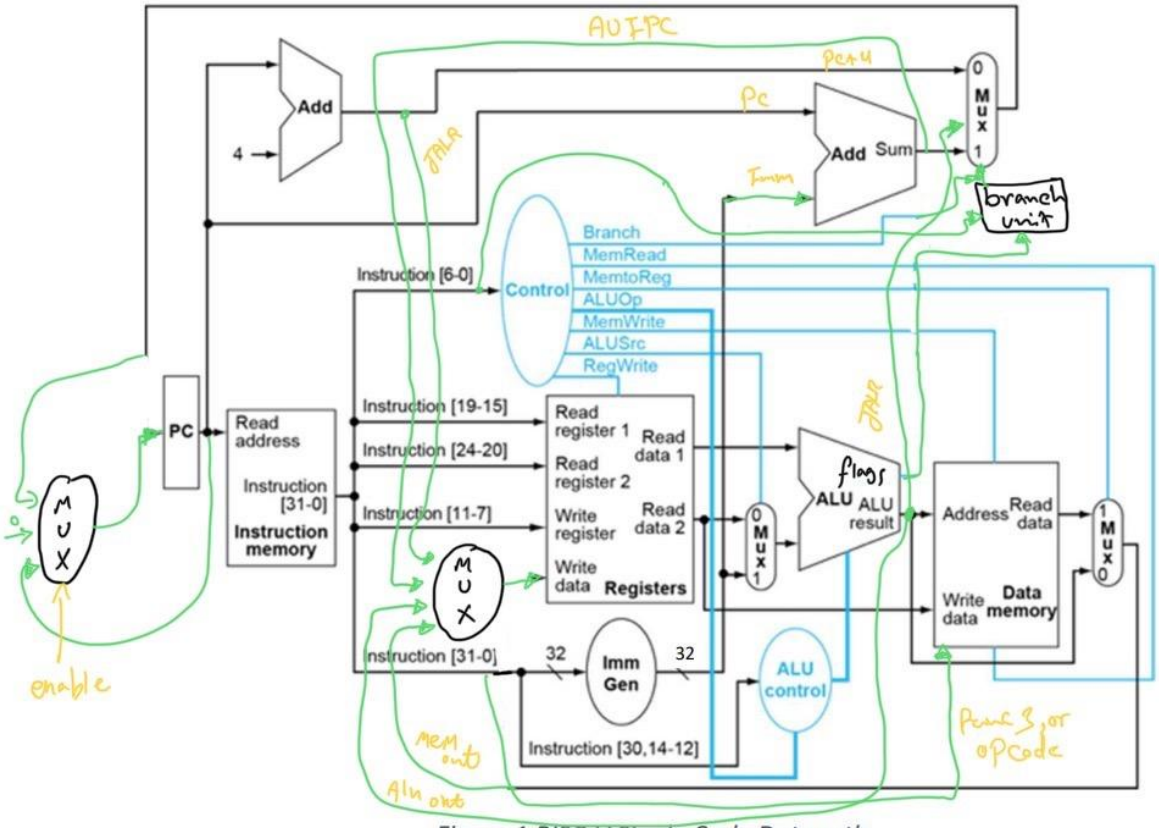

Figure 1 RISC-V Single Cycle Datapath

- PC
  - The program counter
  - Send an address to the instruction memory
  - The adder adds 4 to pc to get the next address
  - Another adder adds ImmGen to pc to jump to an specific address
- Instruction Memory
  - Accommodate all instructions
  - Get the output of the program counter
  - Fetch the instruction

    - Send the instruction (32 bit) to the Register file
    - Send signals to other modules in the data path such as ALU control unit, data memory, ImmGen, and the control unit
- The control unit
    - It's like a select line for the MUXs and other modules to help them decide which operation to do
    - It includes Branch, ALU, RegWrite, RegtoMem, MemRead, MemWrite, ALUOP,
- The imm gen unit
    - Extract the immediate part in the instruction
- The ALU unit
    - Do Arithmetic operations
    - Receive inputs from Register file and MUX
    - ALU control manages the operations
- The ALU control unit
    - Determines which arithmetic operation to execute
- The branching unit
    - Handle all branching instructions

Verilog Description files

The Verilog descriptions supporting all of the RV32I instructions are included in the zip file.

Simulation and Testing

The Verilog test functions that verify all of the RV32I instructions are included in the zip file.

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