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Milestone 3 Report

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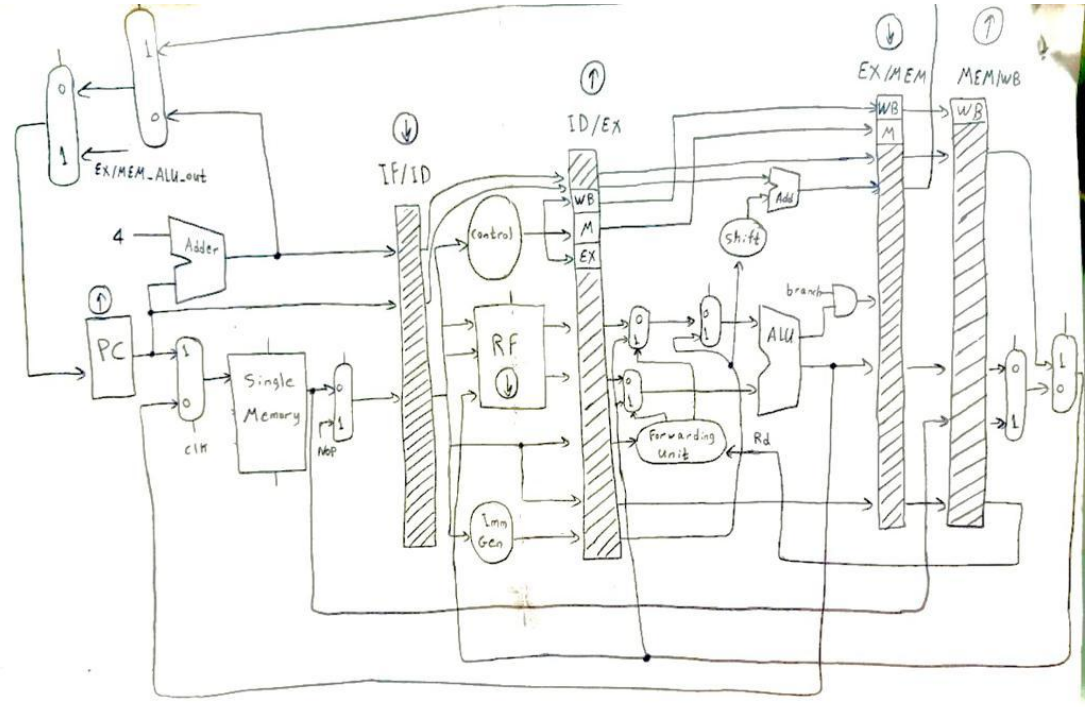
Technical Summary

In Milestone 3, we created a new memory instead of the Data Memory and the Instruction memory. Now, we have two memories in one module, so we divided our new memory into two parts. First half of the memory was for data and the other half was for instructions. Then, in the integration, we added a mux to select whether to fetch an instruction or to deal with data. If the clock is 1, then we fetch an instruction. On the other hand, if the clock is 0, then we deal with data. Moreover, we handled structural hazards by fetching 1 instruction every two cycles of the clock; this happens by alternating between positive and negative edges of the clock.

The Data path [modified single cycle processor]



Above is the data path we used to implement the 40 instructions in the single cycle RISC V processor USING pipelining.

Technical Modifications in the code

- We import the code of the pipelined data path from the lab work
- Now we have the registers between every stage so we can update the outputs of the previous stage, and passing them as inputs to the next stage
- We have 4 registers IF_ID, ID_EX, EX_MEM, and MEM_WB.
    - IF_ID will take the 32-bit instruction, PC, and PC+4 to handle AUIPAC and JALR
    - ID_EX will take output of the register files, PC value, PC+4 , the immediate value, 2 source registers and destination register.
    - EX_MEM will take the signals of the control unit, Pc, PC+4, PC+imm, zero flag, ALU output
    - MEM_WB will take WB, regwrite,memToreg, memory output, PC+4, the destination register, ALU output,.

Verilog Description files

The Verilog descriptions supporting all of the RV32I instructions are included in the zip file.

Simulation and Testing

No simulation or testing were included in this milestone. Only source codes.

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