CSCE 3301 – Computer Architecture

Fall 2020

Project 1: femtoRV32

RISC-V FPGA Implementation and Testing

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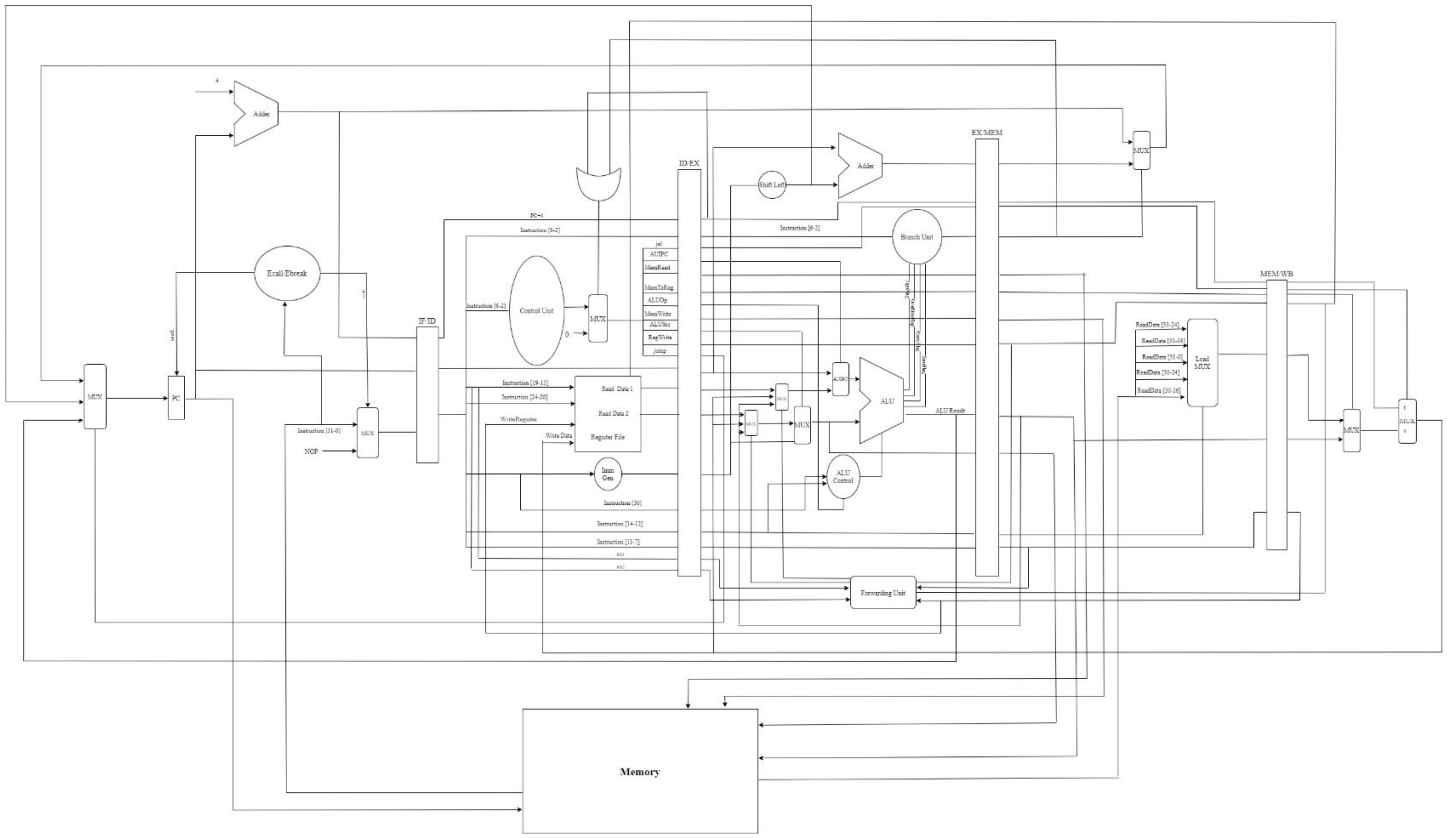

Modified Datapath

Components:

- PC: A single 32-bit register containing the address of the instruction to be fetched from the instruction memory.
- Next Instruction Adder: Adds 4 to the PC register to allow it to fetch the next instruction to execute.
- Register File: A set of 32 registers used for various purposes.
- Immediate Generator: Extracts the immediate from the instruction and arrange it properly if needed. It extends the sign, as well.
- Shift Left: Basically, multiplying the immediate generated by 2 to produce the intended offset; the immediate extracted from the instruction is in halfwords.
- Control Unit: Takes the opcode from the instruction (Instruction[6:2]) and produces several signals used by other components:
    - AUIPC: set to 1 if the current instruction being executed is AUIPC to choose the first input of the ALU to be the PC output.
    - Jal: 1 bit indicator used to store PC+4 in rd.
    - Jump: 2 bits used to control the PC input.
    - MemRead: decides whether the current instruction needs to read from the memory or not.
    - MemToReg: determines whether the current instruction will write back the memory read data to the register file or not. If cleared (set to 0), the writeback MUX will output the ALU result instead.
    - ALUOp: 2-bit signal used by the ALU to allow it to recognize the requested function to do.

- MemWrite: enables writing to the memory to allow for storing in the data memory.
- ALUSrc: used as selection line for a mux choosing between the second read register data 2, and the 32-bit immediate generated by the immediate generator.
- RegWrite: enables writing to the register file in case it is needed to write back the ALU result, or the value loaded from the data memory.

- AUIPC MUX: simply multiplexing between the first read data 1 (RS1) and the current PC. Its selection line is produced by the ALU depending on whether the instruction being executed is AUIPC or not.
- ALU Control: Receives 2-bit signal from the control unit and based on it produces 4-bit signal acting as selection lines for the ALU to pick the right operation to perform.
- ALU second input MUX: Chooses between the second read register data 2 and the immediate generator output as a second input for the ALU.
- Target Address Adder: Adds the offset, which is the shift left output, to the PC to calculate the target address needed by B-type instructions ("branch" instructions).
- Branch Unit: takes the opcode from the instruction to assure this instruction is indeed a B-type (branch) instruction. Then, we take the func3 to decide which instruction is being executed. Using the flags produced by the ALU (cf, zf, sf, vf) to check if the instruction's conditions are met and consequently set the branch flag which is the selection line for the target address MUX.
- Target Address MUX: chooses between the target address coming from the target address adder, and the next instruction adder output. Its selection line the branch signal received from the branch unit.

- Load MUX: Multiplexing between the upper byte, the upper half word, the whole word, the upper byte w/t the sign bit (MSB), and the upper half word w/t the sign bit (MSB).
- Memory: Byte addressable memory of size 512 bytes. It's divided into two portions. 256 bytes for the instructions, and the other 256 bytes for the data. It receives a couple of signals to enable reading from and writing into it besides the func3 signal to determine whether to read 1 byte, 2 bytes (half word), or 4 bytes (full word).
- Writeback MUX: Decides whether the result to be written back into the register file is ALU result or the read data from the data memory.
- Ecall Unit: generates a flag to stall the PC.
- PC Mux: controlling the jump instructions.