



Unit6 MCU Fundamentals

Lesson 1 Assignment



20)

MICRO-PROCESSOR

a single chip which include an ALU, CPU registers to control a set of instructions and control the operation of execution

Designed for general purpose

This MPU chip can be not really integrated/added with/to other components to build any required MC, SOC to do any purpose

So it's enable register to determine the amount of units to be integrated with MPU and the strength, it's just a brain which i can but be to operate and body i need (and body with and size)

MICRO-CONTROLLER

is a MCU in addition to set of other components like RAM, ROM and other peripherals like I/O peripherals, UART peripheral, ... etc

Designed for specific purpose/task

this MCU chip is actually set of MPUS, memory units, peripherals which are designed/integrated together to perform specific task, but the final MCU chip is not scalable to add other units, peripherals

But here i can select the body size i need for my task (brain + body)

MCU

Q3)

Non-Volatile

Data & Instructions are also stored into the same memory "RAM"

There is single common data bus to fetch data & instructions from memory to CPU

Harvard

there is a separate memory for data "RAM" and another for instructions "ROM"

There is single data bus among memory data "RAM" and CPU, another one among instructions "ROM" to CPU

Q4)

→ PROM (Programmable ROM):

it's programmable by the user to burn his own data on it for only one time.

→ EPROM (Erase Programmable ROM):

it's a type of PROM with ability to clear the ROM and write on it again, to burn data on ROM we need a burner.

→ EEPROM (Electrically Erasable Programmable ROM):

it's a type of EPROM with ability to clear specific part of ^{byte} ROM instead the whole ROM to write new changes on it & no need to an external burner to burn the data on it.

→ Flash EPROM:

data contents are divide into blocks, ^{sector} where erasing is done block by another, no need for an external burner to burn the data

→ Mask ROM:

its programmable by only the Manufacturer to burn his own data onto for only one time (biost)

96)

→ SRAM (Static Random access memory)

- consist of 6 transistor
- There is no need to refresh data contents per time
- faster, as there is no refresh operation are done
- More complex design
- More expensive
- Used to build cache memory

→ DRAM (Dynamic access memory)

- consist of 1 transistor, 1 capacitor
- So its less expensive
- less complex
- but the capacitor voltage need to be refreshed per time (1.6 times per second)
- as a result of using refresh operation its slower than SRAM

→ NVRAM (Non Volatile RAM)

- It comes among (SRAM & EPROM) as it make a backup for data per time into ~~temp~~ temporary non volatile memory which has its own battery.

96)

type	volatile?	writable?	erase size	max erase cycle	cost	speed
SRAM	Y	Y	byte	unlimited	expensive	Fast
DRAM	Y	Y	byte	unlimited	moderate	moderate
Masked ROM	N	N	N/A	N/A	inexpensive	Fast
PRAM	N	only with a device on system	N/A	N/A	moderate	Fast
EPROM	N	yes, with special programmer	entire chip	limited	moderate	Fast
EEPROM	N	Y	byte	limited	expensive	Fast to read slow to write
Flash	N	Y	sector	limited	moderate	Fast to read slow to write
NVRAM	N	Y	byte	unlimited	expensive	Fast