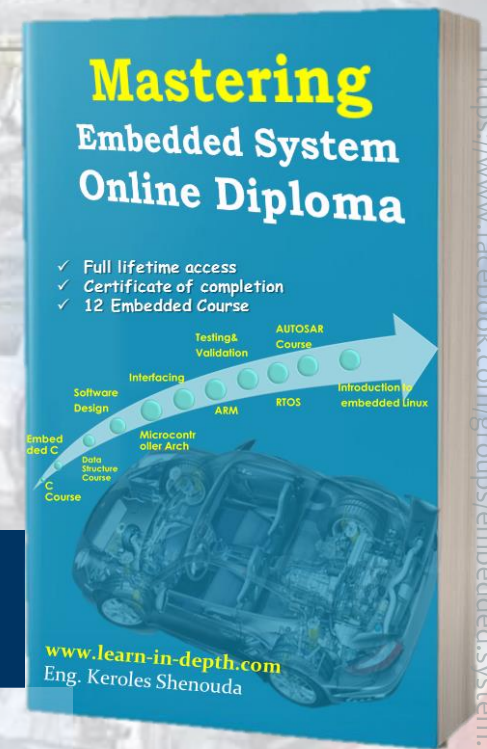


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# Assignments Solution

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# Answer those Questiones in white paper by your handwriting the Following Comparisons

<i>Definition</i>	<i>Meaning</i>
<b><i>Micro-processor</i></b>	General purpose processor contains no RAM , no ROM and no I/O ports and can't operate without adding them to it externally
<b><i>Micro-controller</i></b>	A single specific purpose chip contains CPU , fixed amount of RAM , ROM and I/O ports used to control embedded systems
<b><i>Embedded Systems</i></b>	Systems (electrical or electromechanical devices) controlled by Special purpose computer encapsulated inside it
<b><i>Mechatronic systems</i></b>	Systems in which mechanical hardware are integrated with information – driven systems (Micro-controllers)
<b><i>n-bit processor</i></b>	1- Processor works only on n-bit of data at a time 2- Data larger than n-bit has to be broken into n-bit pieces to be processed

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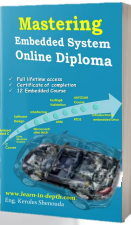


# Answer those Questiones in white paper by your handwriting the Following Comparisons

## ► Q2) Compare between *Micro-processor* Vs *Micro-controller*

<i>Micro-processor</i>	<i>Micro-controller</i>
General purpose	Specific purpose and include a microprocessor inside
Contains no Ram , no Rom and no I/O on the chip itself	Contains fixed amount of on-chip ROM , Ram and number of I/O ports
Disadvantage : Its systems are bulkier and expensive because RAM , ROM and I/O ports are added externally	Disadvantage : The designer can't add any external memory , I/O ports or timers to it to fit more advanced tasks
Advantage : Its systems its systems are versatile enabling the designer to decide on the amount of RAM , ROM and I/O ports to fit the task	Advantage : Ideal for application in which cost and space are critical

# Q3



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## ➤ ***Von-Neuman Vs. Harvard Architecture***

### ✓ ***Von-Neuman :***

- 1) Single common memory space where program instructions and data are stored
- 2) There is a single data bus fetches both instructions and data

### ✓ ***Harvard architecture***

- 1) Separate memory area for instructions and another are for data
- 2) One bus connects the CPU to the RAM and another connects the CPU to ROM

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# Q4

## ✓ **PROM (programmable ROM)**

- 1) The kind of ROM that the user can burn information into
- 2) For every bit , there is a fuse
- 3) PROM is programmed by blowing the fuses
- 4) The information can be burned into PROM only once , so it's called OTP(one-time programmable)

## ✓ **EPROM (Erasable programmable ROM)**

- 1) Can be programmed and erased thousands of times
- 2) A widely used (EPROM) is called (UV-EPROM)
- 3) UV-EPROM has a window through which the programmer can shine ultra-violet radiation to erase its contents
- 4) To burn code into the UV-EPROM , the ROM burner uses 12.5 volts or higher
- 5) The major disadvantage with UV-EPROM is that it cannot be erased while it's in the system board

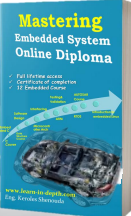
## ✓ **EEPROM (electrically erasable programmable ROM)**

- 1) Its method of erasure is electrical and therefore instant as opposed to 20-minute erasure time required for UV-EPROM
- 2) In EEPROM , you can select the byte to be erased in contrast to UV-EPROM whose contents can be only entirely erased
- 3) It can be programmed while it's in the system board without the need of an external erasure or programming device
- 4) It's cost is higher than UV-EEPROM

## ✓ **Flash memory EPROM**

- 1) The erasure method is electrical so , it's referred to as flash EEPROM

- 2) In old flash EEPROM you can only erase the entire contents (not just specific byte)
  - 3) In recent decades flash memory contents are divided into blocks where erasing is done block by block
  - 4) It can be programmed while it's in the system board
- ## ✓ **Mask ROM**
- 1) It's not a user programmable ROM
  - 2) It's contents are only programmed by the IC-Manufacturer
  - 3) Cheaper than other kinds of ROMs and is one-time programmable (OTP)



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# Q5

## ➤ Types of RAM

### ✓ **SRAM (Static RAM)**

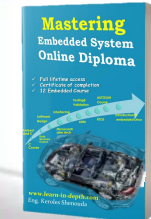
- 1) Storage cells are made of flip-flops and therefore don't require refreshing in order to keep their data
- 2) The problem of flip-flops is that each cell requires at least 6 transistors to build and this cell hold only 1 bit
- 3) The use of 4-transistor cells plus the use of CMOS technology give birth to a high-capacity SRAM but its capacity is so far below that of DRAM

### ✓ **NV-RAM (Non Volatile RAM)**

- 1) It allows the CPU to read and write to it and when the power is off , the contents are not lost
- 2) It can retain its contents up to 10 years after turning off the power
- 3) It uses extremely power-efficient SRAM cells built out of CMOS
- 4) It uses internal lithium battery as a backup energy source
- 5) If the power to the Vcc pin falls bellow out of tolerance condition , the control circuitry switches automatically to its internal power source (the lithium battery)
- 6) Another type of the NVARM combines SRAM and EEPROM so that its content is written into the EEPROM when power is off and is read back from the EEPROM when power is restored.

### ✓ **DRAM (Dynamic RAM)**

- 1) It's lower than SRAM in price power consumption
- 2) The use of capacitors as storage cells in DRAM results in smaller net memory size than SRAM
- 3) Using a capacitor to store data cuts down the number of transistors to build the cells
- 4) The capacitors require constant refreshing due to charge leakage
- 5) While DRAM is being refreshed , its data cannot be accessed in contrast to SRAM whose data can be accessed any time as it doesn't need refreshing



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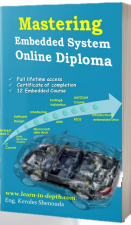
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# Q6

- ▶ It is referred to as ROM since in the normal operations, the CPU does not have the capability to write to it.
- ▶ It may be written to by an external device, or there may be a special configuration within the system wherein the CPU is granted access to write to it



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# Q7) Fill this Table

Type	Volatile?	Writeable?	Erase size	Max Erase cycles	Cost(per Byte)	Speed
SRAM	Yes	Yes	Byte	Unlimited	Expensive	Fast
DRAM	Yes	Yes	Byte	Unlimited	Moderate	Moderate
Masked ROM	No	No	N/A	N/A	Inexpensive	Fast
PROM	No	Once, with a device programmer	N/A	N/A	Moderate	Fast
EPROM	No	Yes, with a device programmer	Entire Chip	Limited (consult Data sheet)	Moderate	Fast
EEPROM	No	Yes	Byte	Limited (consult Data sheet)	Expensive	Fast to read, slow to erase/write
FLASH	No	Yes	Sector	Limited (consult Data sheet)	Moderate	Fast to read, slow to erase/write
NVRAM	No	Yes	Byte	Unlimited	Expensive (SRAM + Battery)	Fast

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