Analog to Digital Converter (ADC)

The ***analog to digital converter*** allows for an input voltage (physical characteristic) to be converted into binary value processable by the µC. Most AVR µC have ***10-bit resolution*** ADC's, each one having multiple ***channels*** that can be read individually or sequentially. Differential voltage can also be evaluated, and a gain applied.

Successive Approximation Method: The ADC in the AVR µCs, uses the ***successive approximation*** technique to detect the analog signal value on one of the ADC channels. The reference voltage is continuously divided by 2 by and internal **DAC** and compared to the input signal to see if its higher or lower, until it can come up with a digital value that is approximately equal to the analog signal ($\pm \mathbf{0.5}\boldsymbol{LSB}$). These tests are repeated 10 times to fill-out all bits of the 10-bit **ADC**.

Sampling Process and Adequate frequency: The ADC has a sampler of type ***"sample and hold"*** to ensure that the input voltage stays constant during conversion. For maximum resolution, an input clock frequency between $\mathbf{50}\boldsymbol{kHz}$ and $\mathbf{200}\boldsymbol{kHz}$ is required. The prescaler bits $\boldsymbol{ADPS}[\mathbf{2}:\mathbf{0}]$ in $\boldsymbol{ADCSRA}$ must be set accordingly.

Supply Pin and Noise Reduction: The ADC has an external power supply pin called **AVCC**. The voltage applied to it must not differ more than $\pm \mathbf{0.3}\boldsymbol{V}$ from the supply voltage of the µC. A noise reduction can be used here, which is to connect an ***LC*** circuit to it ***as shown in the ATmega324PB datasheet on page 299***.

Other Noise Reduction Technics:

1. Keep ADC paths as short as possible. Apply a ***ground plane*** to the PCB and keep ADC paths far from high-speed switching digital tracks (communication modules and frequently switches GPIOs).
2. Avoid switching ***GPIOs*** that are ***ADC ports*** during conversion.

Signal Compatibility: The ADC is optimized to handle signals with an ***output impedance*** lower than $\mathbf{10k\Omega}$. Anything higher will increase the sampling time. If the signals maximum frequency is bigger than the ***Nyquist/Shannon sampling frequency*** of the ADC ($\boldsymbol{f_{ADC}}/\mathbf{2}$), there might be signal distortions. To avoid this, a ***low pass filter*** applied to the signal is necessary before inputting it to the ADC.

Reference Voltage: The ***low*** state of the ADC is referenced by the ***GND***. For the high reference voltage, we have the choice between the internal voltage reference of ***1.1V***, and an external reference voltage defined by the input at the **AREF** or **AVCC** pin. If the internal reference is used, the **AREF** pin must be connected to **GND** with a capacitor of $\mathbf{100}\boldsymbol{nF}$. If the **AREF** pin is used as an external voltage reference, it can be connected to the **AVCC** pin for **5V**.

Error Compensation and Accuracy Definition: Several factors describe a deviation from ideal behavior for the ADC:

- **Offset**: A positive or negative value is added to all measurement of the specific channel.
- **Gain Error**: An error in the ***leading coefficient*** of the linear equation describing the ADC.

These two errors can be corrected in software.

Auto Triggering Conversion: A conversion can be automatically triggered on the ***positive edge*** of a selected source. The source can be selected by assigning a value to the $\boldsymbol{ADTS}[\mathbf{2}:\mathbf{0}]$ bits in the **ADCSRB**. The **ADATE** bit in **ADCSRA** must be set to enable the auto triggering. The ***free running*** mode continuously does the ADC process and updates the data register automatically. The ***timer/counter*** modes can be used to get ADC values at fixed time intervals. The table of all possible source of ADC auto triggering is given ***on page 308 of the ATmega324PB datasheet***.

Interrupt: The ADC peripheral has one interrupt associated with it, which is the ***"ADC conversion complete"*** interrupt. To enable it, the ***interrupt enable*** bit **ADIE** must be set in **ADCSRA**. As soon as a conversion is complete, the hardware enters the ***ISR*** which would be used to fetch the data.

Differential ADC: There are 16 differential voltage input combinations, with two of them having a programmable gain stage (0dB, 20dB (× 10), 46dB (× 200)). Differential mode should be used with $\boldsymbol{AREF} < \mathbf{2}\boldsymbol{V}$. The gain stage is optimized for a ***4kHz*** bandwidth. An analog low pass filter should be used if higher frequency signals are inputted, otherwise the signal could be subject to ***non-linear amplification***. The ***gain stage*** has an ***offset cancellation circuitry*** to correct the output. However, it takes time to settle, therefore the first conversion in differential mode isn't the most reliable.

Important Registers

$\boldsymbol{ADMUX}$	$\boldsymbol{ADCSRA}$	$\boldsymbol{ADCSRB}$	$\boldsymbol{ADC}[\boldsymbol{H}:\boldsymbol{L}]$