LFSR_CRC Testbench Results

********** **Test Case #1** **********
Status *: PASSED*
Data In : 10010011
Expected CRC : 01111000
Observed CRC : 01111000
****

********** **Test Case #2** **********
Status *: PASSED*
Data In : 01110010
Expected CRC : 01000100
Observed CRC : 01000100
****

********** **Test Case #3** **********
Status *: PASSED*
Data In : 00110110
Expected CRC : 00010001
Observed CRC : 00010001
****

********** **Test Case #4** **********
Status *: PASSED*
Data In : 00011011
Expected CRC : 11010010
Observed CRC : 11010010
****

********** **Test Case #5** **********
Status *: PASSED*
Data In : 10100110
Expected CRC : 00001001
Observed CRC : 00001001
****

********** **Test Case #6** **********
Status *: PASSED*
Data In : 11000000
Expected CRC : 10110010
Observed CRC : 10110010
****

********** **Test Case #7** **********
Status *: PASSED*
Data In : 01010101
Expected CRC : 00110110
Observed CRC : 00110110
****

********** **Test Case #8** **********
Status *: PASSED*
Data In : 11110010
Expected CRC : 10000000
Observed CRC : 10000000
****

********** **Test Case #9** **********
Status *: PASSED*
Data In : 01011110
Expected CRC : 00101100
Observed CRC : 00101100
****

********** **Test Case #10** **********
Status *: PASSED*
Data In : 00010001
Expected CRC : 01100011
Observed CRC : 01100011
****

** Note: $stop : LFSR_CRC_tb.v(152)
Time: 4100 us Iteration: 0 Instance: /LFSR_CRC_tb
Break in Module LFSR_CRC_tb at LFSR_CRC_tb.v line 152