

Team name : 32bit

Names :

Mahmoud mohamed alsayd

Omar Khaled elsaid

Abdelkader saad

Codes :

Spi_slave :

```
1 module spi_slave (MOSI , MISO , SS_n , clk , rst_n , rx_data , rx_valid , tx_data , tx_valid );
2   parameter [2:0]IDLE = 3'b000;
3   parameter [2:0]READ_DATA = 3'b001;
4   parameter [2:0]READ_ADD = 3'b010;
5   parameter [2:0]CHK_CMD = 3'b011;
6   parameter [2:0]WRITE = 3'b100;
7
8   input MOSI , SS_n , tx_valid, clk , rst_n;
9   input [7:0] tx_data;
10  output reg [10:0] rx_data;
11  output reg rx_valid , MISO=0;
12  (* fsm_encoding = "sequential" *)
13  reg [2:0] ns ,cs;
14  reg address_or_read=0;
15  reg control_bit ;
16  integer counter = 10;
17  integer counter_to_recieve = 7;
18
19  always @(posedge clk or negedge rst_n) begin
20      if (~rst_n) begin
21          cs <= IDLE ;
22      end
23      else begin
24          cs <= ns;
25      end
26  end
27
28  //next stage
29  always @(cs or SS_n or control_bit ) begin
30      case (cs)
31      IDLE : begin
32          if (SS_n == 0)
33              ns = CHK_CMD;
34          else if (SS_n == 1)
35              ns = IDLE;
36      end
37
38      CHK_CMD : begin
39          if (SS_n ==0 && control_bit==0 )
40              ns = WRITE;
41          else if (SS_n ==0 && control_bit ==1 && address_or_read ==0)begin
42              ns = READ_ADD ;
43              address_or_read =1;
44          end
45          else if (SS_n ==0 && control_bit ==1 && address_or_read ==1)begin
46              ns = READ_DATA ;
47              address_or_read =0;
```

```

43     address_or_read =1;
44     end
45     else if (SS_n ==0 && control_bit ==1 && address_or_read ==1)begin
46         ns = READ_DATA ;
47         address_or_read =0;
48     end
49     else if (SS_n==1)
50         ns = IDLE;
51 end
52
53
54 WRITE : begin
55     if (SS_n == 0 )
56         ns = WRITE;
57     else if (SS_n == 1)
58         ns = IDLE ;
59     end
60
61 READ_ADD : begin
62     if (SS_n ==0 )
63         ns = READ_ADD;
64     else if (SS_n==1)
65         ns = IDLE ;
66
67 end
68
69 READ_DATA : begin
70     if (SS_n == 0)
71         ns = READ_DATA;
72     else if (SS_n==1)
73         ns = IDLE;
74 end
75 default : ns = IDLE;
76 endcase
77 end
78
79
80 //output logic
81 always @(posedge clk) begin
82
83 case (cs)
84 IDLE :begin
85     rx_valid <=0;
86     control_bit <= MOSI;//0
87 end
88
89 WRITE : begin

```

```

79
80 //output logic
81 always @(posedge clk) begin
82
83     case (cs)
84     IDLE :begin
85         rx_valid <=0;
86         control_bit <= MOSI;//0
87     end
88
89     WRITE : begin
90         rx_valid <=1;
91         rx_data[10] <= control_bit ;
92         rx_data [counter -1] <= MOSI;
93         counter <= counter -1;
94         if (counter == 0)
95             counter <= 10;
96     end
97
98     READ_ADD : begin
99         rx_valid <= 1;
100         rx_data [10] <= control_bit;
101         rx_data [counter-1] <= MOSI;
102         counter <= counter -1;
103         if (counter==0)
104             counter <= 10;
105     end
106
107     READ_DATA : begin
108         rx_data [10] <= control_bit;
109         rx_data [counter-1] <= MOSI;
110         counter <= counter -1;
111
112     if (counter==0)
113         counter <=10;
114
115     if (tx_valid) begin
116         MISO <= tx_data[counter_to_recieve];
117         counter_to_recieve <= counter_to_recieve -1;
118     end
119
120     if (counter_to_recieve==0)
121         counter_to_recieve <= 7;
122
123     end
124 endcase
125 end
126 endmodule
127

```

Ram :

```
1 module ram (din,clk,rst_n,rx_valid,dout,tx_valid);
2   parameter MEM_DEPTH = 256;
3   parameter ADDR_SIZE=8;
4   input [10:0] din;
5   input clk , rst_n , rx_valid;
6   output reg [7:0] dout;
7   output reg tx_valid;
8
9   reg [7:0] mem [MEM_DEPTH-1:0];
10  reg [ADDR_SIZE-1:0] wr_addr,rd_addr;
11  always @(posedge clk or negedge rst_n) begin
12      if (~rst_n)begin
13          dout <= 0;
14      end
15      else if (rx_valid) begin
16          if (din[9:8] == 2'b00) begin
17              wr_addr <= din[7:0];
18              tx_valid <= 0;
19          end
20
21          else if (din[9:8] == 2'b01) begin
22              mem[wr_addr] <= din[7:0];
23              tx_valid <= 0;
24          end
25
26          else if (din[9:8] == 2'b10) begin
27              rd_addr <= din[7:0];
28              tx_valid <= 0;
29          end
30      end
31  end
32
33  else if (din[9:8] == 2'b11) begin
34      dout <= mem[rd_addr];
35      tx_valid <= 1;
36  end
37 end
38
39 endmodule
```

Wrapper :

```
1 module spi_wrapper (MOSI , MISO , SS_n , clk , rst_n);
2
3   input MOSI , SS_n , clk , rst_n ;
4   output MISO ;
5
6   wire[10:0] rx_data ;
7   wire rx_valid , tx_valid ;
8   wire [7:0] tx_data ;
9
10  spi_slave dut1 (MOSI , MISO , SS_n , clk , rst_n , rx_data , rx_valid , tx_data , tx_valid );
11
12  ram dut2(rx_data ,clk , rst_n , rx_valid , tx_data ,tx_valid);
13 endmodule
14
```

Mem.dat:

```
1 0
2 1
3 2
4 3
5 4
6 5
7 6
8 7
```

Testbench:

```
1 module SPI_Wrapper_tb();
2   reg MOSI, SS_n, clk, rst_n;
3   wire MISO;
4   reg [9:0] write_addr = 10'b00_1111_0000; //address 240 in decimal
5
6   reg [9:0] write_data = 10'b01_1010_1110; // this data will write in the previos address
7
8   reg [9:0] read_addr = 10'b10_1111_0000; // address 240
9
10  reg [9:0] read_data = 10'b11_0000_0000; // it will be dummy data but we want only 11 to make ram to know that it in read state
11  integer i = 0;
12  spi_wrapper DUT(MOSI, MISO, SS_n, clk, rst_n);
13
14  initial begin
15      clk = 0;
16      forever
17          #10 clk = ~clk;
18  end
19
20  initial begin
21      $readmemh ("mem.dat" , DUT.dut2.mem);
22      rst_n = 0;
23      SS_n = 1;
24      #50;
25      rst_n = 1;
26      MOSI = 0;
27      SS_n = 0;
28      #50
29      for (i=0; i<10 ; i=i+1)begin
30          @(negedge clk)
31              MOSI = write_addr [9-i];
32          #5;
33      end
34      SS_n = 1;
35      #50
36
37      // to write data in the previos address
38      MOSI = 0;
39      SS_n = 0;
40      #50
41      for (i=0 ; i<10 ; i=i+1)begin
42          @(negedge clk)
43              MOSI = write_data [9-i];
44          #5;
45      end
46      SS_n = 1;
47      #50
48      // to write the address that i will read from
49
```

```

33     end
34     SS_n = 1;
35     #50
36
37
38     // to write data in the previos address
39     MOSI = 0;
40     SS_n = 0;
41     #50
42     for (i=0 ; i<10 ; i=i+1)begin
43         @(negedge clk)
44         MOSI = write_data [9-i];
45         #5;
46     end
47     SS_n = 1;
48     #50
49     // to write the address that i will read from
50     MOSI =1;
51     SS_n =0;
52     #50
53     for (i=0 ; i<10 ; i=i+1)begin
54         @(negedge clk)
55         MOSI = read_addr [9-i];
56         #5;
57     end
58     SS_n =1;
59     #50
60     MOSI =1;
61     SS_n =0;
62     #50
63     for (i=0 ; i<10 ; i=i+1)begin
64         @(negedge clk)
65         MOSI = read_data [9-i];
66         #5;
67     end
68
69     #40 $stop;
70 end
71
72 endmodule

```

Do file :

```

1 |vlib work
2
3 vlog ram_spi.v spi_slave.v testbench.v wrapper.v
4
5 vsim -voptargs=+acc work.SPI_Wrapper_tb
6
7 add wave *
8 add wave -position insertpoint \
9 sim:/SPI_Wrapper_tb/DUT/dut2/mem
10 add wave -position insertpoint \
11 sim:/SPI_Wrapper_tb/DUT/dut1/tx_valid \
12 sim:/SPI_Wrapper_tb/DUT/dut1/tx_data \
13 sim:/SPI_Wrapper_tb/DUT/dut1/rx_data \
14 sim:/SPI_Wrapper_tb/DUT/dut1/rx_valid
15
16 run -all

```

Tcl file :

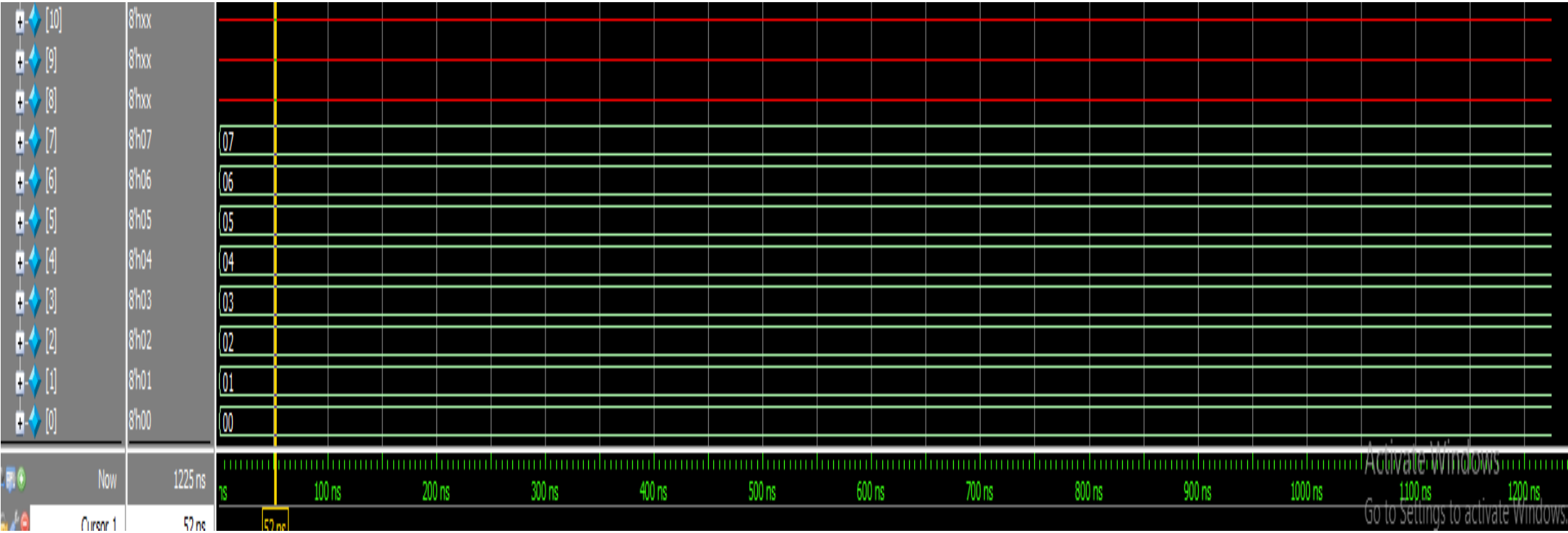
```
1 create_project project_SPI_ram C:/Users/M/Desktop/projectspislave -part xc7a35ticpg236-1L -force
2
3 add_files ram_spi.v spi_slave.v wrapper.v basys_master.xdc
4
5 synth_design -rtl -top spi_wrapper > elab.log
6 #report_timing_summary -delay_type min_max -report_unconstrained -check_timing_verbos -max_paths 10 -input_pins -routable_nets -name tim
7
8 write_schematic elaborated_schematic.pdf -format pdf -force
9
10 launch_runs synth_1 > synth.log
11
12 wait_on_run synth_1
13 open_run synth_1
14
15 write_schematic synthesized_schematic.pdf -format pdf -force
16
17 write_verilog -force SPI_netlist.v
18
19 launch_runs impl_1 -to_step write_bitstream
20
21 wait_on_run impl_1
22 open_run impl_1
23
24 open_hw
25
26 connect_hw_server
```

Note : here I want to make schematic after synthesis as pdf in file and write it in tcl but when run no pdf appear and no errors or critical warning appear .

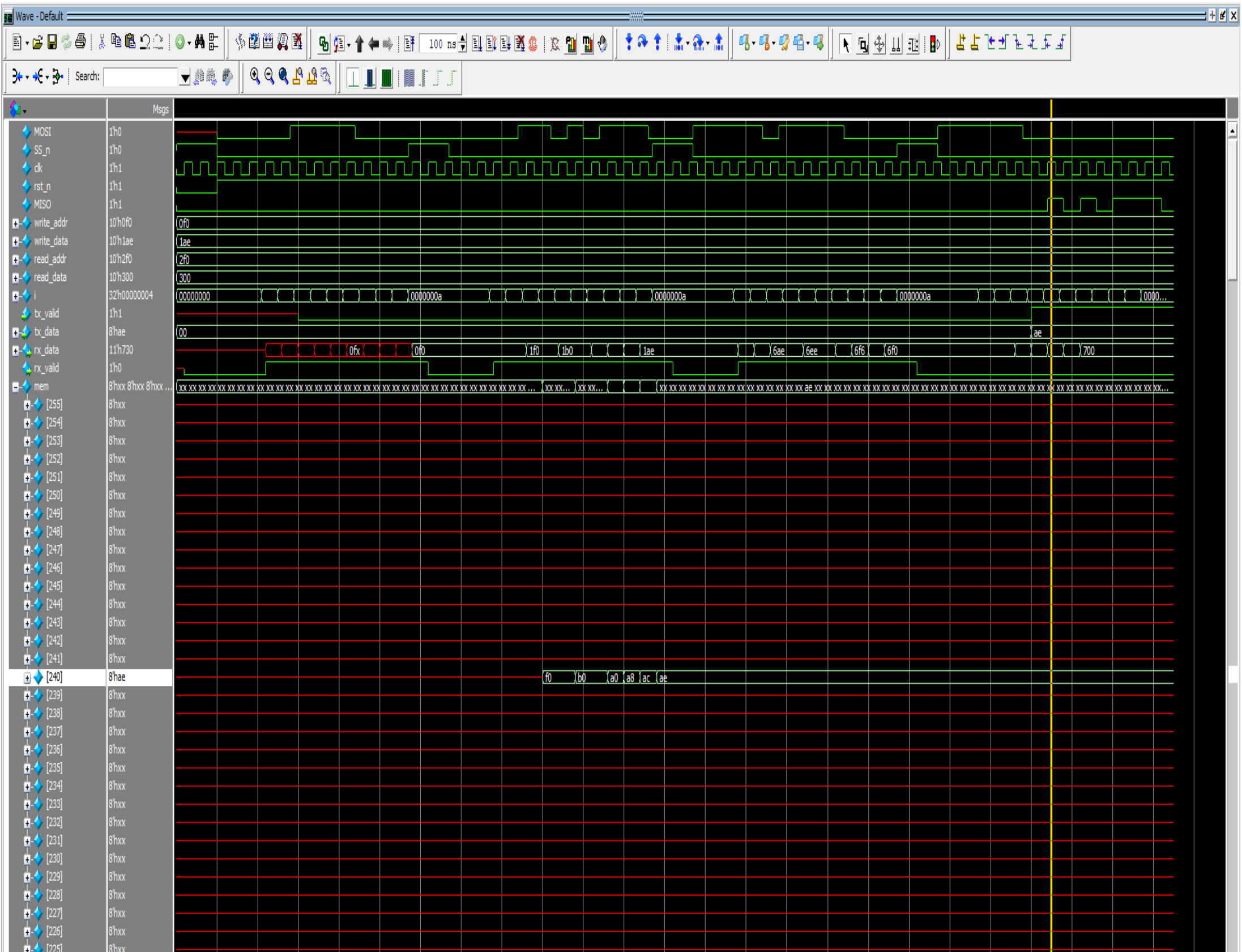
Constrain file :

```
1 ## This file is a general .xdc for the Basys3 rev B board
2 ## To use it in a project:
3 ## - uncomment the lines corresponding to used pins
4 ## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6 ## Clock signal
7 set_property -dict { PACKAGE_PIN W5 IOSTANDARD LVCMOS33 } [get_ports clk]
8 create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]
9
10
11 ## Switches
12 set_property -dict { PACKAGE_PIN V17 IOSTANDARD LVCMOS33 } [get_ports {rst_n}]
13 set_property -dict { PACKAGE_PIN V16 IOSTANDARD LVCMOS33 } [get_ports {SS_n}]
14 set_property -dict { PACKAGE_PIN W16 IOSTANDARD LVCMOS33 } [get_ports {MOSI}]
15 # set_property -dict { PACKAGE_PIN W17 IOSTANDARD LVCMOS33 } [get_ports {A[0]}]
16 # set_property -dict { PACKAGE_PIN W15 IOSTANDARD LVCMOS33 } [get_ports {A[1]}]
17 # set_property -dict { PACKAGE_PIN V15 IOSTANDARD LVCMOS33 } [get_ports {A[2]}]
18 # set_property -dict { PACKAGE_PIN W14 IOSTANDARD LVCMOS33 } [get_ports {B[0]}]
19 # set_property -dict { PACKAGE_PIN W13 IOSTANDARD LVCMOS33 } [get_ports {B[1]}]
20 # set_property -dict { PACKAGE_PIN V2 IOSTANDARD LVCMOS33 } [get_ports {B[2]}]
21 # set_property -dict { PACKAGE_PIN T3 IOSTANDARD LVCMOS33 } [get_ports {cin}]
22 # set_property -dict { PACKAGE_PIN T2 IOSTANDARD LVCMOS33 } [get_ports {red_op_A}]
23 # set_property -dict { PACKAGE_PIN R3 IOSTANDARD LVCMOS33 } [get_ports {red_op_B}]
24 # set_property -dict { PACKAGE_PIN W2 IOSTANDARD LVCMOS33 } [get_ports {bypass_A}]
25 # set_property -dict { PACKAGE_PIN U1 IOSTANDARD LVCMOS33 } [get_ports {bypass_B}]
26 # set_property -dict { PACKAGE_PIN T1 IOSTANDARD LVCMOS33 } [get_ports {direction}]
27 # set_property -dict { PACKAGE_PIN R2 IOSTANDARD LVCMOS33 } [get_ports {serial_in}]
28
29
30 ## LEDs
31 set_property -dict { PACKAGE_PIN U16 IOSTANDARD LVCMOS33 } [get_ports {MISO}]
32 # set_property -dict { PACKAGE_PIN E19 IOSTANDARD LVCMOS33 } [get_ports {leds[1]}]
33 # set_property -dict { PACKAGE_PIN U19 IOSTANDARD LVCMOS33 } [get_ports {leds[2]}]
34 # set_property -dict { PACKAGE_PIN V19 IOSTANDARD LVCMOS33 } [get_ports {leds[3]}]
35 # set_property -dict { PACKAGE_PIN W18 IOSTANDARD LVCMOS33 } [get_ports {leds[4]}]
36 # set_property -dict { PACKAGE_PIN U15 IOSTANDARD LVCMOS33 } [get_ports {leds[5]}]
37 # set_property -dict { PACKAGE_PIN U14 IOSTANDARD LVCMOS33 } [get_ports {leds[6]}]
```

Simulation in questasim :
as we see the data load as in mem.dat file



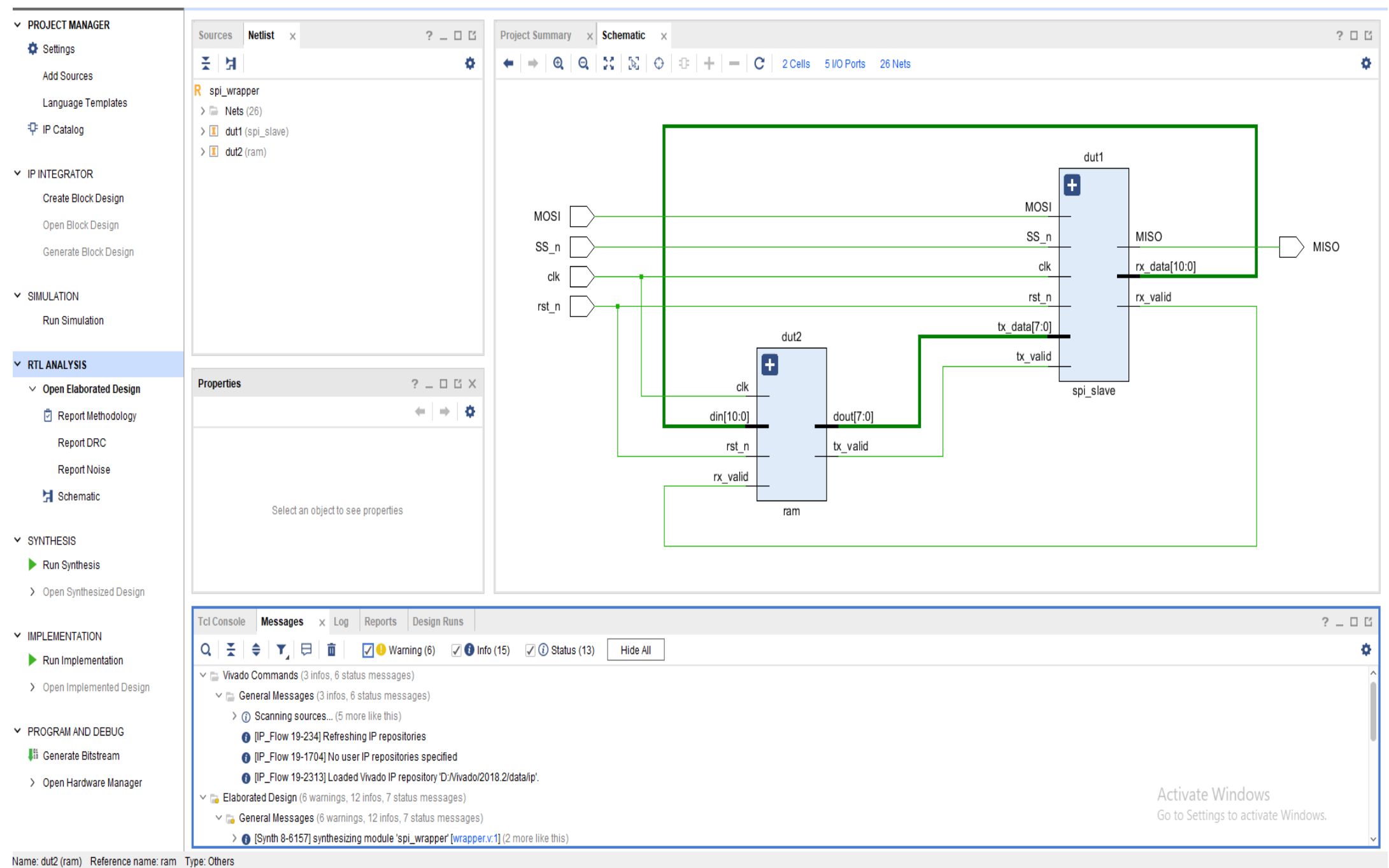
as we see the value loaded in address 240 (ae) and the value that we want in this same address will the same in miso (10101111):



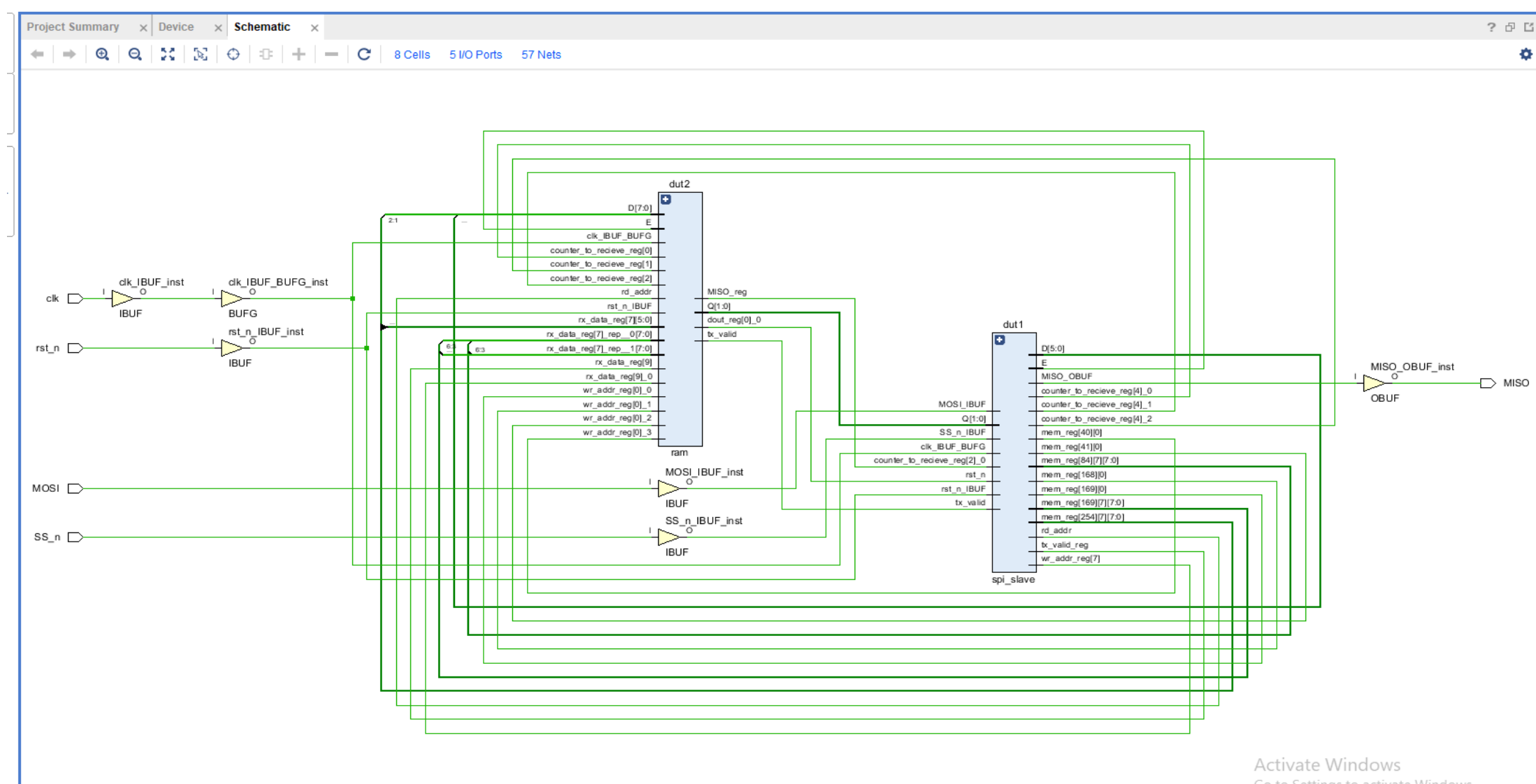
Vivado :

Gray encoding :

Schematic after elaborated without error :



Schematic after synthesis :



Schematic without error :

Flow Navigator

- Create Block Design
- Open Block Design
- Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Set Up Debug
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design

SYNTHESIZED DESIGN - xc7a35t1cp236-1L (active)

Netlist

Net Properties

Project Summary

Device

Schematic

8 Cells 5 I/O Ports 57 Nets

Tcl Console

Messages

Log

Reports

Design Runs

Warning (22) Info (164) Status (30) Hide All

Vivado Commands (3 infos, 6 status messages)

General Messages (3 infos, 6 status messages)

Scanning sources... (5 more like this)

[IP_Flow 19-234] Refreshing IP repositories

[IP_Flow 19-1704] No user IP repositories specified

[IP_Flow 19-2313] Loaded Vivado IP repository 'D:/vivado/2018.2/data/ip'

Elaborated Design (6 warnings, 12 infos, 11 status messages)

General Messages (6 warnings, 12 infos, 11 status messages)

[Synth 8-6157] synthesizing module 'spi_wrapper' [wrapper.v:1] (2 more like this)

Activate Windows
Go to Settings to activate Windows.

Time report :

Flow Navigator

- Create Block Design
- Open Block Design
- Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Open Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic
- SYNTHESIS
 - Run Synthesis
 - Open Synthesized Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Set Up Debug
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic
- IMPLEMENTATION
 - Run Implementation
 - Open Implemented Design

SYNTHESIZED DESIGN - xc7a35t1cp236-1L (active)

Netlist

Path Properties

Project Summary

Device

Schematic

8 Cells 5 I/O Ports 57 Nets

Tcl Console

Messages

Log

Reports

Design Runs

Timing

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	5.411	3	4	29	dut1/counter_to_recieve_reg[17]/C	dut1/counter_to_recieve_reg[10]/R	3.976	0.999	2.977	10.0	sys_clk_pin	sys_clk_pin
Path 2	5.411	3	4	29	dut1/counter_to_recieve_reg[17]/C	dut1/counter_to_recieve_reg[11]/R	3.976	0.999	2.977	10.0	sys_clk_pin	sys_clk_pin
Path 3	5.411	3	4	29	dut1/counter_to_recieve_reg[17]/C	dut1/counter_to_recieve_reg[12]/R	3.976	0.999	2.977	10.0	sys_clk_pin	sys_clk_pin
Path 4	5.411	3	4	29	dut1/counter_to_recieve_reg[17]/C	dut1/counter_to_recieve_reg[13]/R	3.976	0.999	2.977	10.0	sys_clk_pin	sys_clk_pin
Path 5	5.411	3	4	29	dut1/counter_to_recieve_reg[17]/C	dut1/counter_to_recieve_reg[14]/R	3.976	0.999	2.977	10.0	sys_clk_pin	sys_clk_pin
Path 6	5.411	3	4	29	dut1/counter_to_recieve_reg[17]/C	dut1/counter_to_recieve_reg[15]/R	3.976	0.999	2.977	10.0	sys_clk_pin	sys_clk_pin

Timing Summary - timing_1

Setup 5.411 ns (10)

Activate Windows
Go to Settings to activate Windows.

Gray encoding :

Sources **Netlist** ? — □ ✕

counter_to_recieve_reg[4] (FDRE)
 counter_to_recieve_reg[5] (FDRE)
 counter_to_recieve_reg[6] (FDRE)
 counter_to_recieve_reg[7] (FDRE)
 counter_to_recieve_reg[8] (FDRE)
 counter_to_recieve_reg[9] (FDRE)
counter_to_recieve_reg[10] (FDRE)
 counter_to_recieve_reg[11] (FDRE)
 counter_to_recieve_reg[12] (FDRE)
 counter_to_recieve_reg[13] (FDRE)
 counter_to_recieve_reg[14] (FDRE)
 counter_to_recieve_reg[15] (FDRE)
 counter_to_recieve_reg[16] (FDRE)
counter_to_recieve_reg[17] (FDRE)

Project Summary **Device** **Schematic** **synth_1_synth_synthesis_report_0 - synth_1** ✕

F:/project_SPI/project_SPI/runs/synth_1/spi_wrapper.vds

encodi **Next** **Previous** **Highlight** ☐ Match Case ☐ Whole Words 4 Match(es)

```

100 INFO: [Synth 8-5544] ROM "counter" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
101 INFO: [Synth 8-5544] ROM "control_bit" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
102 INFO: [Synth 8-5544] ROM "rx_valid" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
103 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
104 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
105 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
106 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
107 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
108 INFO: [Synth 8-5544] ROM "dout" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
109 INFO: [Synth 8-5544] ROM "wr_addr" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
110 INFO: [Synth 8-5544] ROM "tx_valid" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
111 -----
112 State | New Encoding | Previous Encoding
113 -----
114 IDLE | 000 | 000
115 CHK_CMD | 001 | 011
116 WRITE | 011 | 100
117 READ_ADD | 010 | 010
118 READ_DATA | 111 | 001
119 -----
120 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'spi_slave'
121 WARNING: [Synth 8-327] inferring latch for variable 'FSM_gray_ns_reg' [C:/Users/M/Desktop/project_spi/spi_slave.v:33]
122 WARNING: [Synth 8-327] inferring latch for variable 'address_or_read_reg' [C:/Users/M/Desktop/project_spi/spi_slave.v:41]
123 -----
124 Finished RIL Optimization Phase 2 : Time (s): cpu = 00:00:37 ; elapsed = 00:00:39 . Memory (MB): peak = 838.695 ; gain = 526.020
125 -----
126
127 Report RIL Partitions:

```

Path Properties ? — □ ✕

Path 1 ◀ ▶ ⚙

Summary

Name	Path 1
Slack	5.411ns
Source	dut1/counter_to_recieve_reg[17]/C (rising edge)
Destination	dut1/counter_to_recieve_reg[10]/R (rising edge)
Path Group	sys_clk_pin

General Properties **Report** Cells Nets Net Segs

Tcl Console **Messages** **Log** **Reports** **Design Runs** **Timing**

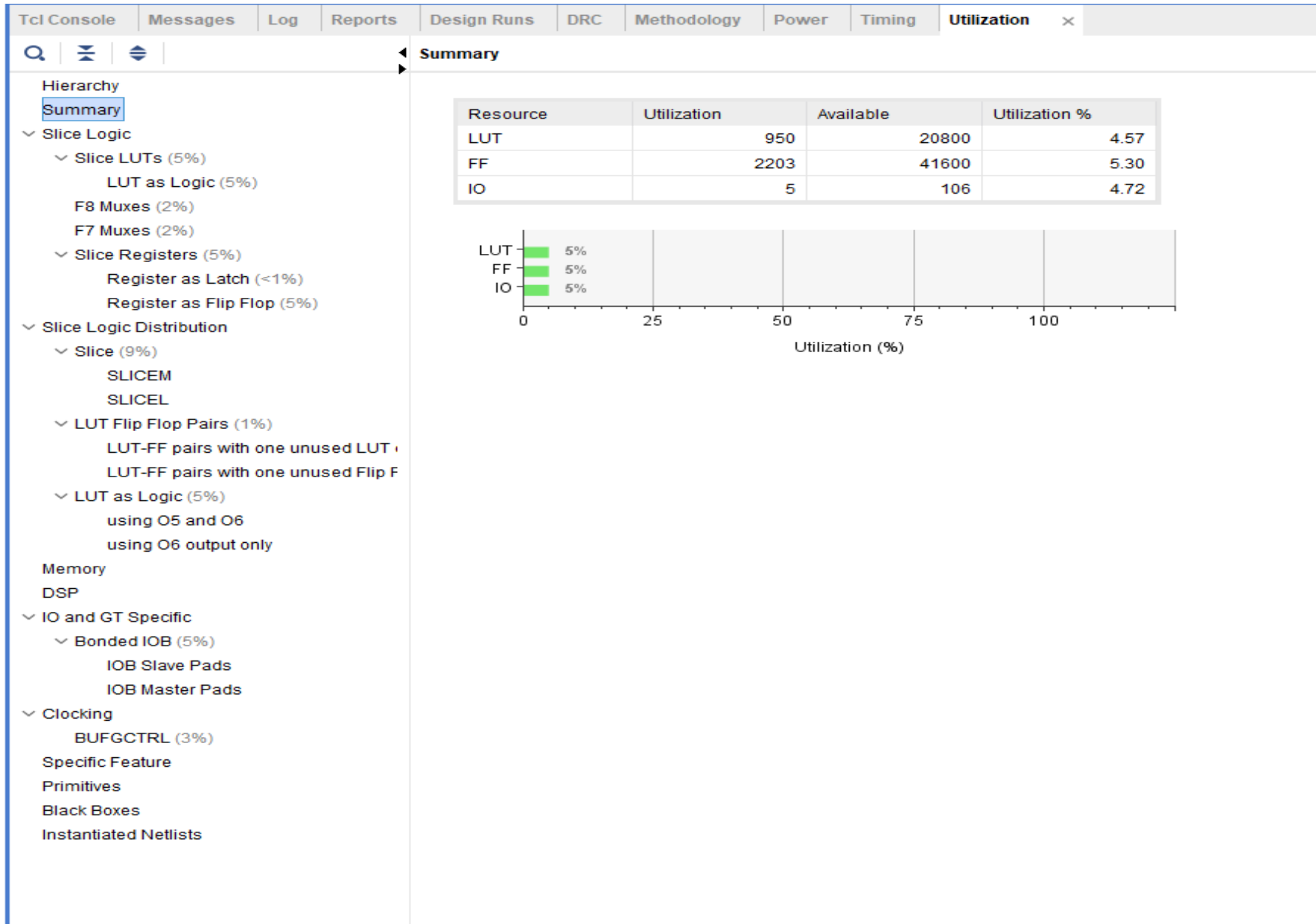
Report **Report Type** **Options** **Modified** **Size**

Report	Report Type	Options	Modified	Size
▼ Synthesis				
▼ Synth Design (synth_design)				
synth_1_synth_report_utilization_0	Report on utilization of resources on the targeted device (report_utilization)		8/21/23 1...	7.1 KB
synth_1_synth_synthesis_report_0	Vivado Synthesis Report		8/21/23 1...	32.5 KB
▼ Implementation				
impl_1				

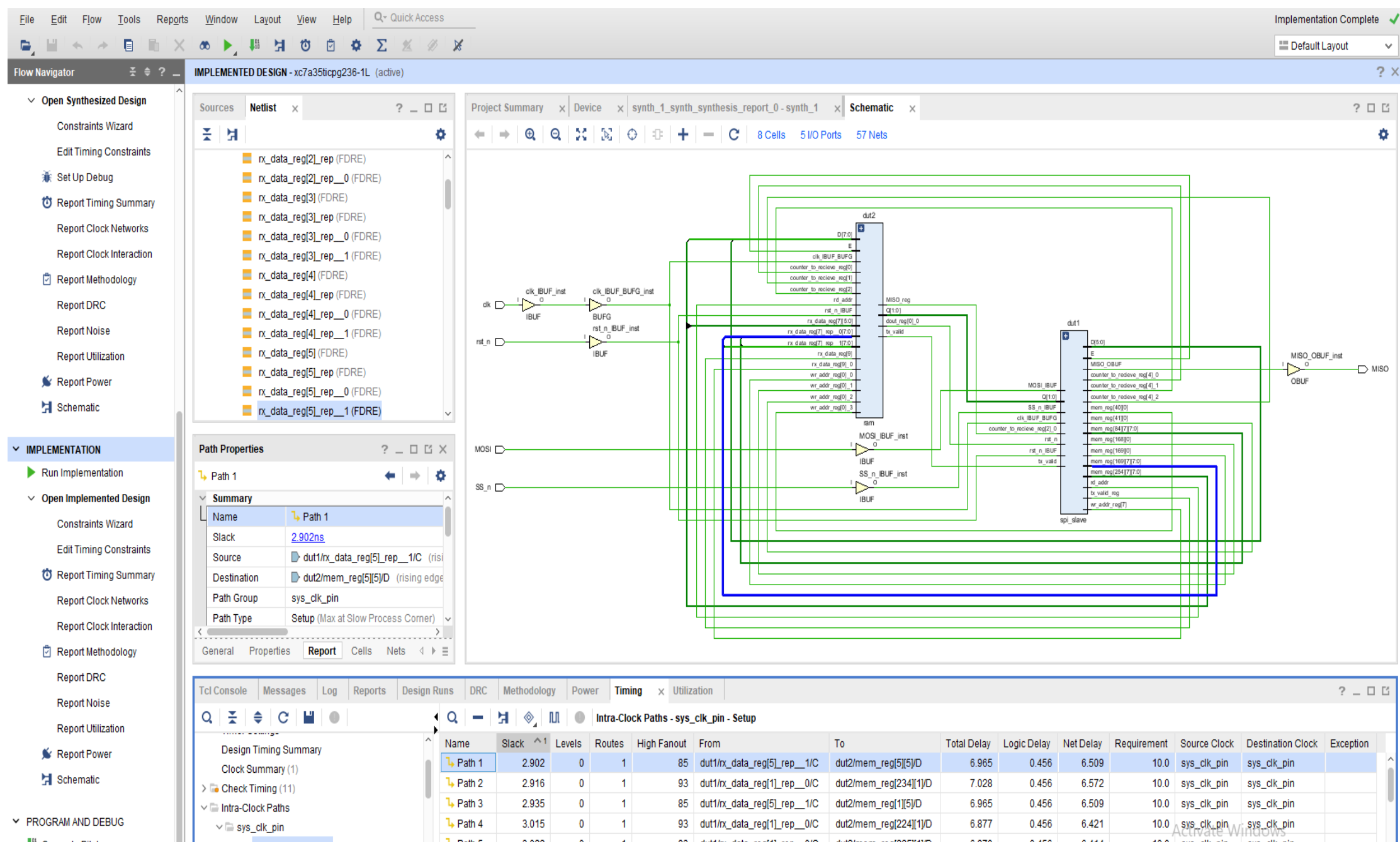
Implementation device and no error :

The screenshot displays the Xilinx Vivado IDE interface during the implementation phase. The top status bar confirms 'Implementation Complete'. The left-hand 'Flow Navigator' pane is set to 'Open Implemented Design', listing various reports and constraints. The central workspace is divided into several panes: 'Sources' showing a netlist of memory registers (mem_reg[4][0] to mem_reg[5][5]), 'Path Properties' for 'Path 1' showing a setup time of 2.902ns, and a large 'Device' view showing a dark, mostly empty chip layout. The bottom pane is the 'Messages' window, displaying Vivado commands and general messages, including IP repository updates and warnings.

Utilization report :



worst_slack in implementaion_gray:



Successful generate bit:

Bitstream Generation Completed

Bitstream Generation successfully completed.

Next:

- ☒ View Reports
- ☐ Open Hardware Manager
- ☐ Generate Memory Configuration File
- ☐ Don't show this dialog again

Path Properties - Path 1

Name	Slack	Source	Destination	Path Group	Path Type
Path 1	2.902ns	dut1/rx_data_reg[5]_rep__1/C (rising edge)	dut2/mem_reg[5][5]D (rising edge)	sys_clk_pin	Setup (Max at Slow Process Corner)

Timing Report: Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception
Path 1	2.902	0	1	85	dut1/rx_data_reg[5]_rep__1/C	dut2/mem_reg[5][5]D	6.965	0.456	6.509	10.0	sys_clk_pin	sys_clk_pin	
Path 2	2.916	0	1	93	dut1/rx_data_reg[1]_rep__0/C	dut2/mem_reg[234][1]D	7.028	0.456	6.572	10.0	sys_clk_pin	sys_clk_pin	
Path 3	2.935	0	1	85	dut1/rx_data_reg[5]_rep__1/C	dut2/mem_reg[1][5]D	6.965	0.456	6.509	10.0	sys_clk_pin	sys_clk_pin	
Path 4	3.015	0	1	93	dut1/rx_data_reg[1]_rep__0/C	dut2/mem_reg[224][1]D	6.877	0.456	6.421	10.0	sys_clk_pin	sys_clk_pin	
Path 5	3.022	0	1	93	dut1/rx_data_reg[1]_rep__0/C	dut2/mem_reg[225][1]D	6.870	0.456	6.414	10.0	sys_clk_pin	sys_clk_pin	

One_hot_encoding : schematic after elaborated without error :

Sources

- Netlist
- spi_wrapper
 - Nets (26)
 - dut1 (spi_slave)
 - dut2 (ram)

Properties

Select an object to see properties

Schematic

2 Cells 5 I/O Ports 26 Nets

Messages

- Vivado Commands (3 Infos, 6 status messages)
 - General Messages (3 Infos, 6 status messages)
 - Scanning sources... (5 more like this)
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/vivado/2018.2/data/ip'.
 - Elaborated Design (2 Infos, 5 status messages)
 - General Messages (2 Infos, 5 status messages)

Schematic after synthesis with no error:

SYNTHESIZED DESIGN - xc7a35t1cp236-1L (active)

Sources Netlist x ? - □ □

Project Summary x Device x Schematic x ? □ □

8 Cells 5 I/O Ports 57 Nets

Properties ? - □ □ x

Select an object to see properties

Tcl Console Messages x Log Reports Design Runs Timing ? - □ □

Vivado Commands (3 infos, 6 status messages)

- General Messages (3 infos, 6 status messages)
 - Scanning sources... (5 more like this)
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Vivado/2018.2/data/ip'.
- Elaborated Design (2 infos, 7 status messages)
 - General Messages (2 infos, 7 status messages)
 - [Project 1-570] Preparing netlist for logic optimization

Activate Windows
Go to Settings to activate Windows.

Time report after synthesis the same:

Flow Navigator SYNTHESIZED DESIGN - xc7a35t1cp236-1L (active)

Sources Netlist x ? - □ □

Project Summary x Device x Schematic x synth_1_synth_synthesis_report_0 - synth_1 x ? □ □

8 Cells 5 I/O Ports 57 Nets

Path Properties ? - □ □ x

Path 1

Summary

Name	Slack
Path 1	5.411ns

General Properties Report Cells Nets Net Seg 4

Tcl Console Messages Log Reports Design Runs Timing x

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Path 1	5.411	3	4	29	dut1/counter_to_recieve_reg[4]/C	dut1/counter_to_recieve_reg[10]/R	3.976	0.999	2.977	10.0	sys_clk_pin	sys_clk_pin
Path 2	5.411	3	4	29	dut1/counter_to_recieve_reg[4]/C	dut1/counter_to_recieve_reg[11]/R	3.976	0.999	2.977	10.0	sys_clk_pin	sys_clk_pin
Path 3	5.411	3	4	29	dut1/counter_to_recieve_reg[4]/C	dut1/counter_to_recieve_reg[12]/R	3.976	0.999	2.977	10.0	sys_clk_pin	sys_clk_pin
Path 4	5.411	3	4	29	dut1/counter_to_recieve_reg[4]/C	dut1/counter_to_recieve_reg[13]/R	3.976	0.999	2.977	10.0	sys_clk_pin	sys_clk_pin
Path 5	5.411	3	4	29	dut1/counter_to_recieve_reg[4]/C	dut1/counter_to_recieve_reg[14]/R	3.976	0.999	2.977	10.0	sys_clk_pin	sys_clk_pin
Path 6	5.411	3	4	29	dut1/counter_to_recieve_reg[4]/C	dut1/counter_to_recieve_reg[15]/R	3.976	0.999	2.977	10.0	sys_clk_pin	sys_clk_pin

Timing Summary - timing_1

Setup 5.411 ns (10)

One_hot encoding :

SYNTHESIZED DESIGN - xc7a35t1cpg236-1L (active)

Sources Netlist x

- counter_to_recieve[31]_i_2 (LUT5)
- counter_to_recieve[31]_i_3 (LUT5)
- counter_to_recieve[31]_i_4 (LUT5)
- counter_to_recieve[31]_i_5 (LUT5)
- counter_to_recieve[31]_i_6 (LUT5)
- counter_to_recieve[31]_i_7 (LUT4)
- counter_to_recieve[31]_i_8 (LUT4)
- counter_to_recieve[31]_i_9 (LUT4)
- counter_to_recieve[31]_i_10 (LUT4)
- counter_to_recieve_reg[0] (FDRE)
- counter_to_recieve_reg[1] (FDRE)
- counter_to_recieve_reg[2] (FDRE)
- counter_to_recieve_reg[3] (FDRE)
- counter_to_recieve_reg[4] (FDRE)

Path Properties

Path 1

Summary

Name	Path 1
Slack	5.411ns
Source	dut1/counter_to_recieve_reg[4]/C (rising edge)
Destination	dut1/counter_to_recieve_reg[10]/R (rising edge)
Path Group	sys_clk_pin

General Properties Report Cells Nets Net Seg4

Project Summary x Device x Schematic x synth_1_synth_synthesis_report_0 - synth_1 x

F:/project_SPI/project_SPI.runs/synth_1/spi_wrapper.vds

end Next Previous Highlight Match Case Whole Words 6 Match(es)

```
96 INFO: [Synth 8-802] inferred FSM for state register 'cs_reg' in module 'spi_slave'
97 INFO: [Synth 8-5545] ROM "counter" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
98 INFO: [Synth 8-5545] ROM "counter_to_recieve" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
99 INFO: [Synth 8-5545] ROM "counter_to_recieve" won't be mapped to RAM because address size (32) is larger than maximum supported(25)
100 INFO: [Synth 8-5544] ROM "counter" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
101 INFO: [Synth 8-5544] ROM "control_bit" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
102 INFO: [Synth 8-5544] ROM "rx_valid" won't be mapped to Block RAM because address size (3) smaller than threshold (5)
103 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
104 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
105 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
106 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
107 INFO: [Synth 8-5544] ROM "ns" won't be mapped to Block RAM because address size (1) smaller than threshold (5)
108 INFO: [Synth 8-5544] ROM "dout" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
109 INFO: [Synth 8-5544] ROM "wr_addr" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
110 INFO: [Synth 8-5544] ROM "tx_valid" won't be mapped to Block RAM because address size (2) smaller than threshold (5)
111
112 State | New Encoding | Previous Encoding
113 -----|-----|-----
114 IDLE | 00001 | 000
115 CHK_CMD | 00010 | 011
116 WRITE | 00100 | 100
117 READ_ADD | 01000 | 010
118 READ_DATA | 10000 | 001
119
120 INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'spi_slave'
121 WARNING: [Synth 8-327] inferring latch for variable 'FSM_onehot_ns_reg' [C:/Users/M/Desktop/project spi/spi_slave.v:33]
122 WARNING: [Synth 8-327] inferring latch for variable 'address_or_read_reg' [C:/Users/M/Desktop/project spi/spi_slave.v:41]
123
```

Tcl Console Messages Log Reports Design Runs Timing x

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destin
Path 1	5.411	3	4	29	dut1/counter_to_recieve_reg[4]/C	dut1/counter_to_recieve_reg[10]/R	3.976	0.999	2.977	10.0	sys_clk_pin	sys_c

Schematic after implementation without errors :

Flow Navigator

SYNTHESIS

- Run Synthesis
- Open Synthesized Design
 - Constraints Wizard
 - Edit Timing Constraints
- Set Up Debug
- Report Timing Summary
- Report Clock Networks
- Report Clock Interaction
- Report Methodology
- Report DRC
- Report Noise
- Report Utilization

IMPLEMENTATION

- Run Implementation
- Open Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
- Report Timing Summary
- Report Clock Networks
- Report Clock Interaction
- Report Methodology
- Report DRC
- Report Noise
- Report Utilization

Schematic

Project Summary x Device x synth_1_synth_synthesis_report_0 - synth_1 x Schematic x

8 Cells 5 IO Ports 57 Nets

Sources Netlist x

- rx_data_reg[2] (FDRE)
- rx_data_reg[2]_rep (FDRE)
- rx_data_reg[2]_rep_0 (FDRE)
- rx_data_reg[3] (FDRE)
- rx_data_reg[3]_rep (FDRE)
- rx_data_reg[3]_rep_0 (FDRE)
- rx_data_reg[3]_rep_1 (FDRE)
- rx_data_reg[4] (FDRE)
- rx_data_reg[4]_rep (FDRE)
- rx_data_reg[4]_rep_0 (FDRE)
- rx_data_reg[4]_rep_1 (FDRE)
- rx_data_reg[5] (FDRE)
- rx_data_reg[5]_rep (FDRE)
- rx_data_reg[5]_rep_0 (FDRE)

Path Properties

Path 1

Summary

Name	Path 1
Slack	2.798ns
Source	dut1/rx_data_reg[5]_rep_0/C (rising edge)
Destination	dut2/mem_reg[121][5]/D (rising edge)
Path Group	sys_clk_pin
Path Type	Setup (Max at Slow Process Corner)

General Properties Report Cells Nets

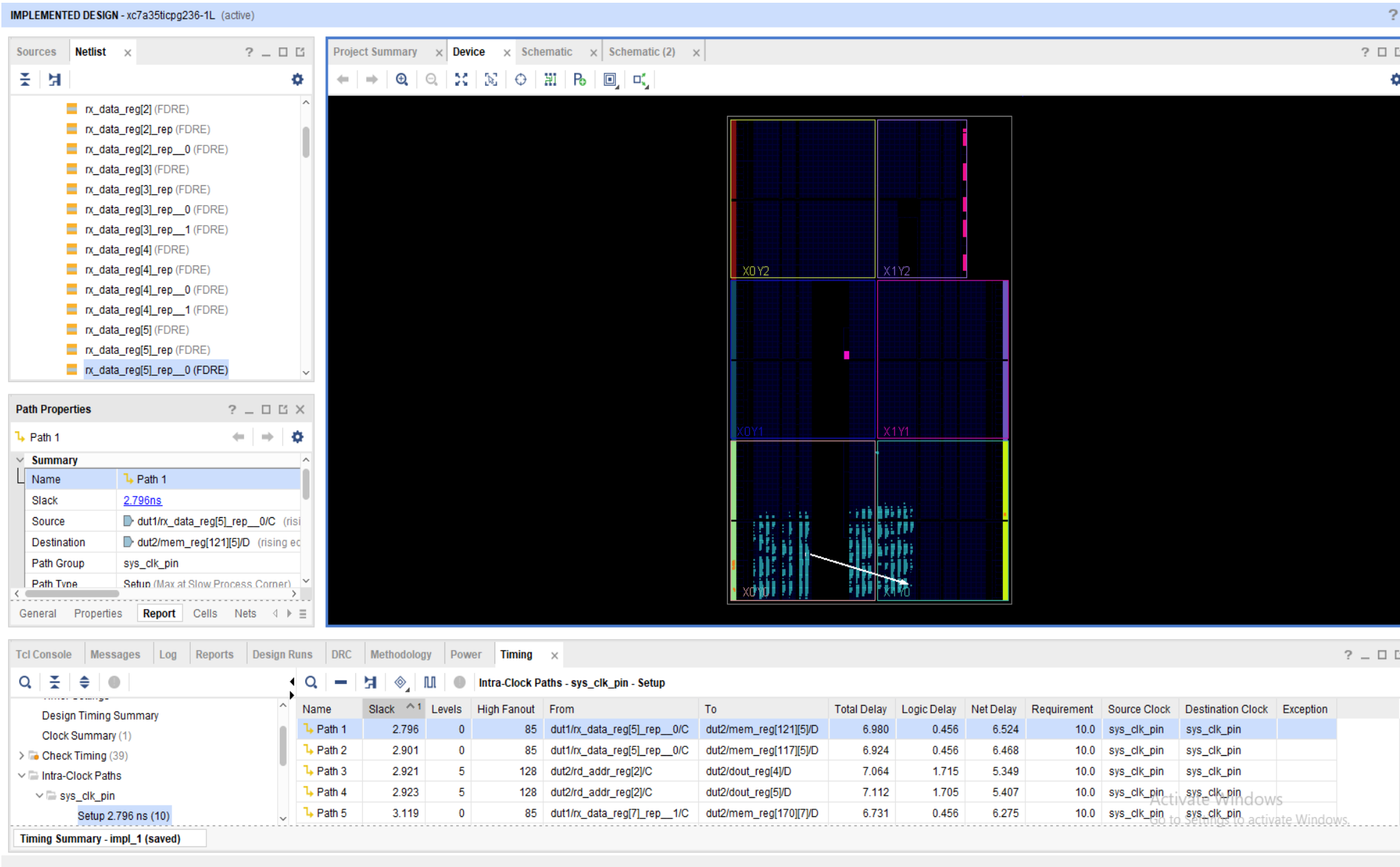
Tcl Console Messages x Log Reports Design Runs DRC Methodology Power Timing Utilization

Warning (16) Info (347) Status (481) Hide All

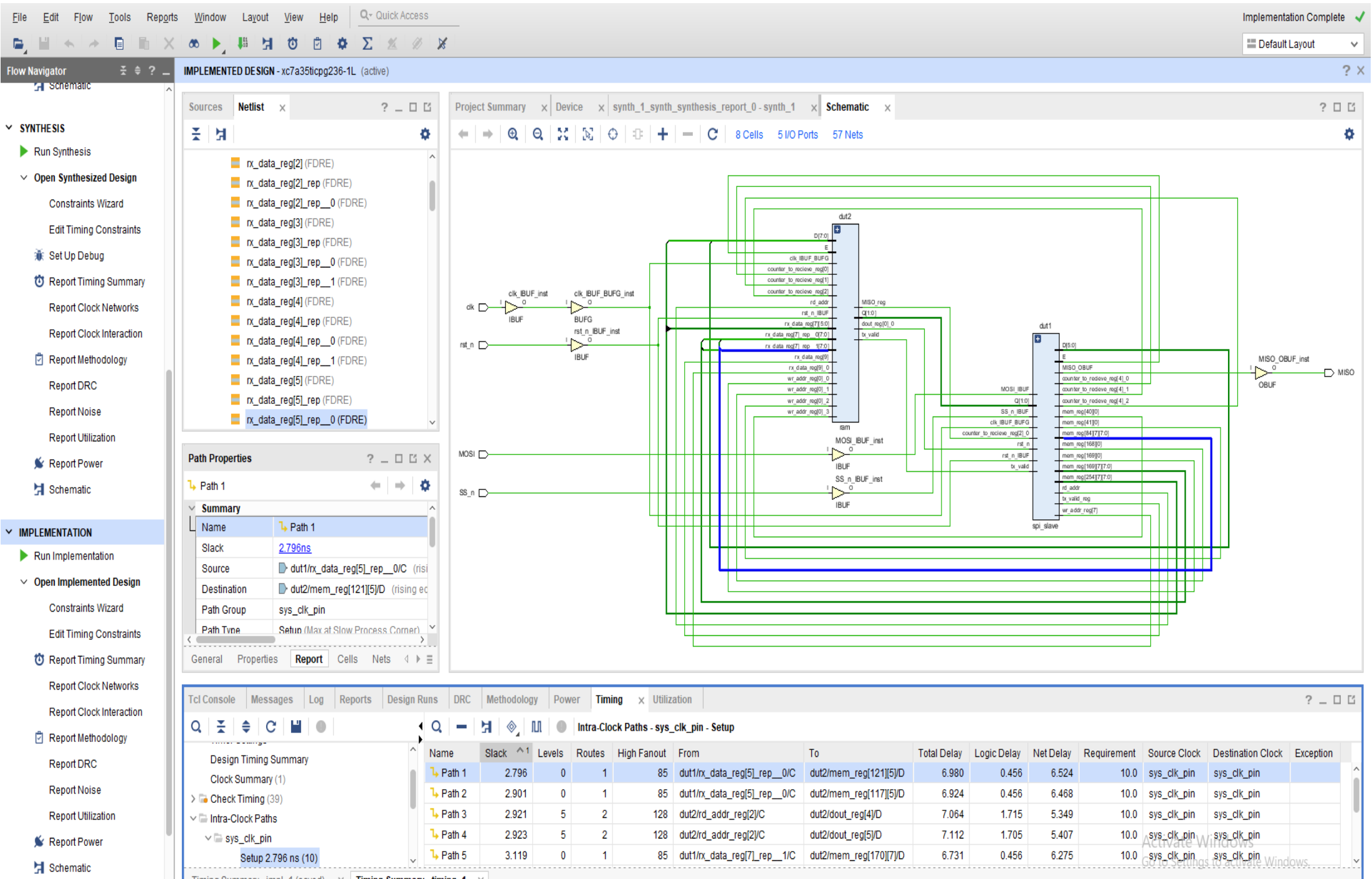
Vivado Commands (3 infos, 6 status messages)

- General Messages (3 infos, 6 status messages)
 - Scanning sources... (5 more like this)
 - [IP_Flow 19-234] Refreshing IP repositories
 - [IP_Flow 19-1704] No user IP repositories specified
 - [IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Vivado/2018.2/data/ip/
- Elaborated Design (2 infos, 7 status messages)
 - General Messages (2 infos, 7 status messages)

Device :



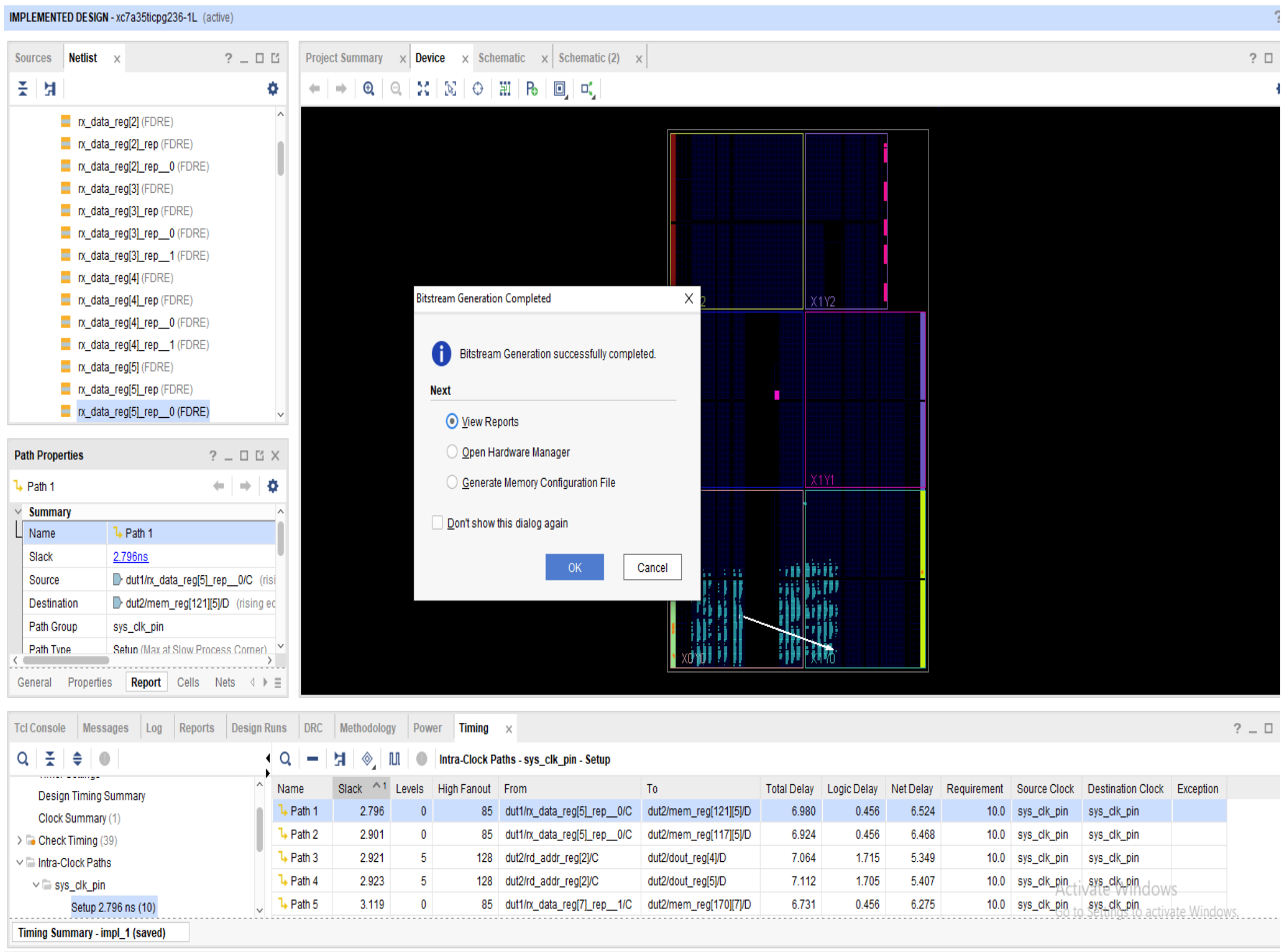
Worst slack after implementation :



Utilization report :

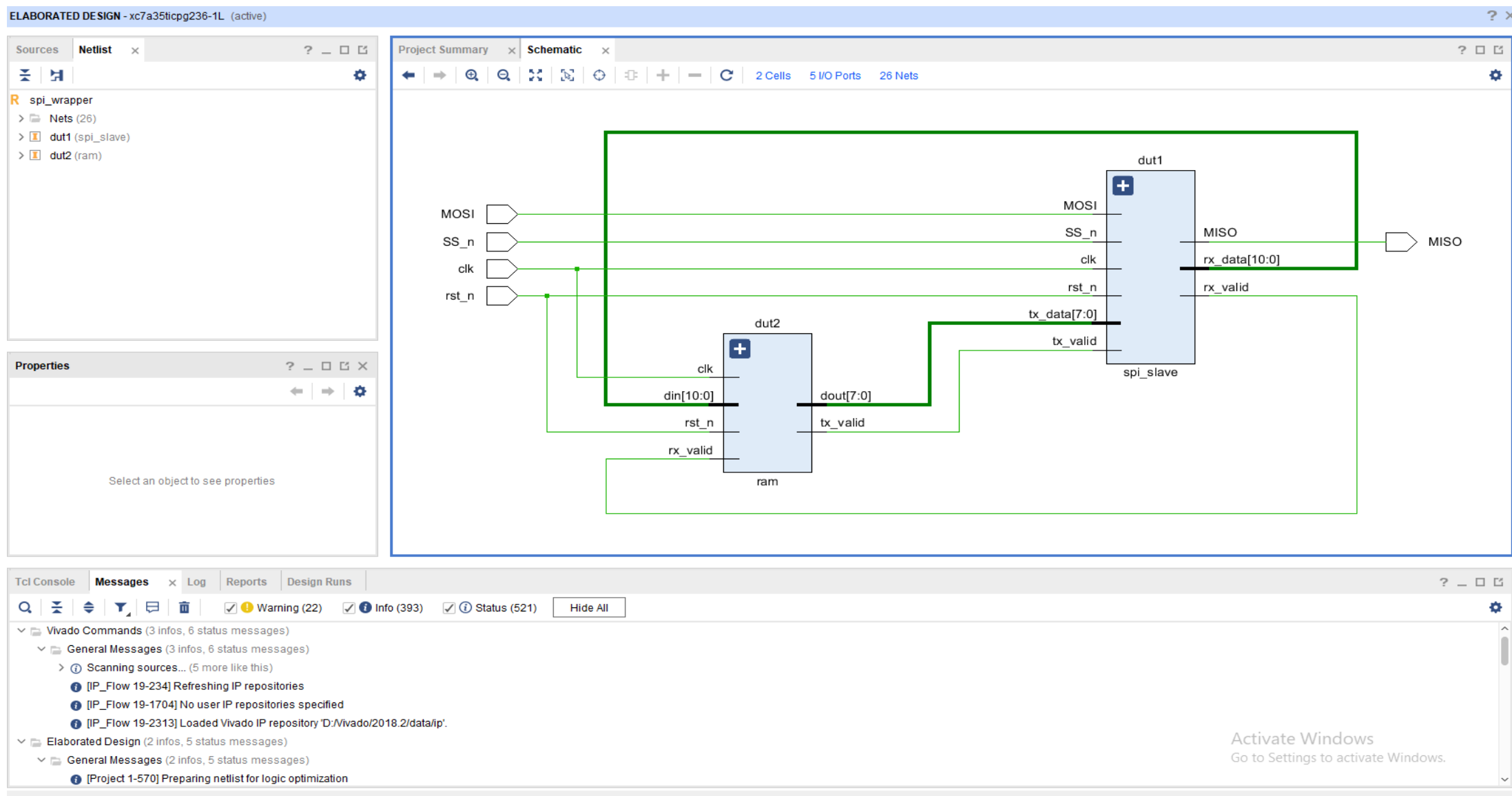


Generate bit stream successful :

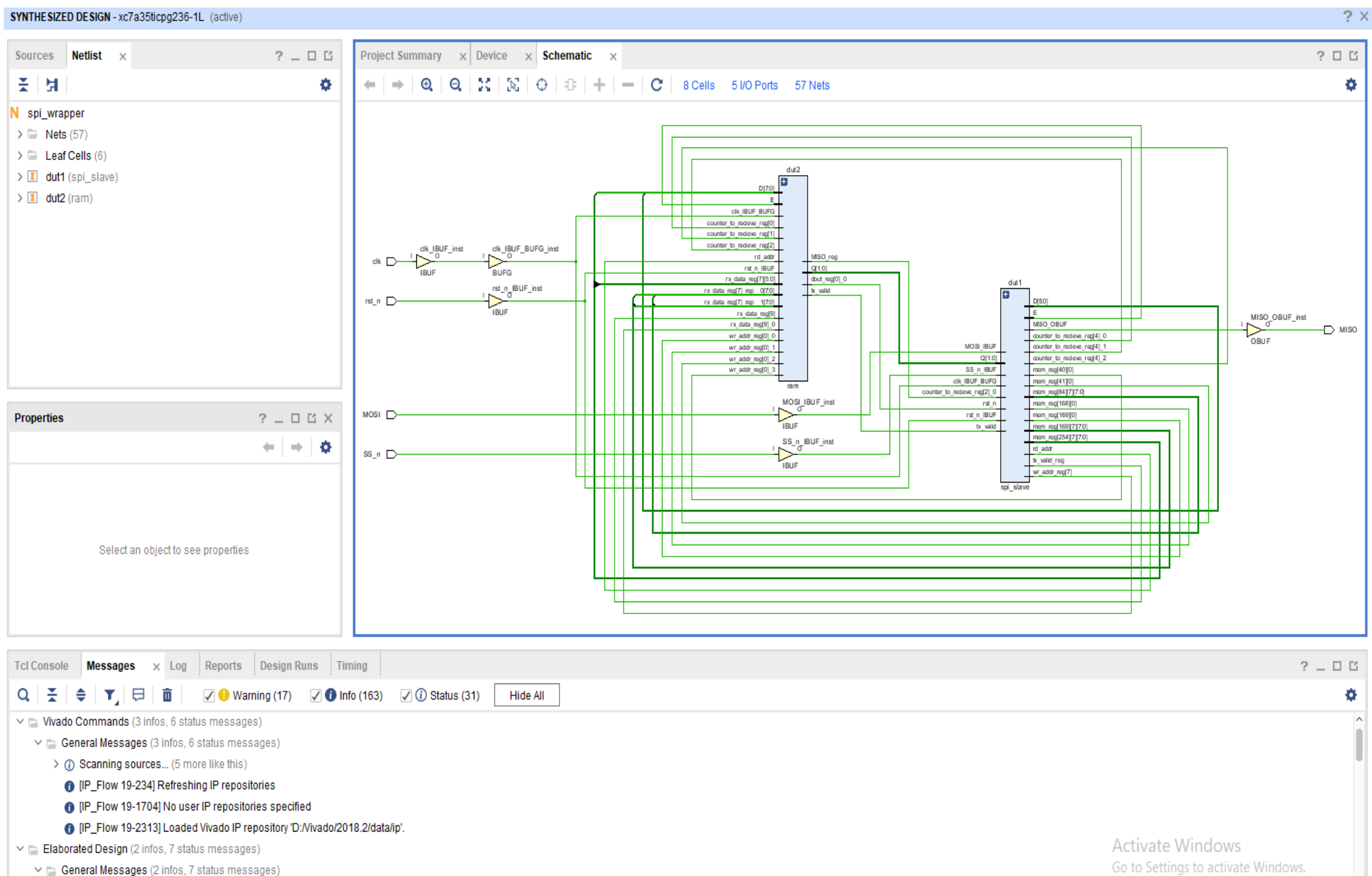


Sequential :

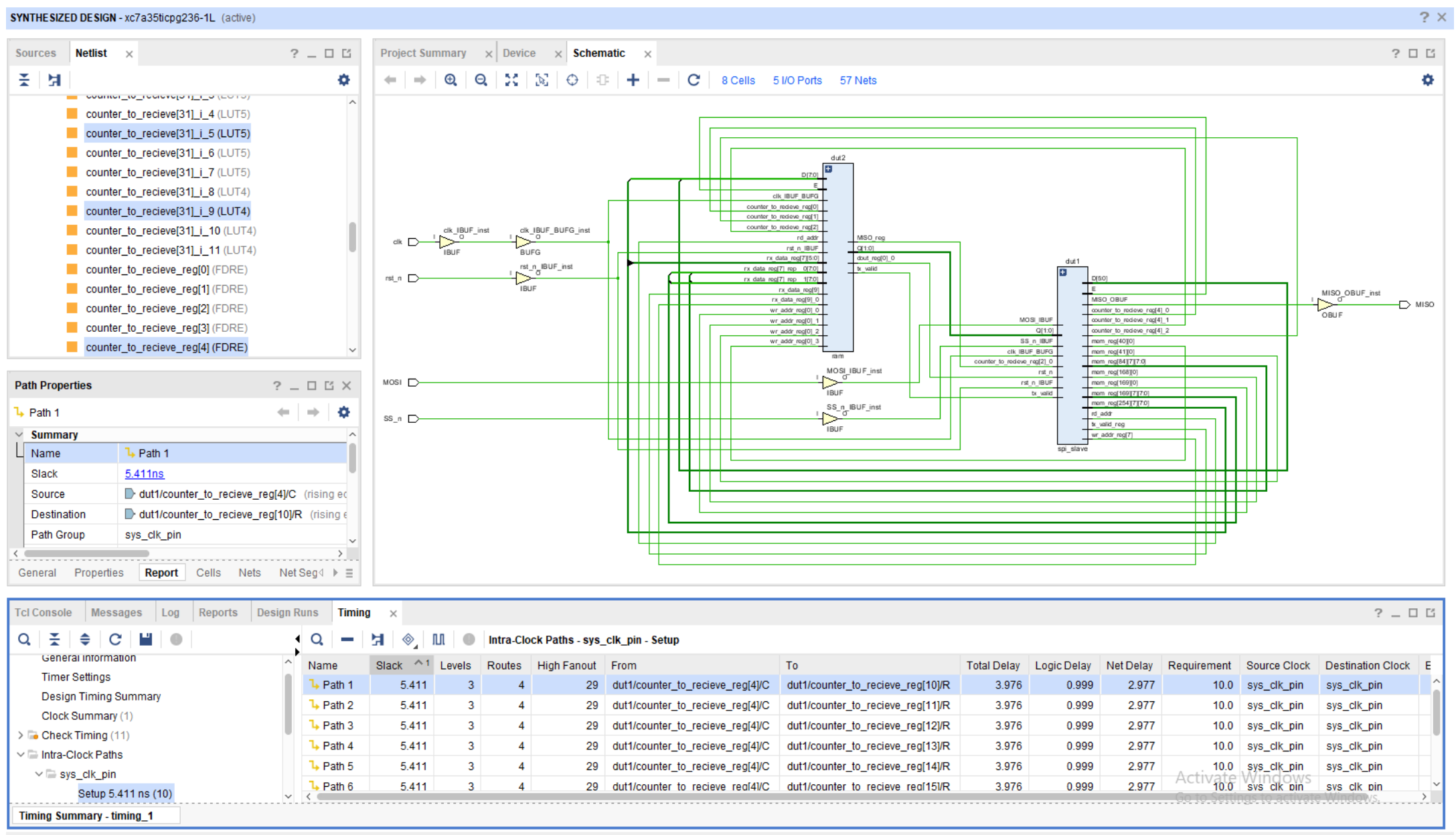
schematic after elaborated without error :



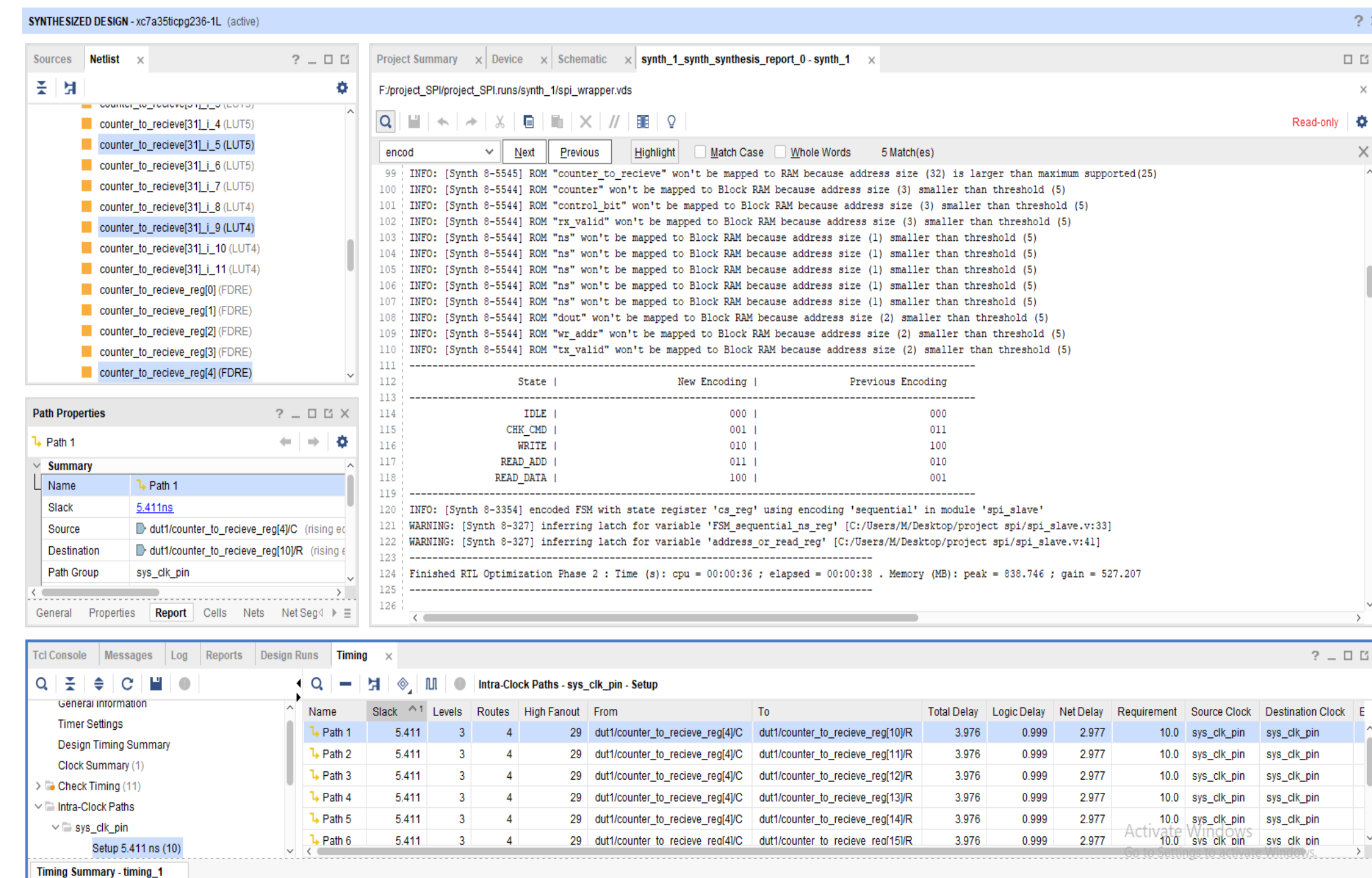
Schematic after synthesis with no error :



Time report after synthesis is same for all encoding :



Sequential encoding :



Schematic after implementation without error :

IMPLEMENTED DESIGN - xc7a35ticipg236-1L (active)

Sources Netlist x ? _ □ □

Project Summary x Device x Schematic x ? _ □ □

8 Cells 5 I/O Ports 57 Nets

Path Properties

Path 1

Summary

Name	Path 1
Slack	3.124ns
Source	dut2/rd_addr_reg[1]_rep_1/C (rising edge-tri
Destination	dut2/dout_reg[4]/D (rising edge-tri
Path Group	sys_clk_pin
Path Type	Setup (Max at Slow Process Corner)

General Properties Report Cells Nets

Tcl Console Messages x Log Reports Design Runs DRC Methodology Power Timing Utilization ? _ □ □

Warning (19) Info (345) Status (475) Hide All

Vivado Commands (3 infos, 6 status messages)

General Messages (3 infos, 6 status messages)

Scanning sources... (5 more like this)

[IP_Flow 19-234] Refreshing IP repositories

[IP_Flow 19-1704] No user IP repositories specified

[IP_Flow 19-2313] Loaded Vivado IP repository 'D:/Vivado/2018.2/data/ip'.

Elaborated Design (2 infos, 7 status messages)

General Messages (2 infos, 7 status messages)

Activate Windows
Go to Settings to activate Windows.

Device :

IMPLEMENTED DESIGN - xc7a35ticipg236-1L (active)

Sources Netlist x ? _ □ □

Project Summary x Device x ? _ □ □

Timing x Utilization ? _ □ □

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception
Path 1	3.124	6	64	dut2/rd_addr_reg[1]_rep_1/C	dut2/dout_reg[4]/D	6.863	1.646	5.217	10.0	sys_clk_pin	sys_clk_pin	
Path 2	3.390	6	64	dut2/rd_addr_reg[0]_rep_3/C	dut2/dout_reg[2]/D	6.598	1.556	5.042	10.0	sys_clk_pin	sys_clk_pin	
Path 3	3.699	6	64	dut2/rd_addr_reg[1]_rep_4/C	dut2/dout_reg[1]/D	6.337	1.685	4.652	10.0	sys_clk_pin	sys_clk_pin	
Path 4	3.901	6	64	dut2/rd_addr_reg[1]_rep/C	dut2/dout_reg[6]/D	6.087	1.651	4.436	10.0	sys_clk_pin	sys_clk_pin	
Path 5	3.907	0	93	dut1/rx_data_reg[1]_rep_0/C	dut2/mem_reg[172]/1/D	5.892	0.518	5.374	10.0	sys_clk_pin	sys_clk_pin	

Design Timing Summary

Clock Summary (1)

Check Timing (11)

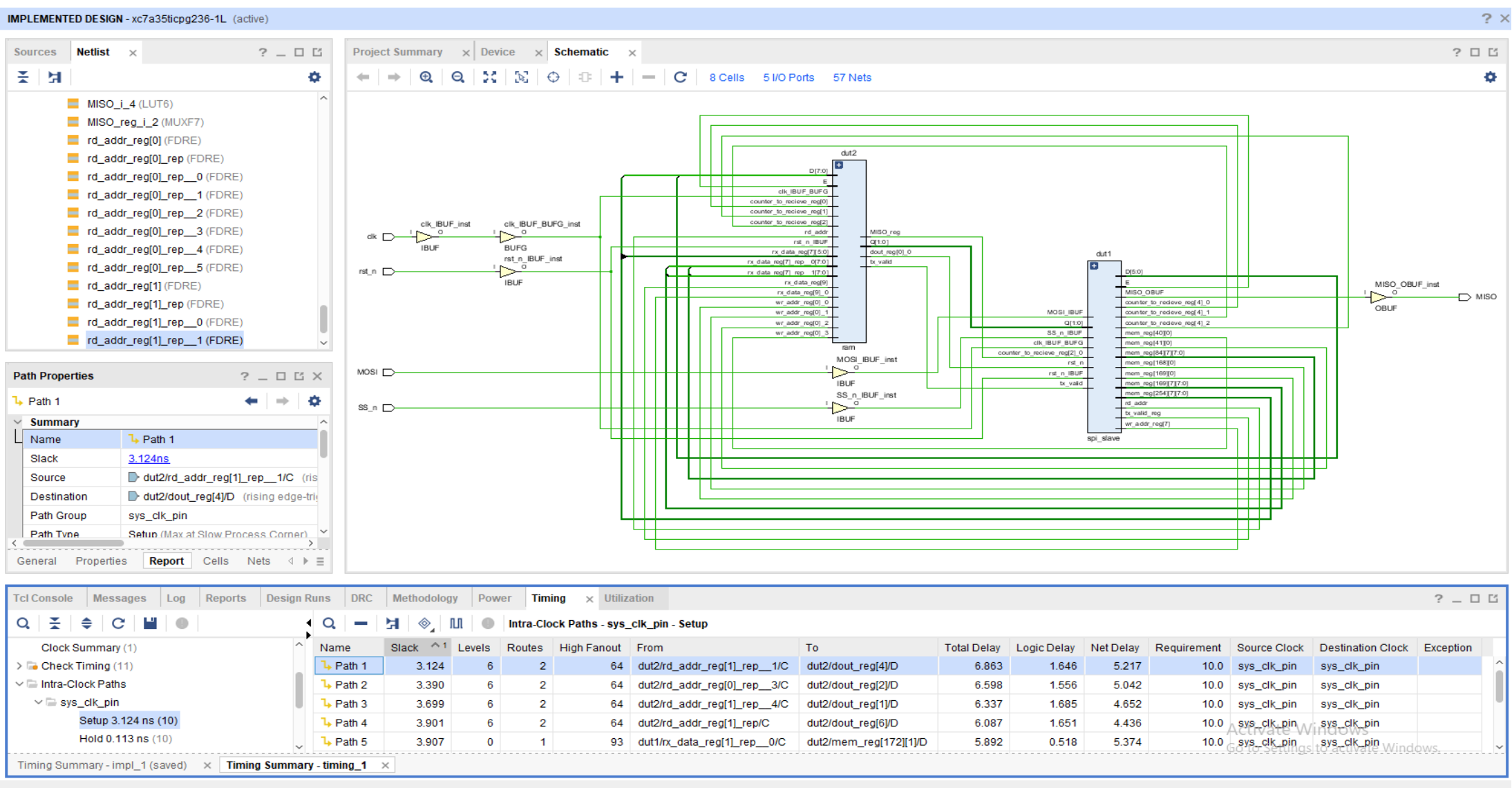
Intra-Clock Paths

sys_clk_pin

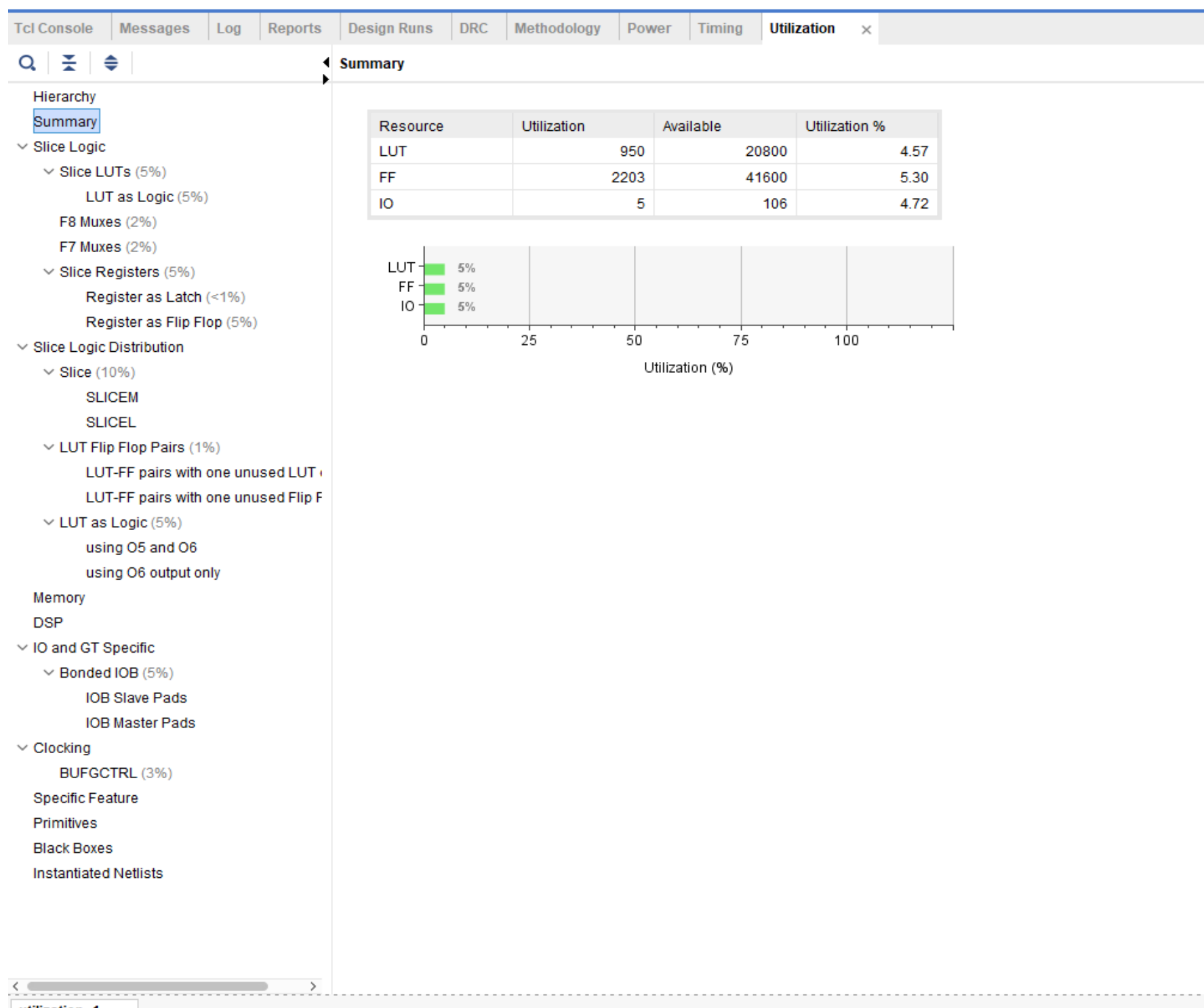
Setup 3.124 ns (10)

Activate Windows
Go to Settings to activate Windows.

Worst slack for sequential :



Utilization report :



Generate bit successful :

IMPLEMENDED DESIGN - xc7a35ticipg236-1L (active)

SourcesNetlist

MISO_I_4 (LUT6)

MISO_reg_i_2 (MUXF7)

rd_addr_reg[0] (FDRE)

rd_addr_reg[0]_rep (FDRE)

rd_addr_reg[0]_rep__0 (FDRE)

rd_addr_reg[0]_rep__1 (FDRE)

rd_addr_reg[0]_rep__2 (FDRE)

rd_addr_reg[0]_rep__3 (FDRE)

rd_addr_reg[0]_rep__4 (FDRE)

rd_addr_reg[0]_rep__5 (FDRE)

rd_addr_reg[1] (FDRE)

rd_addr_reg[1]_rep (FDRE)

rd_addr_reg[1]_rep__0 (FDRE)

rd_addr_reg[1]_rep__1 (FDRE)

Path Properties

Path 1

Summary

NamePath 1

Slack3.124ns

Sourcedut2/rd_addr_reg[1]_rep__1/C (ris

Destinationdut2/dout_reg[4]/D (rising edge-tri

Path Groupsys_clk_pin

Path TvneSetup (Max at Slow Process Corner)

Project SummaryDevice

Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

View Reports

Open Hardware Manager

Generate Memory Configuration File

Don't show this dialog again

OK

Cancel

Timing

Design Timing Summary

Clock Summary (1)

Check Timing (11)

Intra-Clock Paths

sys_clk_pin

Setup 3.124 ns (10)

Intra-Clock Paths - sys_clk_pin - Setup

Name	Slack	Levels	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception
Path 1	3.124	6	64	dut2/rd_addr_reg[1]_rep__1/C	dut2/dout_reg[4]/D	6.863	1.646	5.217	10.0	sys_clk_pin	sys_clk_pin	
Path 2	3.390	6	64	dut2/rd_addr_reg[0]_rep__3/C	dut2/dout_reg[2]/D	6.598	1.556	5.042	10.0	sys_clk_pin	sys_clk_pin	
Path 3	3.699	6	64	dut2/rd_addr_reg[1]_rep__4/C	dut2/dout_reg[1]/D	6.337	1.685	4.652	10.0	sys_clk_pin	sys_clk_pin	
Path 4	3.901	6	64	dut2/rd_addr_reg[1]_rep/C	dut2/dout_reg[6]/D	6.087	1.651	4.436	10.0	sys_clk_pin	sys_clk_pin	
Path 5	3.907	0	93	dut1/rx_data_reg[1]_rep__0/C	dut2/mem_reg[172][1]/D	5.892	0.518	5.374	10.0	sys_clk_pin	sys_clk_pin	

Activate Windows
Go to Settings to activate Windows.