

Team name: 32bit

Names:

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Abdelkader saad

Code :

```
1 module project_dsp (A , B , C , D , BCIN , CARRYIN , M , P , CARRYOUT , CARRYOUTF , CLK , OPMODE , CEA , CEB , CEC , CECARRYIN , CED , CEM , CEOPMODE , CEP , RSTA , RSTB , RSTC , RSTCARRYIN ,
2
3 parameter A0REG = 0;
4 parameter A1REG = 1;
5 parameter B0REG = 0;
6 parameter B1REG = 1;
7 parameter CREG = 1;
8 parameter DREG = 1;
9 parameter MREG = 1;
10 parameter PREG = 1;
11 parameter CARRYINREG =1;
12 parameter CARRYOUTREG =1;
13 parameter OPMODEREG =1;
14 parameter CARRYINSEL = "OPMODE5" ;
15 parameter B_INPUT = "DIRECT" ;
16 parameter RSTTYPE = "SYNC" ;
17
18 input [17:0] A , B , D , BCIN ;
19 input [47:0] C , PCIN ;
20 input CARRYIN , CLK , CEA , CEB , CEC ,CECARRYIN , CED , CEM , CEOPMODE , CEP , RSTA , RSTB , RSTC , RSTCARRYIN , RSTD , RSTM , RSTOPMODE , RSTP ;
21 output [35:0] M ;
22 output CARRYOUTF , CARRYOUT ;
23 input [7:0] OPMODE ;
24 output [17:0] BCOUT ;
25 output [47:0] PCOUT,P ;
26
27
28 wire [17:0] D_from_mux , B0_from_mux , A0_from_mux , Pre_Add_Sub , Pre_Add_Sub_from_mux , A1_from_mux, B1_from_mux ;
29 wire [47:0] C_from_mux , concatenated , post_Add_Sub , P_from_mux ;
30 wire[35:0] mult_out , mult_out_from_mux ;
31 reg [17:0] data_b;
32 wire CYI_from_mux , cout , CYO_from_mux;
33 reg carryin;
34 wire [7:0] OPMODE_from_mux;
35 reg [47:0] X_out , Z_out;
36
37 //op regs
38 ff_and_mux #(.ENable_ff(OPMODEREG) ,.SYN_OR_ASN(RSTTYPE) ,.WIDTH(8)) op (OPMODE ,CLK, CEOPMODE , RSTOPMODE , OPMODE_from_mux );
39
40
41 always @(*) begin
42 case (B_INPUT)
43 "DIRECT" : data_b = B ;
44 "CASCADE" : data_b = BCIN ;
45 default : data_b = 0;
46 endcase
47 end
48 //stg 1
49 ff_and_mux #(.FNable_ff(DREG) ,.SYN_OR_ASN(RSTTYPE) ,.WIDTH(18)) m1 (D ,CLK, CED , RSTD , D_from_mux );
```

```

46   endcase
47   end
48   //stg 1
49   ff_and_mux #(.ENable_ff(DREG),.SYN_OR_ASN(RSTTYPE),.WIDTH(18)) m1 (D ,CLK, CED , RSTD , D_from_mux );
50   ff_and_mux # (.ENable_ff(B0REG),.SYN_OR_ASN(RSTTYPE),.WIDTH(18)) m2 (data_b ,CLK, CEB , RSTB , B0_from_mux);
51   ff_and_mux # (.ENable_ff(A0REG),.SYN_OR_ASN(RSTTYPE),.WIDTH(18)) m3 (A ,CLK, CEA , RSTA , A0_from_mux);
52   ff_and_mux # (.ENable_ff(CREG),.SYN_OR_ASN(RSTTYPE),.WIDTH(48)) m4 (C ,CLK, CEC , RSTC ,C_from_mux);
53
54   //stg 2
55   add_sub #(.WIDTH_2(18),.FULLADDER("OFF")) pre (D_from_mux , B0_from_mux , Pre_Add_Sub , OPMODE_from_mux[6]);
56   assign Pre_Add_Sub_from_mux = (OPMODE_from_mux[4]) ? Pre_Add_Sub : B0_from_mux ;
57
58   //stg 3
59   ff_and_mux #(.ENable_ff(B1REG),.SYN_OR_ASN(RSTTYPE),.WIDTH(18)) m5 (Pre_Add_Sub_from_mux , CLK , CEB , RSTB ,B1_from_mux );
60   ff_and_mux # (.ENable_ff(A1REG),.SYN_OR_ASN(RSTTYPE),.WIDTH(18)) m6 (A0_from_mux ,CLK, CEA , RSTA , A1_from_mux);
61
62   //stg 4
63   assign mult_out = A1_from_mux * B1_from_mux;
64   //wires
65   assign concatenated = {D_from_mux[11:0] , A1_from_mux[17:0] , B1_from_mux[17:0]} ;
66   assign BCOUT = B1_from_mux ;
67
68   //stg 5
69   ff_and_mux #(.ENable_ff(MREG),.SYN_OR_ASN(RSTTYPE),.WIDTH(36)) m7 (mult_out , CLK , CEM , RSTM , mult_out_from_mux);
70   assign M = mult_out_from_mux ;
71   always @(*) begin
72       case (CARRYINSEL)
73           "CARRYIN" : carryin=CARRYIN;
74           "OPMODE5" : carryin=OPMODE_from_mux[5];
75           default : carryin=0;
76       endcase
77   endcase
78   end
79   ff_and_mux # (.ENable_ff(CARRYINREG),.SYN_OR_ASN(RSTTYPE),.WIDTH(1)) m8 (carryin , CLK , CECARRYIN , RSTCARRYIN , CYI_from_mux);
80
81   //stg 6
82
83   always @(*) begin
84       case (OPMODE_from_mux[1:0])
85           2'b00 : X_out = 0;
86           2'b01 : X_out = mult_out_from_mux ;
87           2'b10 : X_out = PCOUT ;
88           2'b11 : X_out = concatenated ;
89       endcase
90   endcase
91   end

```

```

83   always @(*) begin
84       case (OPMODE_from_mux[1:0])
85           2'b00 : X_out = 0;
86           2'b01 : X_out = mult_out_from_mux ;
87           2'b10 : X_out = PCOUT ;
88           2'b11 : X_out = concatenated ;
89       endcase
90   endcase
91   end
92   always @(*) begin
93       case (OPMODE_from_mux[3:2])
94           2'b00 : Z_out = 0;
95           2'b01 : Z_out = PCIN ;
96           2'b10 : Z_out = PCOUT ;
97           2'b11 : Z_out = C_from_mux ;
98       endcase
99   endcase
100  end
101
102
103  //stg 7
104  add_sub #(.WIDTH_2(48),.FULLADDER("ON")) post (Z_out,X_out,post_Add_Sub,OPMODE_from_mux[7], CYI_from_mux , cout );
105  ff_and_mux #(.ENable_ff(CARRYOUTREG),.SYN_OR_ASN(RSTTYPE),.WIDTH(1)) m9 (cout , CLK, CECARRYIN , RSTCARRYIN , CYO_from_mux );
106  assign CARRYOUT = CYO_from_mux ;
107  assign CARRYOUTF = CYO_from_mux ;
108  //stg 8
109  ff_and_mux #(.ENable_ff(PREG),.SYN_OR_ASN(RSTTYPE),.WIDTH(48)) m10 (post_Add_Sub , CLK, CEP , RSTP , P_from_mux );
110  assign PCOUT = P_from_mux;
111  assign P = P_from_mux;
112
113  endmodule
114
115
116

```

Ffandmux:

```
1 module ff_and_mux (inp , clk, clk_enable , rst , out );
2
3     parameter ENable_ff = 1;
4     parameter SYN_OR_ASN = "SYNC" ;
5     parameter WIDTH = 18 ;
6
7
8     input [WIDTH -1 : 0] inp ;
9     input clk ,clk_enable, rst ;
10    output [WIDTH -1 : 0] out ;
11    reg [WIDTH-1 : 0] out_ff;
12
13    generate
14        if (SYN_OR_ASN == "SYNC")begin
15            always @(posedge clk ) begin
16                if (rst) begin
17                    out_ff <= 0;
18                end
19                else if (clk_enable) begin
20                    out_ff <= inp;
21                end
22            end
23        end
24        else if (SYN_OR_ASN == "ASYN")begin
25            always @(posedge clk or posedge rst) begin
26                if (rst) begin
27                    out_ff <= 0;
28                end
29                else if (clk_enable) begin
30                    out_ff <= inp ;
31                end
32            end
33        end
34    end
35
36    endgenerate
37
38    assign out = (ENable_ff == 1)? out_ff : inp ;
39    endmodule
40
41
```

Adder and subtractor:

```
1 module add_sub (in1,in2,out,OPMODE,cin,cout);
2     parameter FULLADDER="ON";
3     parameter WIDTH_2=18;
4     input OPMODE,cin;
5     input [WIDTH_2-1:0] in1,in2;
6     output reg [WIDTH_2-1:0] out;
7     output reg cout ;
8     generate
9         if (FULLADDER=="ON") begin
10             always@(*) begin
11
12                 if(OPMODE)
13                     {cout,out}=in1-(in2+cin);
14                 else
15                     {cout,out}=in1+in2+cin;
16
17             end
18         end
19
20         else if (FULLADDER=="OFF") begin
21             always@(*) begin
22
23                 if(OPMODE)
24                     out=in1-in2;
25                 else
26                     out=in1+in2;
27
28             end
29         end
30     endgenerate
31    endmodule
32
```

Verify :

```
1 module project_dsp_tb ();
2 parameter A0REG = 0;
3 parameter A1REG = 1;
4 parameter B0REG = 0;
5 parameter B1REG = 1;
6 parameter CREG = 1;
7 parameter DREG = 1;
8 parameter MREG = 1;
9 parameter PREG = 1;
10 parameter CARRYINREG =1;
11 parameter CARRYOUTREG =1;
12 parameter OPMODEREG =1;
13 parameter CARRYINSEL = "OPMODE5" ;
14 parameter B_INPUT = "DIRECT" ;
15 parameter RSTTYPE = "SYNC" ;
16
17 reg [17:0] A , B , D , BCIN ;
18 reg [47:0] C , PCIN ;
19 reg CARRYIN , CLK , CEA , CEB , CEC ,CECARRYIN , CED , CEM , CEOPMODE , CEP , RSTA , RSTB , RSTC , RSTCARRYIN , RSTD , RSTM , RSTOPMODE , RSTP ;
20 reg [7:0] OPMODE ;
21
22 wire [35:0] M ;
23 wire CARRYOUTF , CARRYOUT ;
24 wire [17:0] BCOUT ;
25 wire [47:0] PCOUT,P ;
26
27 project_dsp dut (A , B , C , D , BCIN , CARRYIN , M , P , CARRYOUT , CARRYOUTF , CLK , OPMODE , CEA , CEB , CEC , CECARRYIN , CED , CEM , CEOPMODE , CEP , RSTA , RSTB , RSTC , RSTCARRYIN , RSTD , RSTM , RSTOPMODE , RSTP );
28
29
30 initial begin
31
32     CLK=0;
33     forever
34         #1 CLK=~CLK;
35
36 end
37
38
39
40 initial begin
41
42     RSTA =1;
43     RSTB =1;
44     RSTC =1;
45     RSTCARRYIN =1;
46     RSTD =1;
47     RSTM =1;
48     RSTOPMODE =1;
49     RSTP =1;
```

```
42     RSTA =1;
43     RSTB =1;
44     RSTC =1;
45     RSTCARRYIN =1;
46     RSTD =1;
47     RSTM =1;
48     RSTOPMODE =1;
49     RSTP =1;
50     A=0;
51     B=0 ;
52     C=0 ;
53     D =0;
54     BCIN =0;
55     CARRYIN =0;
56     OPMODE =8'b1011_1101;
57     CEA =1;
58     CEB =1;
59     CEC =1;
60     CECARRYIN =1;
61     CED =1;
62     CEM =1;
63     CEOPMODE=1;
64     CEP=1;
65     PCIN =0;
66     #50;
67     RSTA =0;
68     RSTB =0;
69     RSTC =0;
70     RSTCARRYIN =0;
71     RSTD =0;
72     RSTM =0;
73     RSTOPMODE =0;
74     RSTP =0;
75     A=18'd4;
76     B=18'd10 ;
77     C=48'd150 ;
78     D =18'd15;
79     BCIN =0;
80     CARRYIN =0;
81     OPMODE =8'b1001_1101;
82     CEA =1;
83     CEB =1;
84     CEC =1;
85     CECARRYIN =1;
86     CED =1;
87     CEM =1;
88     CFOPMODF=1;
```

```

84     CEC = 1;
85     CECARRYIN = 1;
86     CED = 1;
87     CEM = 1;
88     CEOPMODE=1;
89     CEP=1;
90     PCIN = 0;
91     #50;
92     OPMODE=8'b0101_1010;
93     #50;
94     A=0;
95     D=0;
96     OPMODE=8'b0010_0011;
97
98     #20 $stop;
99
100
101
102
103
104
105
106
107
108     end
109     endmodule

```

Do file :

```

1  vlib work
2
3  vlog add_sub.v ffandmux.v project_1.v project_tb.v
4
5  vsim -voptargs=+acc work.project_dsp_tb
6  add wave *
7
8  run -all

```

Tcl file :

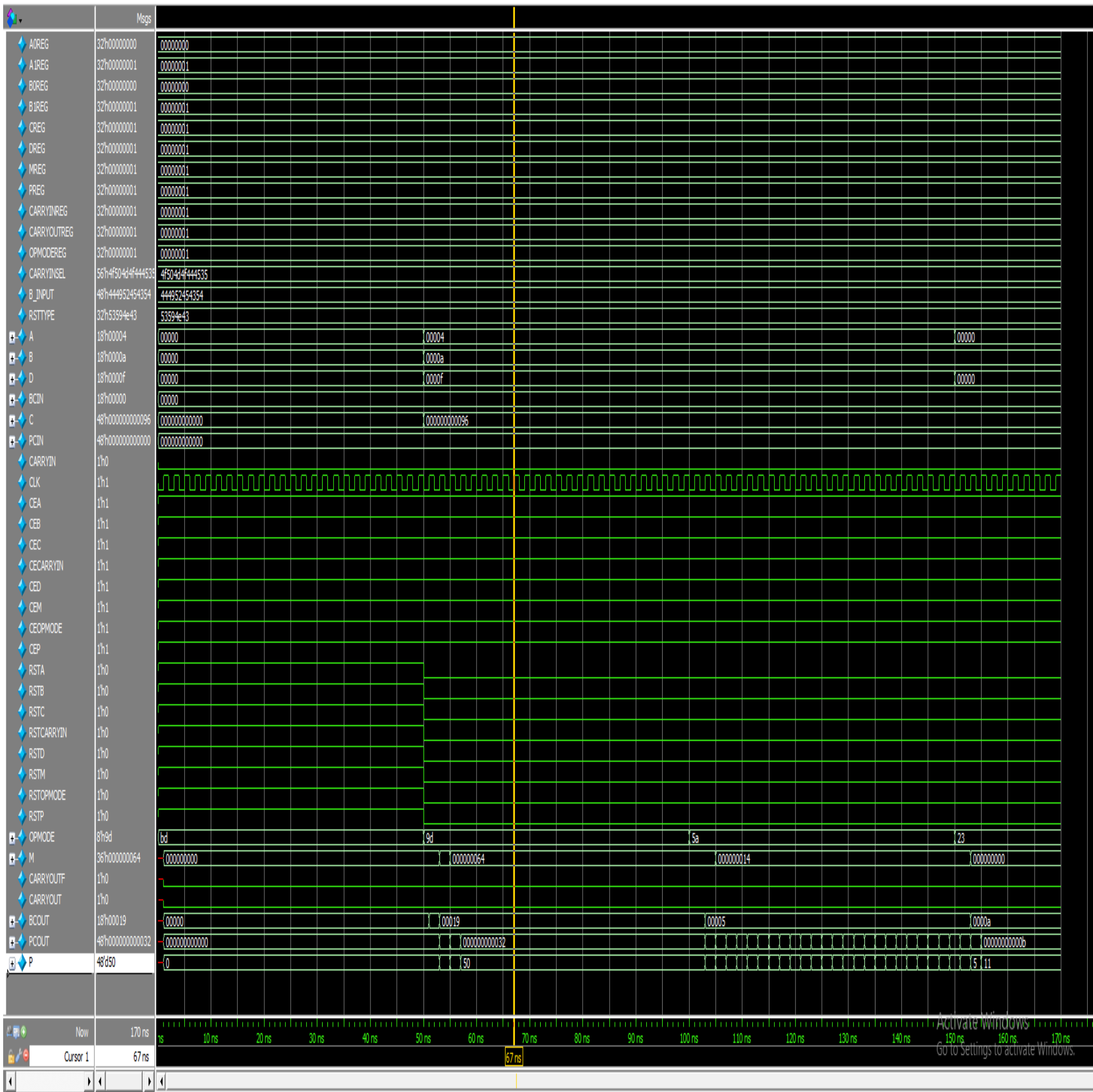
```

1  create_project project_DSP D:/kwtraining/final_project_1/code -part xc7a200tffg1156-1 -force
2
3  add_files project_1.v add_sub.v ffandmux.v
4
5  synth_design -rtl -top project_dsp > elab.log
6  # report_timing_summary -delay_type min_max -report_unconstrained -check_timing_verbose -max_paths 10 -input_pins -routable_nets -name timing_1>timing rpt
7
8  write_schematic elaborated_schematic.pdf -format pdf -force
9
10 launch_runs synth_1 > synth.log
11
12 wait_on_run synth_1
13 open_run synth_1
14
15 write_schematic synthesized_schematic.pdf -format pdf -force
16
17 write_verilog -force DSP_netlist.v
18
19 launch_runs impl_1 > impl.log
20
21 wait_on_run impl_1
22 open_run impl_1
23
24 open_hw
25
26 connect_hw_server

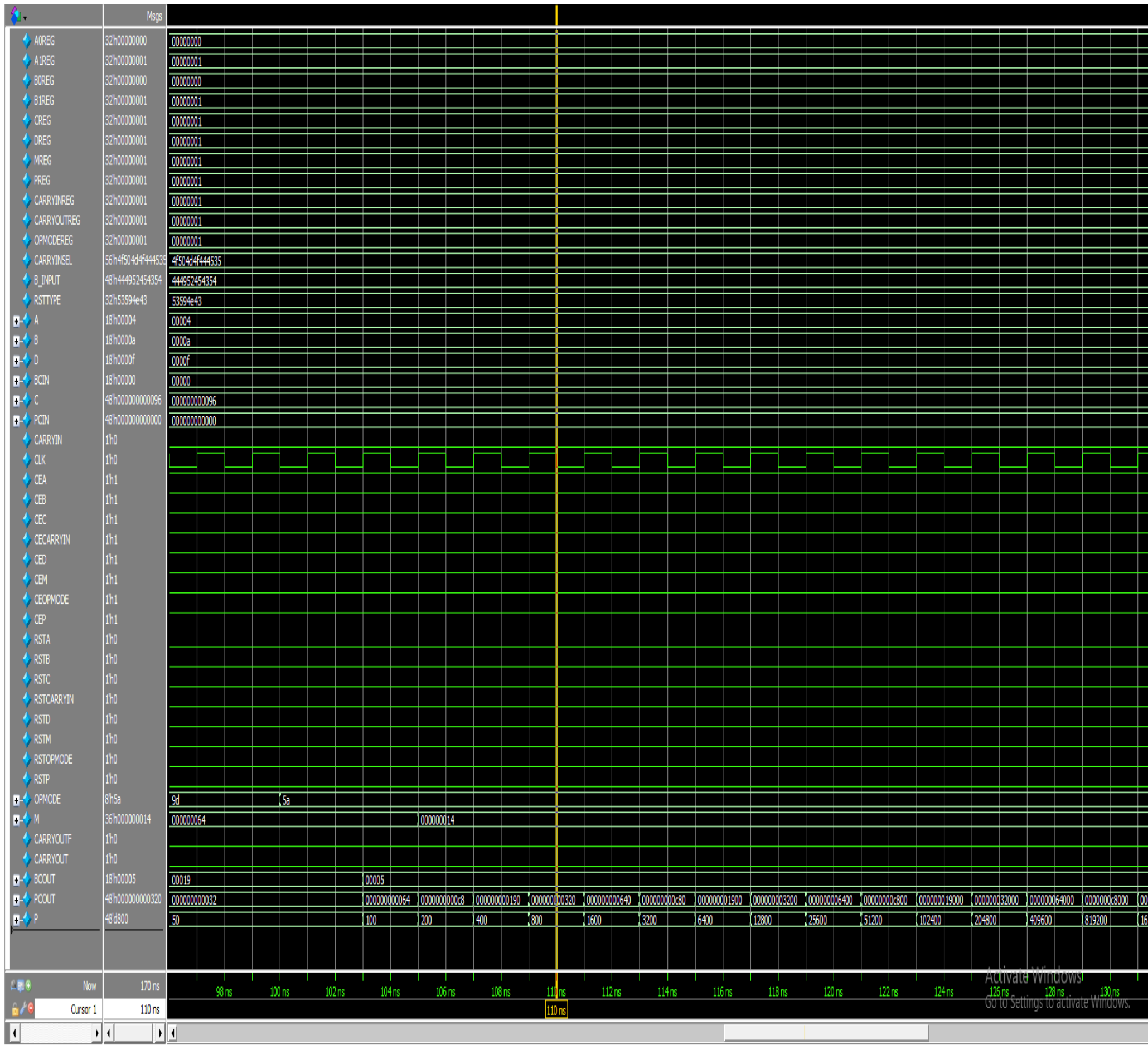
```

Questasim:

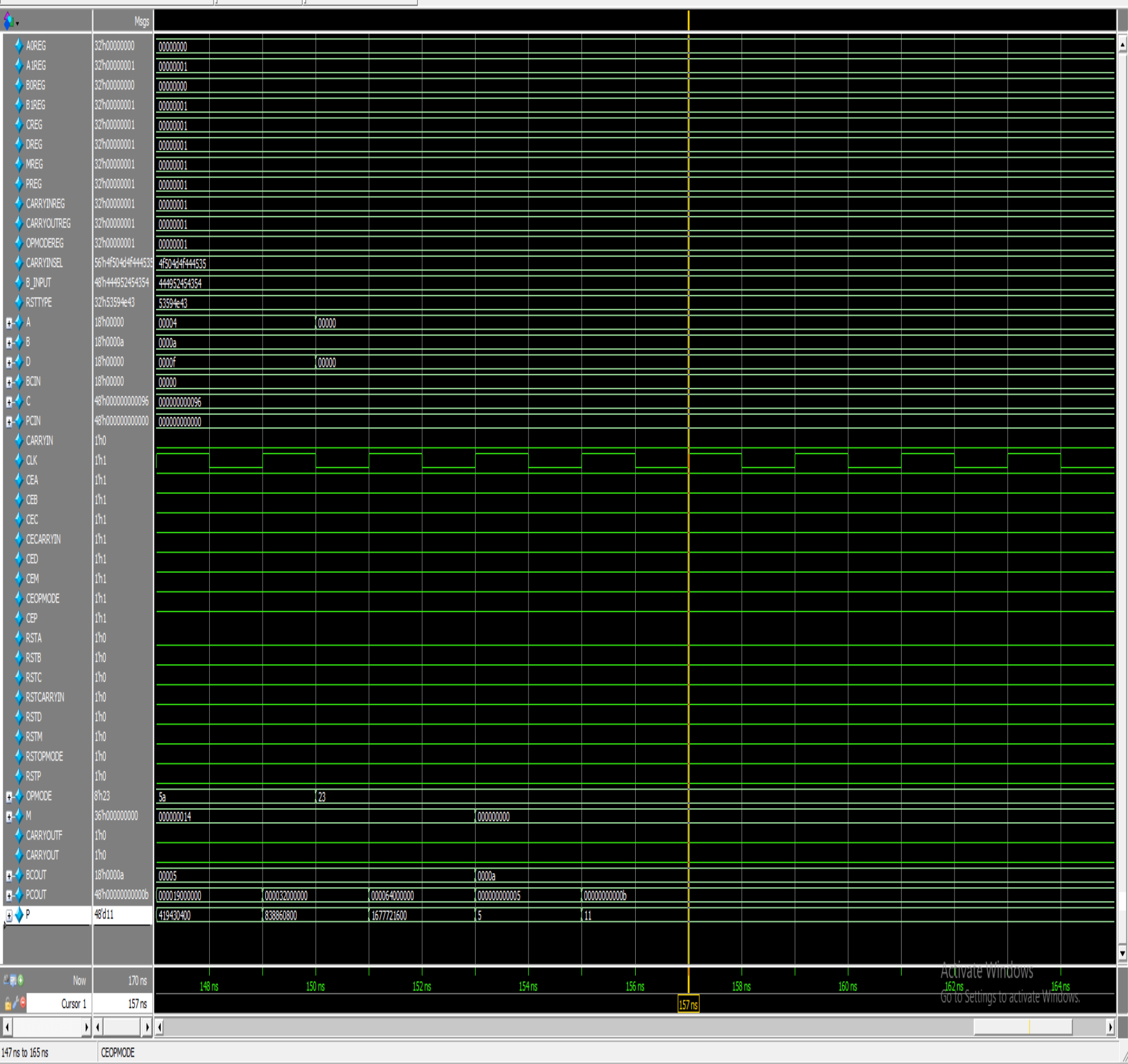
snippet for test and (P) RESULT WILL EQUAL 50 due to values that i put to inputs
as you see:



by zoom in as you see i test the accumulation p in both mux X and Z so number will be double:

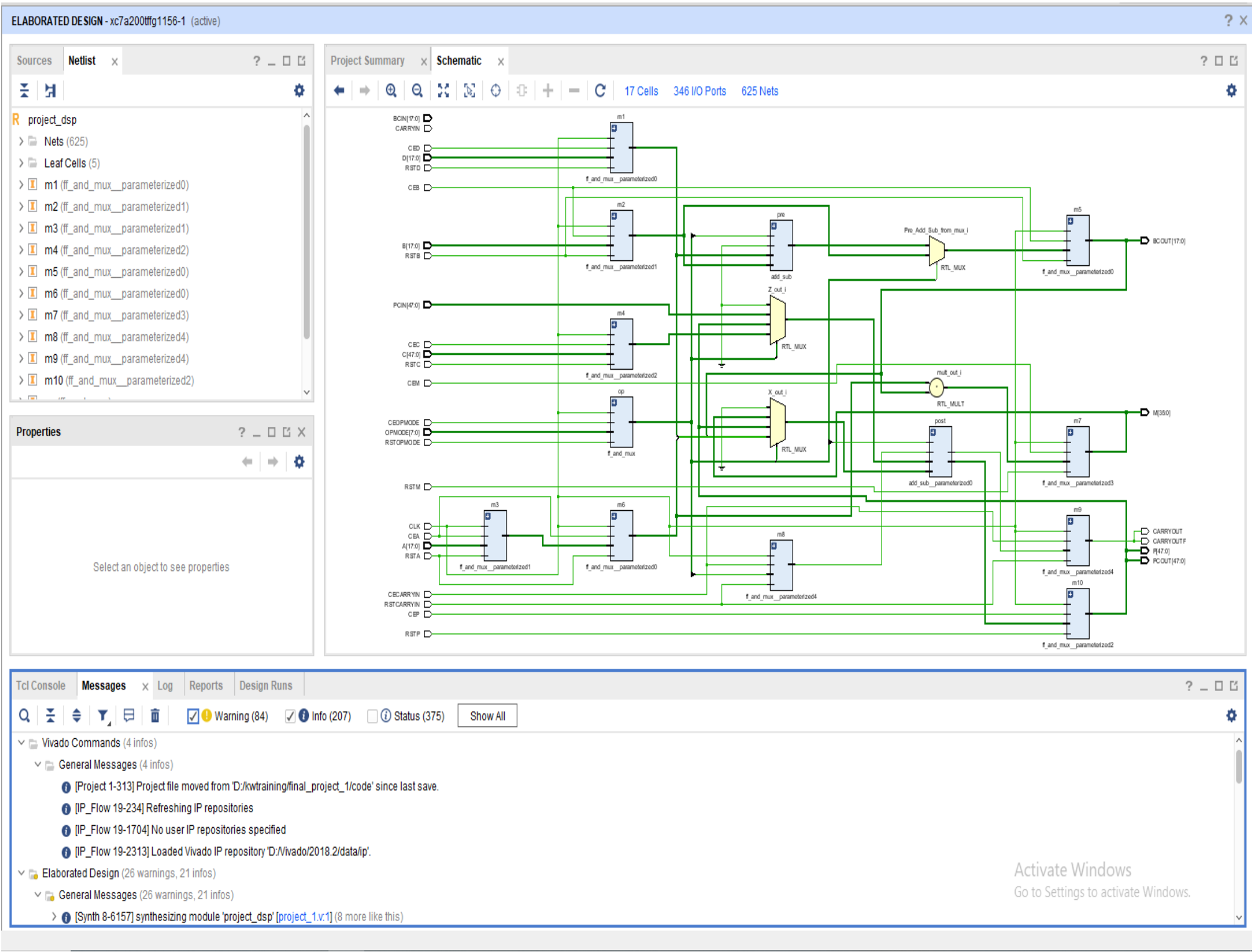


here i test concatenated and carry in =1 by opmode so result equal to 11:

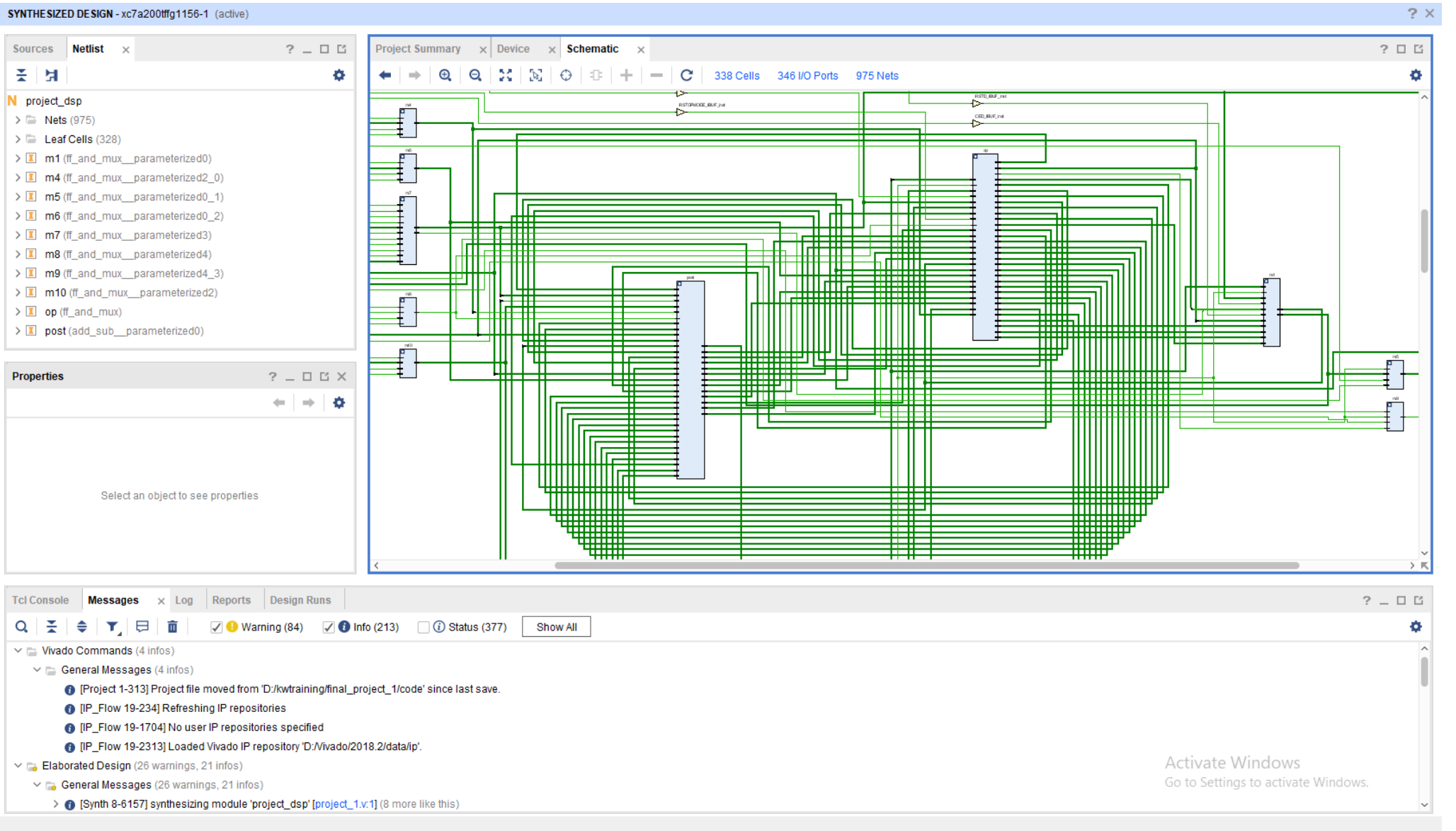


Vivado :

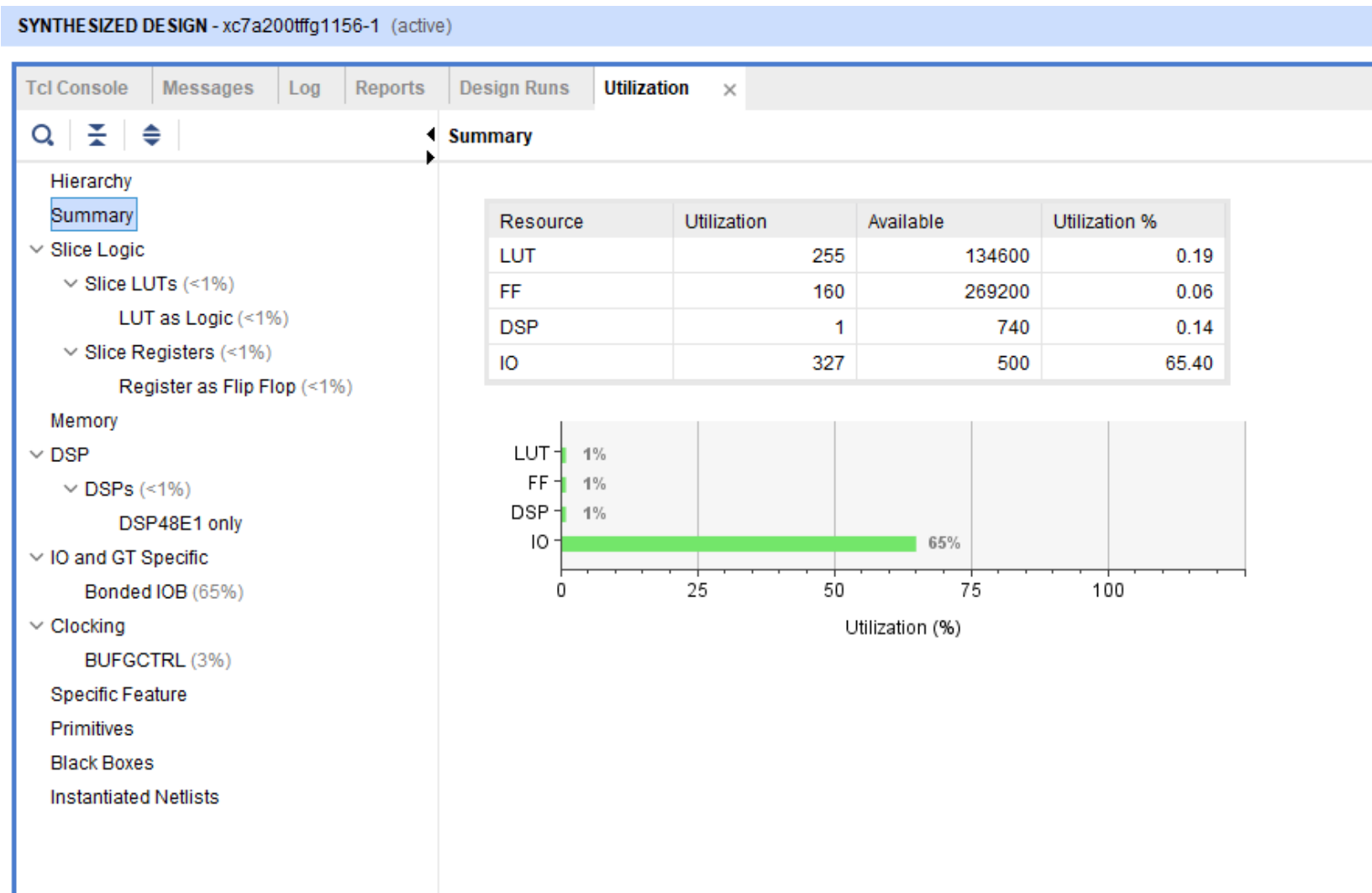
Schematic after elaborated without error :



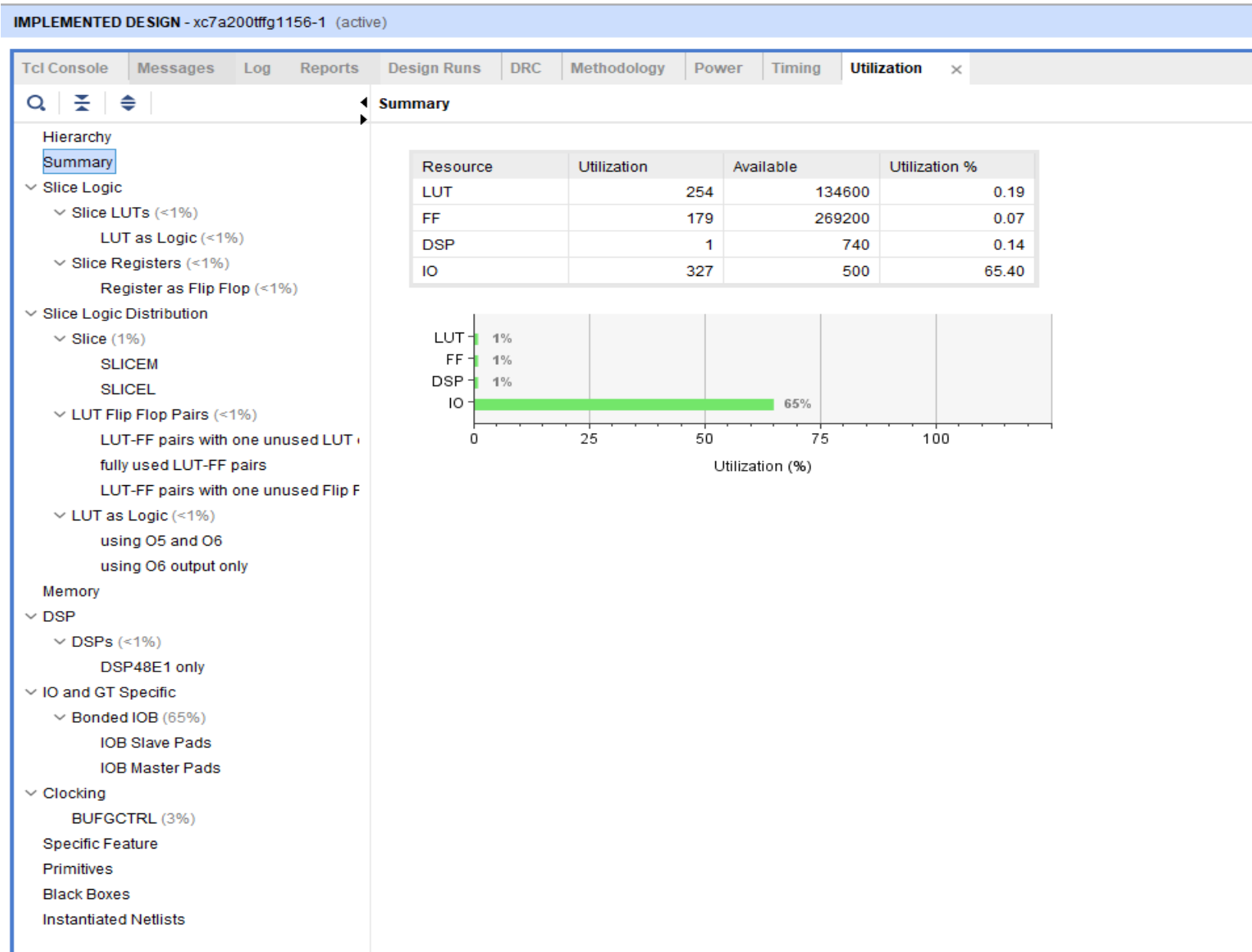
schematic after synthsis with no error :



utilization after synthesis :



utullization after implementation:



implemantaion with no errors and its schematic :

IMPLEMENTS DESIGN - xc7a200tffg1156-1 (active)

SourcesNetlist x ? _ □ □ ?

project_dsp

> Nets (994)

> Leaf Cells (328)

> m1 (ff_and_mux_parameterized0)

> m4 (ff_and_mux_parameterized2_0)

> m5 (ff_and_mux_parameterized0_1)

> m6 (ff_and_mux_parameterized0_2)

> m7 (ff_and_mux_parameterized3)

> m8 (ff_and_mux_parameterized4)

> m9 (ff_and_mux_parameterized4_3)

> m10 (ff_and_mux_parameterized2)

> op (ff_and_mux)

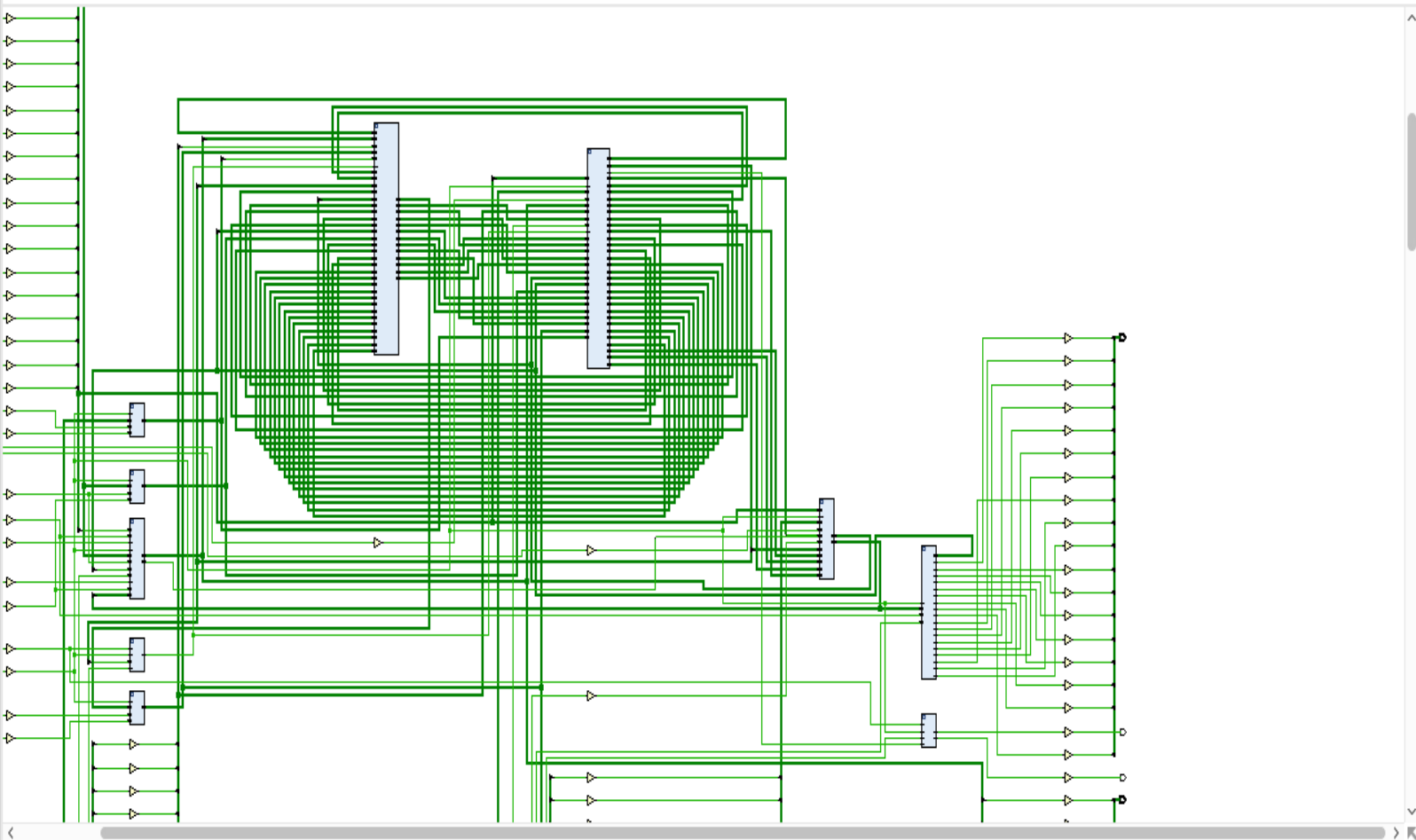
> post (add_sub__parameterized0)

Properties ? _ □ □ □ x

Select an object to see properties

Project Summary x Device x Schematic x ? _ □ □ ?

338 Cells 346 I/O Ports 994 Nets



Tcl Console Messages x Log Reports Design Runs DRC Methodology Power Timing ? _ □ □ ?

Warning (85) Info (218) Status (382) Show All

Vivado Commands (4 infos)

General Messages (4 infos)

[Project 1-313] Project file moved from 'D:/kwtraining/final_project_1/code' since last save.

[IP_Flow 19-234] Refreshing IP repositories

[IP_Flow 19-1704] No user IP repositories specified

[IP_Flow 19-2313] Loaded Vivado IP repository 'D:/vivado/2018.2/data/ip'.

Elaborated Design (26 warnings, 21 infos)

General Messages (26 warnings, 21 infos)

[Synth 8-6157] synthesizing module 'project_dsp' [project_1.v:1] (8 more like this)

Activate Windows
Go to Settings to activate Windows.

Device :

IMPLEMENTS DESIGN - xc7a200tffg1156-1 (active)

SourcesNetlist x ? _ □ □ ?

project_dsp

> Nets (994)

> Leaf Cells (328)

> m1 (ff_and_mux_parameterized0)

> m4 (ff_and_mux_parameterized2_0)

> m5 (ff_and_mux_parameterized0_1)

> m6 (ff_and_mux_parameterized0_2)

> m7 (ff_and_mux_parameterized3)

> m8 (ff_and_mux_parameterized4)

> m9 (ff_and_mux_parameterized4_3)

> m10 (ff_and_mux_parameterized2)

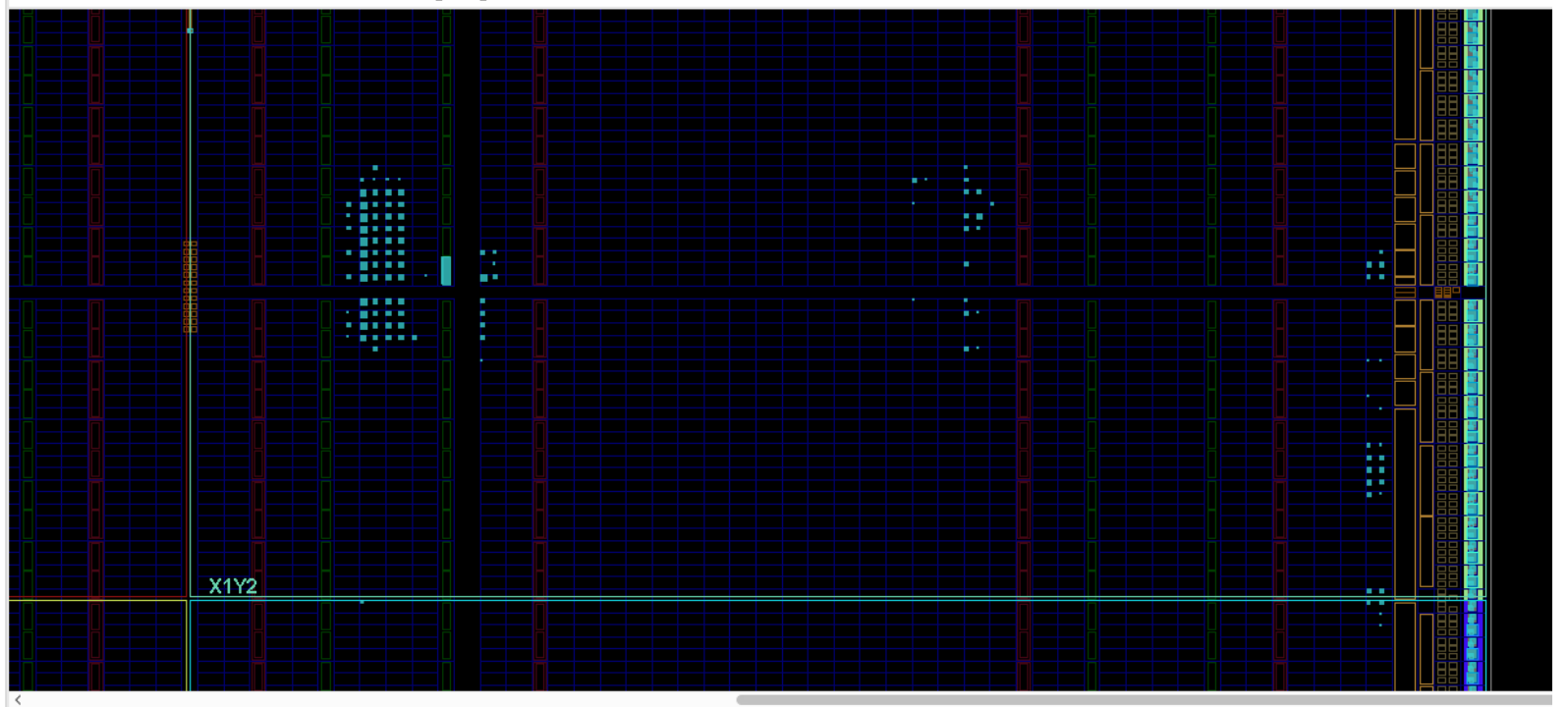
> op (ff_and_mux)

> post (add_sub__parameterized0)

Properties ? _ □ □ □ x

Select an object to see properties

Project Summary x Device x Schematic x ? _ □ □ ?



Tcl Console Messages x Log Reports Design Runs DRC Methodology Power Timing ? _ □ □ ?

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Activate Windows
Go to Settings to activate Windows.