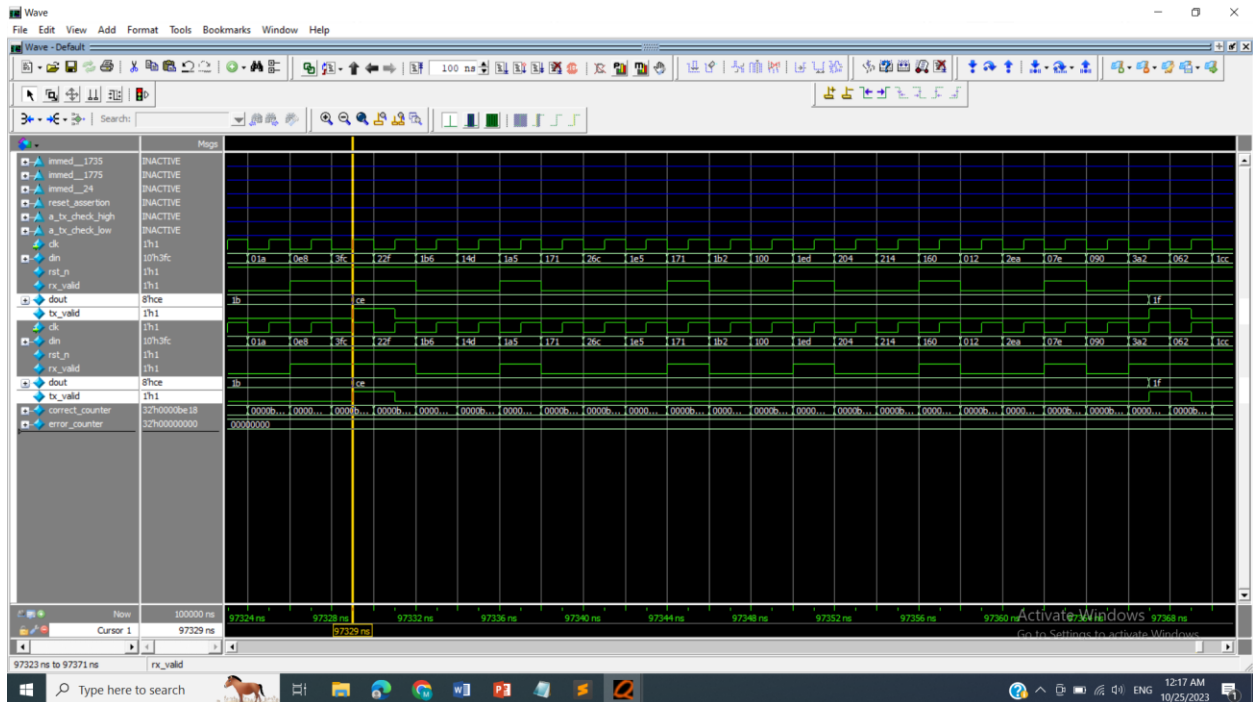


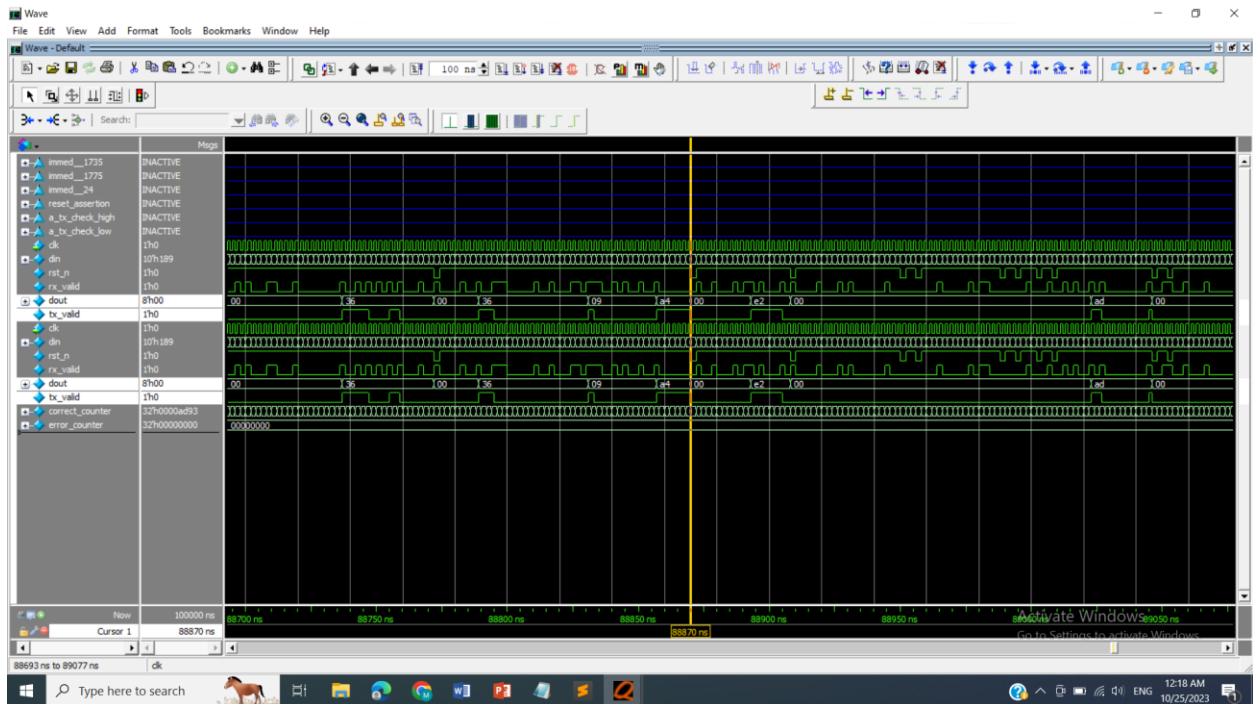
Part 1:

RAM:

Successful operation(hint the upper dout is the golden one):

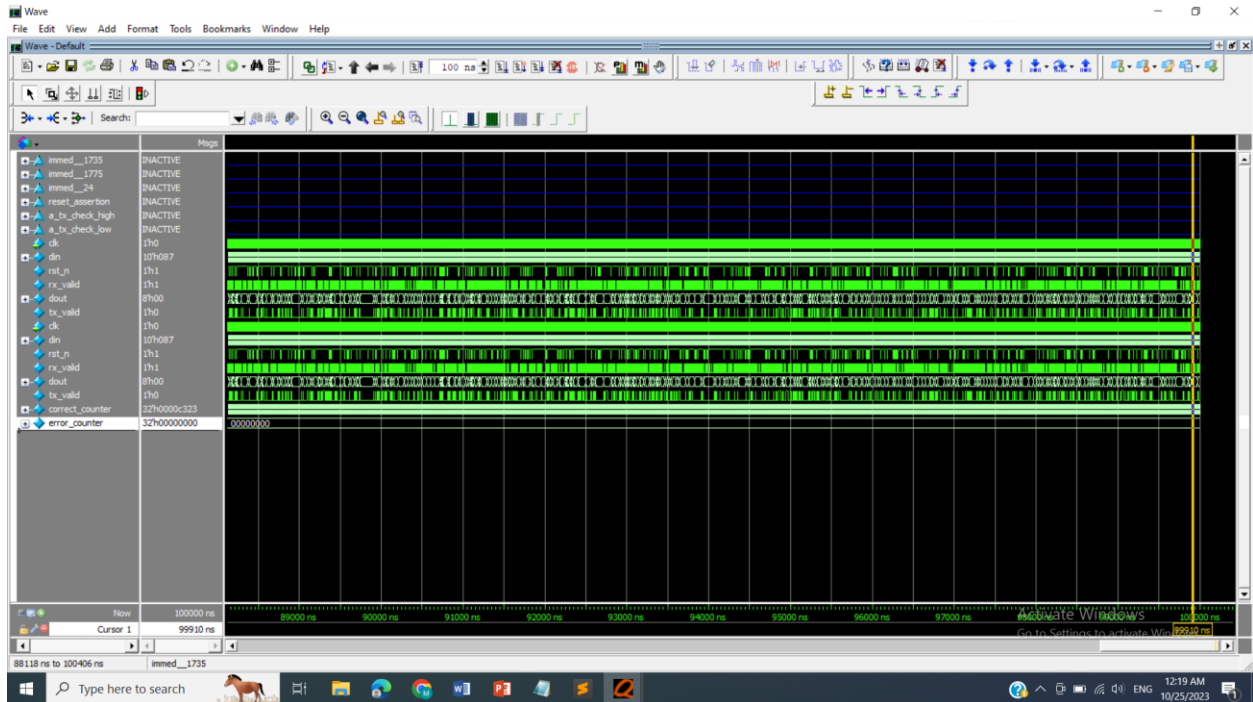


When rst is asserted:



Whole WF:

As you can see error is zero and assertions has no error:



Functional coverage:

The screenshot displays the Questasim-64 2021.1 software interface. The main window is divided into several panes. On the left, the 'Instance' pane shows a hierarchical tree of simulation components, including 'uvm_root', 'uvm_test_top', 'Top_module', 'RAM_intf', 'RAM_golden_intf', 'DUT', 'Golden_ref', '#INITIAL#', and '#INITIAL#22'. The 'Coverage Details' pane in the center is currently empty. On the right, the 'Covergroups' pane displays a table of coverage results for various covergroups.

Name	Class Type	Coverage	Goal	% of Goal	Status	Ind
RAM_coverage_p...		100.00%	100	100.00...		
TXFE_cov_grp...		100.00%	100	100.00...		
CVP_cov_grp...		100.00%	100	100.00...		
CVP_cov_grp...		100.00%	100	100.00...		
CROSS_cov...		100.00%	100	100.00...		

At the bottom of the interface, there is a taskbar with various application icons and a system tray showing the time as 12:19 AM on 10/25/2023. A watermark 'Activate Windows' is visible in the bottom right corner of the application window.

Code coverage:

```
C:\Users\HP\Downloads\RAM_UVM\ram_coverage.rpt.txt - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help

ram_coverage.rpt.txt
166 =====
167 === Instance: /Top_module/DUT
168 === Design Unit: work.spi_ram
169 =====
170 Branch Coverage:
171 Enabled Coverage      Bins      Hits      Misses  Coverage
172 -----
173 Branches              8        7        1      87.50%
174
175 =====Branch Details=====
176
177 Branch Coverage for instance /Top_module/DUT
178
179 Line      Item      Count      Source
180 ----      -
181 File project_ram.v
182 -----IF Branch-----
183 17          1      52313      Count coming in to IF
184 17          1      4792       if(rst_n==0) begin
185
186 24          1      14224      else if(rx_valid==1) begin
187
188          33297      All False Count
189 Branch totals: 3 hits of 3 branches = 100.00%
190
191 -----IF Branch-----
192 25          1      14224      Count coming in to IF
193 25          1      3640       if(din[9:8]==2'b00) begin
194
195 29          1      3563      else if(din[9:8]==2'b01) begin
196
197 33          1      3540      else if(din[9:8]==2'b10) begin
198
199 37          1      3481      else if(din[9:8]==2'b11) begin
200
201          ***0***      All False Count
```

Activate Windows
Go to Settings to activate Windows...

Line 1, Column 1 Spaces: 4 Plain Text

Type here to search 12:24 AM 10/25/2023

```
C:\Users\HP\Downloads\RAM_UVM\ram_coverage.rpt.txt - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help

ram_coverage.rpt.txt
267
268 Statement Coverage:
269   Enabled Coverage      Bins   Hits   Misses Coverage
270   -----
271   Statements            13     13     0    100.00%
272
273 =====Statement Details=====
274
275 Statement Coverage for instance /Top_module/DUT --
276
277   Line      Item      Count   Source
278   ----      -
279   File project_ram.v
280   1
281       module spi_ram(din,rx_valid,tx_valid,dout,clk,rst_n);
282   2
283       parameter MEM_DEPTH = 256,ADDR_SIZE=8;
284   3
285
286   4
287       input [9:0] din;
288   5
289       input rx_valid;
290   6
291       input clk,rst_n;
292   7
293       output reg tx_valid;
294   8
295       output reg[7:0] dout;
296   9
297   10
298   11
299   12
300
301       reg [ADDR_SIZE-1:0] WRITE_ADD,READ_ADD;
302
```

```
C:\Users\HP\Downloads\RAM_UVM\ram_coverage.rpt.txt - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help

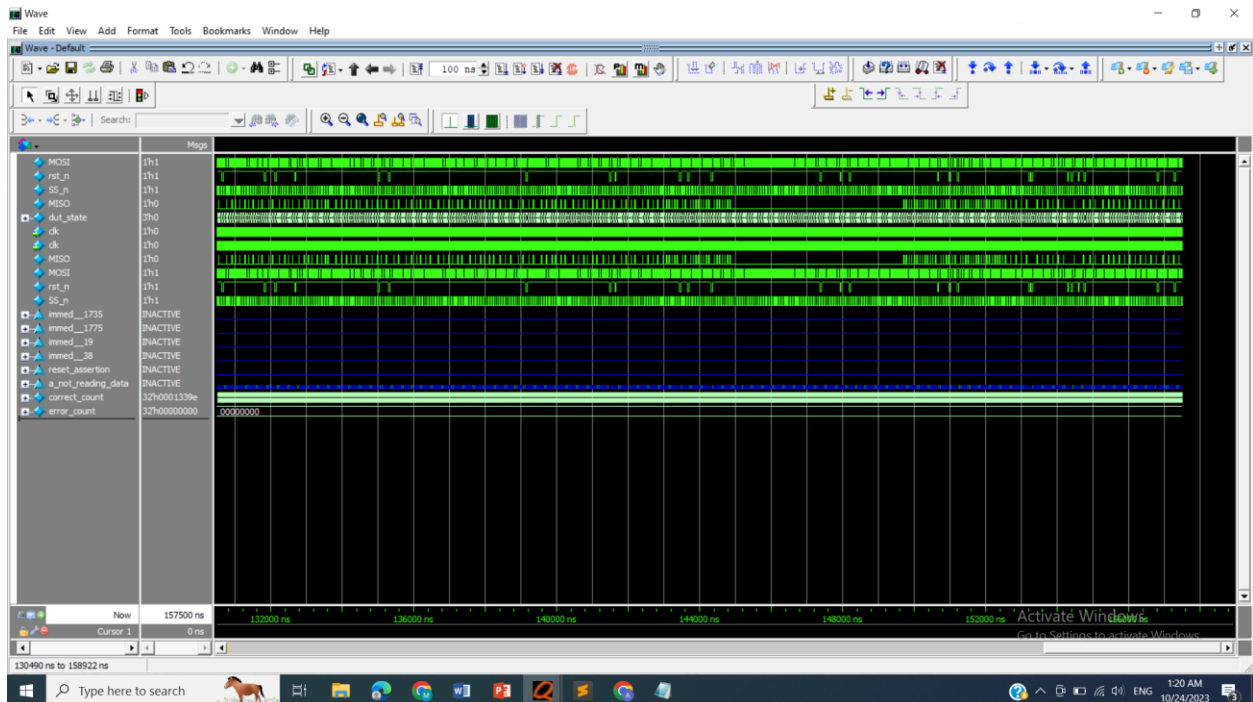
ram_coverage.rpt.txt
357
358
359 Toggle Coverage:
360   Enabled Coverage      Bins   Hits   Misses Coverage
361   -----
362   Toggles               78     76     2    97.43%
363
364 =====Toggle Details=====
365
366 Toggle Coverage for instance /Top_module/DUT --
367
368   Node      1H->0L   0L->1H   "Coverage"
369   ----
370   RAM_intf0      0         0         0.00
371   READ_ADD[7-0]  1         1        100.00
372   WRITE_ADD[7-0] 1         1        100.00
373   clk            1         1        100.00
374   din[0-9]       1         1        100.00
375   dout[7-0]      1         1        100.00
376   rst_n          1         1        100.00
377   rx_valid       1         1        100.00
378   tx_valid       1         1        100.00
379
380 Total Node Count = 39
381 Toggled Node Count = 38
382 Untoggled Node Count = 1
383
384 Toggle Coverage = 97.43% (76 of 78 bins)
385
386 =====
387 === Instance: /Top_module/Golden_ref
388 === Design Unit: work.RAM_golden
389 =====
390 Branch Coverage:
391   Enabled Coverage      Bins   Hits   Misses Coverage
392   -----
```

Part 2:

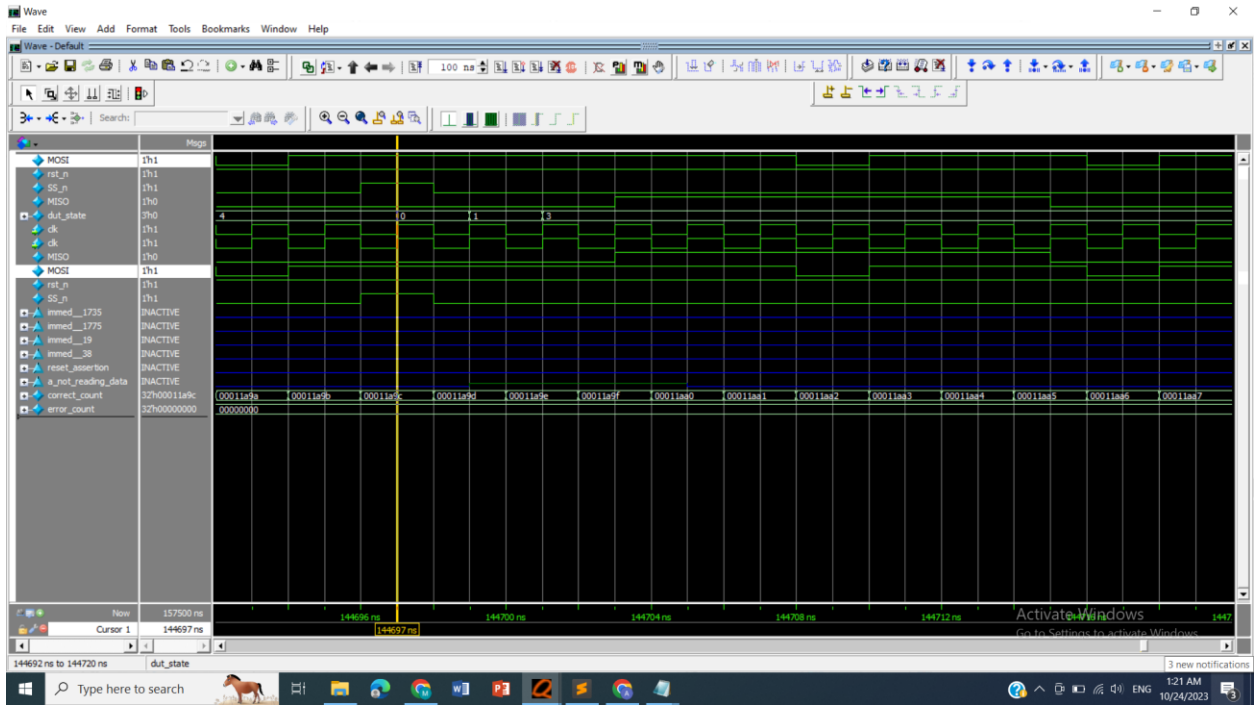
SPI:

Full Wv:

Error is zero and all assertions are fine



Zoom:



Functional coverage:

Questa Sim-64 2021.1

File Edit View Compile Simulate Add Covergroups Tools Layout Bookmarks Window Help

ColumnLayout [Default] 100 ns 100 Threshold 100

sim (Recursive Coverage Aggregation) - Default

Instance

- uvm_root
- uvm_test_top
- top
- spi_intf
- spi_golden_intf
- DUT
- golden
- #INITIAL#7
- #INITIAL#21
- uvm_pkg
- seq_item
- seq
- scoreboard
- myconfig
- driver
- monitor
- sequencer
- agent
- coverage
- env
- spi_test1
- top_pi_unit
- questa_uvm_pkg
- std
- #vsm_capacity#

Coverage Details

Covergroups

Name	Class Type	Coverage	Goal	% of Goal	Status	Inc
/coverage/spi_cov...		100.00%	100	100.00%		
TYPE cvr_grp...		100.00%	100	100.00%		
CVP cvr_grp...		100.00%	100	100.00%		
CVP cvr_grp...		100.00%	100	100.00%		
bin auto...		130	1	100.00%		
bin auto...		6201	1	100.00%		
CROSS cvr...		100.00%	100	100.00%		
bin writ...		11	1	100.00%		
bin read...		2	1	100.00%		
bin writ...		6	1	100.00%		
bin read...		2	1	100.00%		
ignore...		0	-	-		

Project: abdo Now: 157,500 ns Delta: 61 sim/top/#INITIAL#21

Covergroups Filter: NoFilter Covergroups Coverage: 100.00% Recursive Mode

C:\Users\HP\Downloads\SPI UVM\UVM\cover_report.txt - Sublime Text (UNREGISTERED)

File Edit Selection Find View Goto Tools Project Preferences Help

coverage_rpt.txt fcover_report.txt project_spiv

```
1 Coverage Report by instance with details
2
3 =====
4 === Instance: /coverage
5 === Design Unit: work.coverage
6 =====
7
8 Covergroup Coverage:
9   Covergroups      1      na      na  100.00%
10  Coverpoints/Crosses 3      na      na
11  Covergroup Bins   10     10     0  100.00%
12
13 -----
14
15 Covergroup                      Metric      Goal      Bins      Status
16 -----
17 TYPE /coverage/spi_coverage/cvr_grp_spi      100.00%      100      -      Covered
18 covered/total bins:      10      10      -
19 missing/total bins:      0      10      -
20 % Hit:      100.00%      100
21 Coverpoint c_din      100.00%      100      -      Covered
22 covered/total bins:      4      4      -
23 missing/total bins:      0      4      -
24 % Hit:      100.00%      100
25 ignore_bin not_address[1]      7      -      Occurred
26 ignore_bin not_address[2]      7      -      Occurred
27 ignore_bin not_address[3]      8      -      Occurred
28 ignore_bin not_address[4]      4      -      Occurred
29 ignore_bin not_address[5]      6      -      Occurred
30 ignore_bin not_address[6]      4      -      Occurred
31 ignore_bin not_address[7]      4      -      Occurred
32 ignore_bin not_address[8]      5      -      Occurred
33 ignore_bin not_address[9]      9      -      Occurred
34 ignore_bin not_address[10]      8      -      Occurred
35 ignore_bin not_address[11]      5      -      Occurred
36 ignore_bin not_address[12]      7      -      Occurred
37 ignore_bin not_address[13]      7      -      Occurred
```

Line 1, Column 1

Spaces: 4 Plain Text

Code coverage:

```
C:\Users\HP\Downloads\SPI UVM\SPI UVM\coverage_rpt.txt - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help

SPI_Wrapper_tb.sv | interface.sv | top.sv | spi_wrapper.sv | coverage_rpt.txt | SPI_pkg.sv

942 =====
943 === Instance: /\top#DUT
944 === Design Unit: work.spi_wrapper
945 =====
946 Statement Coverage:
947 Enabled Coverage      Bins    Hits    Misses Coverage
948 -----
949 Statements            1      1      0    100.00%
950
951 =====Statement Details=====
952
953 Statement Coverage for instance /\top#DUT --
954
955 Line      Item      Count    Source
956 ----      -
957 File spi_wrapper.sv
958 1
959                                module spi_wrapper(SPI_IF spi_intf);
960 2
961 3
962 4
963                                wire [9:0] W1;
964 5
965                                wire W2,W3;
966 6
967                                wire [7:0] W4;
968 7
969
970 8
971                                assign spi_intf.dut_state=m1.cs;
972 8          1          14561
973
974
975 Toggle Coverage:
976 Enabled Coverage      Bins    Hits    Misses Coverage
977 -----
978 Toggles              40      36      4    90.00%
979
980 =====Toggle Details=====
981
982 Toggle Coverage for instance /\top#DUT --
983
984 Node      1H->0L    0L->1H    "Coverage"
985 -----
986 W1[0-9]    1          1    100.00
987 W2         1          1    100.00
988 W3         1          1    100.00
989 W4[0-1]    0          0     0.00
990 W4[2-7]    1          1    100.00
991
992 Total Node Count = 20
993 Toggled Node Count = 18
994 Untoggled Node Count = 2
995
996 Toggle Coverage = 90.00% (36 of 40 bins)
997
998 =====
```

```
Line 1, Column 1
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10/24/2023 1:15 AM
ENG

C:\Users\HP\Downloads\SPI UVM\SPI UVM\coverage_rpt.txt - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help

SPI_Wrapper_tb.sv | interface.sv | top.sv | spi_wrapper.sv | coverage_rpt.txt | SPI_pkg.sv

963
964                                wire [9:0] W1;
965
966                                wire W2,W3;
967
968                                wire [7:0] W4;
969
970
971
972                                assign spi_intf.dut_state=m1.cs;
973
974
975 Toggle Coverage:
976 Enabled Coverage      Bins    Hits    Misses Coverage
977 -----
978 Toggles              40      36      4    90.00%
979
980 =====Toggle Details=====
981
982 Toggle Coverage for instance /\top#DUT --
983
984 Node      1H->0L    0L->1H    "Coverage"
985 -----
986 W1[0-9]    1          1    100.00
987 W2         1          1    100.00
988 W3         1          1    100.00
989 W4[0-1]    0          0     0.00
990 W4[2-7]    1          1    100.00
991
992 Total Node Count = 20
993 Toggled Node Count = 18
994 Untoggled Node Count = 2
995
996 Toggle Coverage = 90.00% (36 of 40 bins)
997
998 =====
```

Assertions:

```
C:\Users\HP\Downloads\SPI UVM\SPI UVM\coverage_rpt.txt - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help

coverage_rpt.txt x project_splv x
864 rx_valid 1 1 100.00
865 rx_valid 1 1 100.00
866 tx_valid 1 1 100.00
867
868 Total Node Count = 38
869 Toggled Node Count = 28
870 Untoggled Node Count = 10
871
872 Toggle Coverage = 73.68% (56 of 76 bins)
873
874 =====
875 == Instance: /\top#DUT /SPI_AS
876 == Design Unit: work.SPI_assertions
877 =====
878
879 Assertion Coverage:
880 Assertions 2 2 0 100.00%
881 -----
882 Name File(Line) Failure Count Pass Count
883 -----
884 /\top#DUT /SPI_AS/reset_assertion
885 SPI_assertions.sv(6) 0 1
886 /\top#DUT /SPI_AS/a_not_reading_data
887 SPI_assertions.sv(18) 0 1
888
889 Branch Coverage:
890 Enabled Coverage Bins Hits Misses Coverage
891 -----
892 Branches 2 2 0 100.00%
893
894 =====Branch Details=====
895
896 Branch Coverage for instance /\top#DUT /SPI_AS
897
898 Line Item Count Source
899 -----
900
910 Directive Coverage:
911 Directives 2 2 0 100.00%
912
913 DIRECTIVE COVERAGE:
914 -----
915 Name Design Design Lang File(Line) Hits Status
916 Unit UnitType
917 -----
918 /\top#DUT /SPI_AS/cover_assertion SPI_assertions Verilog SVA SPI_assertions.sv(7) 144 Covered
919
920 /\top#DUT /SPI_AS/c_not_reading_data SPI_assertions Verilog SVA SPI_assertions.sv(19) 2439 Covered
921
922 Statement Coverage:
923 Enabled Coverage Bins Hits Misses Coverage
924 -----
925 Statements 1 1 0 100.00%
926
927 =====Statement Details=====
928
929 Statement Coverage for instance /\top#DUT /SPI_AS --
930
931 Line Item Count Source
932 -----
933 File SPI_assertions.sv
934 1 module SPI_assertions(SPI_IF asser);
935
936 2
937 3 1 1454 always @(*) begin
938
939
940
941
942 =====
943 == Instance: /\top#DUT
944 == Design Unit: work.spi_wrapper
945 =====
```

FSM:

```
C:\Users\HP\Downloads\SPI UVM\SPI UVM\coverage_rpt.txt - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help

coverage_rpt.txt x project_splv x

251
252 =====FSM Details=====
253
254 FSM Coverage for instance /top#DUT /m1 --
255
256 FSM_ID: cs
257 Current State Object : cs
258 -----
259 State Value MapInfo :
260 -----
261 Line      State Name      Value
262 ----
263 29        IDLE            0
264 35        CHK_CMD         1
265 57        READ_ADD        4
266 65        READ_DATA       3
267 50        WRITE           2
268
269 Covered States :
270 -----
271 State      Hit_count
272 ----
273 IDLE       5292
274 CHK_CMD    4853
275 READ_ADD   1234
276 READ_DATA  1164
277 WRITE      7308
278
279 Covered Transitions :
280 -----
281 Line      Trans_ID      Hit_count      Transition
282 ----
283 31         0          4853          IDLE -> CHK_CMD
284 47         1          617          CHK_CMD -> READ_ADD
285 43         2          582          CHK_CMD -> READ_DATA
286 40         3          3654         CHK_CMD -> WRITE
287 63         5          617          READ_ADD -> IDLE
288 70         6          582          READ_DATA -> IDLE
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
=====Statement Details=====
```

Activate Windows
Go to Settings to activate Windows.

Line 1, Column 1

Type here to search

C:\Users\HP\Downloads\SPI UVM\SPI UVM\coverage_rpt.txt - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help

```
coverage_rpt.txt x project_splv x

269 -----
270 State      Hit_count
271 ----
272 IDLE       5292
273 CHK_CMD    4853
274 READ_ADD   1234
275 READ_DATA  1164
276 WRITE      7308
277
278 Covered Transitions :
279 -----
280 Line      Trans_ID      Hit_count      Transition
281 ----
282 31         0          4853          IDLE -> CHK_CMD
283 47         1          617          CHK_CMD -> READ_ADD
284 43         2          582          CHK_CMD -> READ_DATA
285 40         3          3654         CHK_CMD -> WRITE
286 63         5          617          READ_ADD -> IDLE
287 70         6          582          READ_DATA -> IDLE
288 55         7          3654          WRITE -> IDLE
289
290 Uncovered Transitions :
291 -----
292 Line      Trans_ID      Transition
293 ----
294 38         4          CHK_CMD -> IDLE
295
296
297
298
299
300
301
302
303
304
Summary
-----
Bins Hits Misses Coverage
-----
FSM States      5     5     0  100.00%
FSM Transitions 8     7     1   87.50%
Statement Coverage:
-----
Enabled Coverage
-----
Statements      50    49     1   98.00%
=====Statement Details=====
```

Activate Windows
Go to Settings to activate Windows.

Line 1, Column 1

Type here to search

C:\Users\HP\Downloads\SPI UVM\SPI UVM\coverage_rpt.txt - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help

