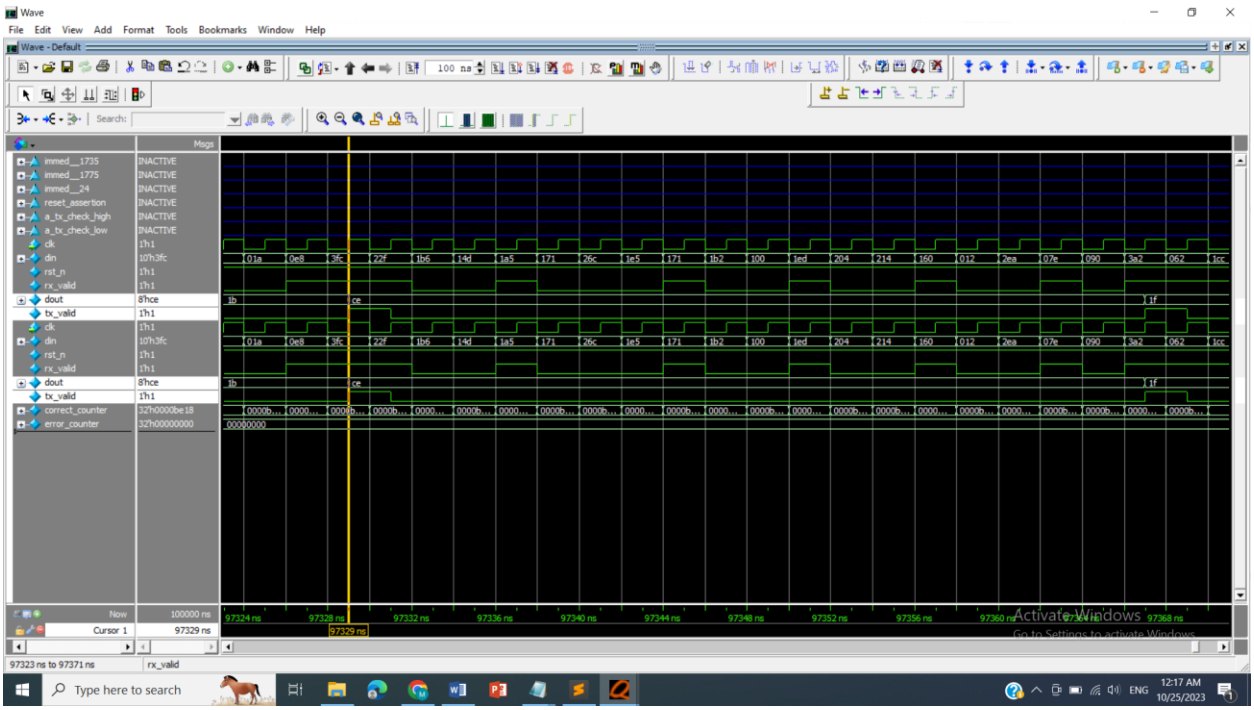
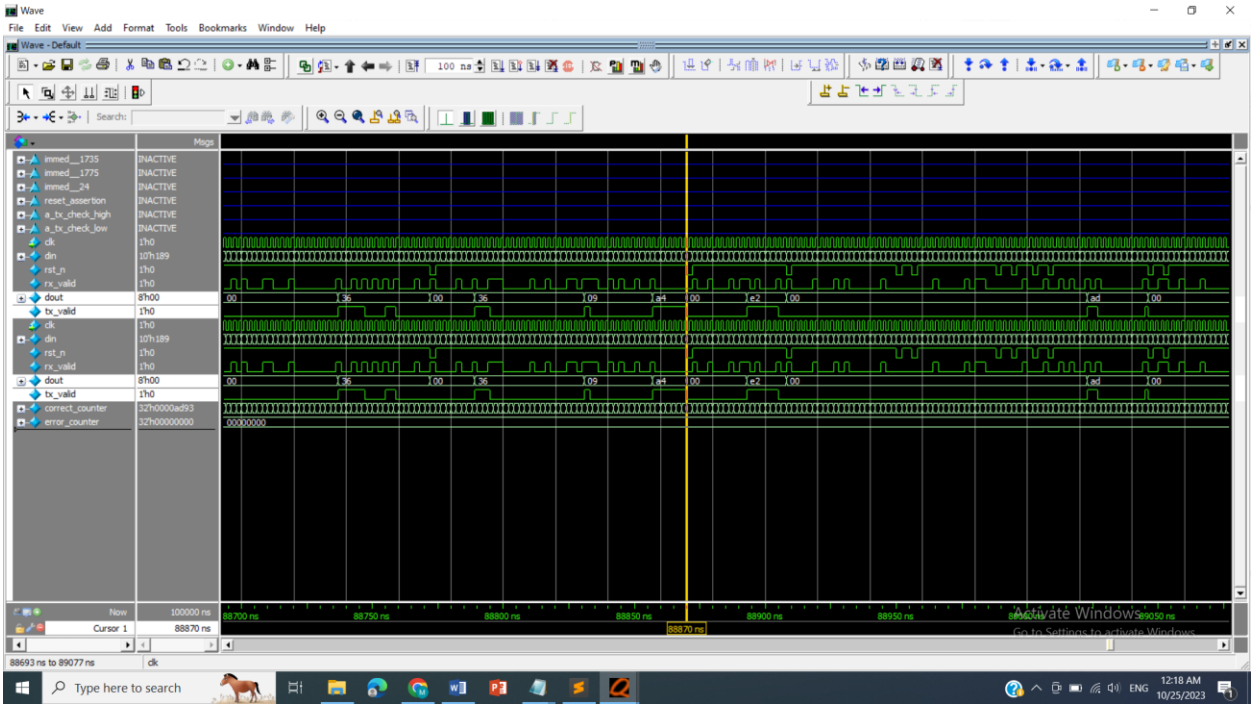
Part 1:

RAM:

Successful operation(hint the upper dout is the golden one):

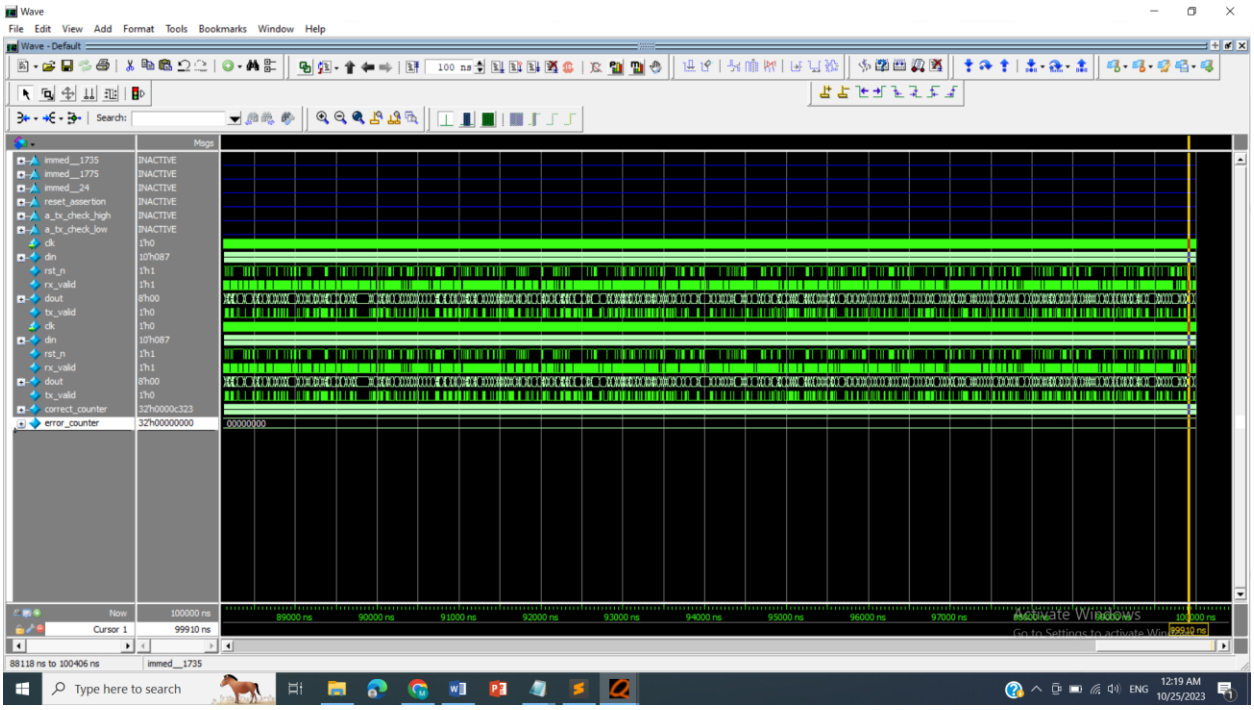


When rst is asserted:

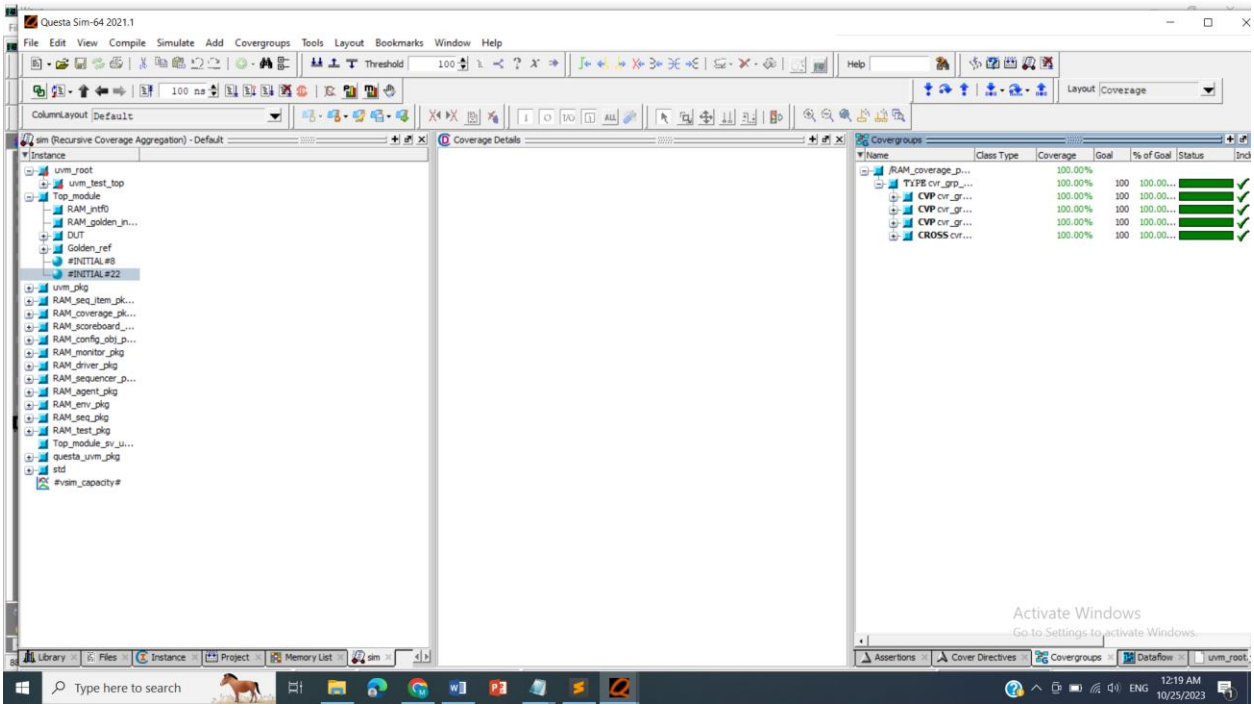


Whole WF:

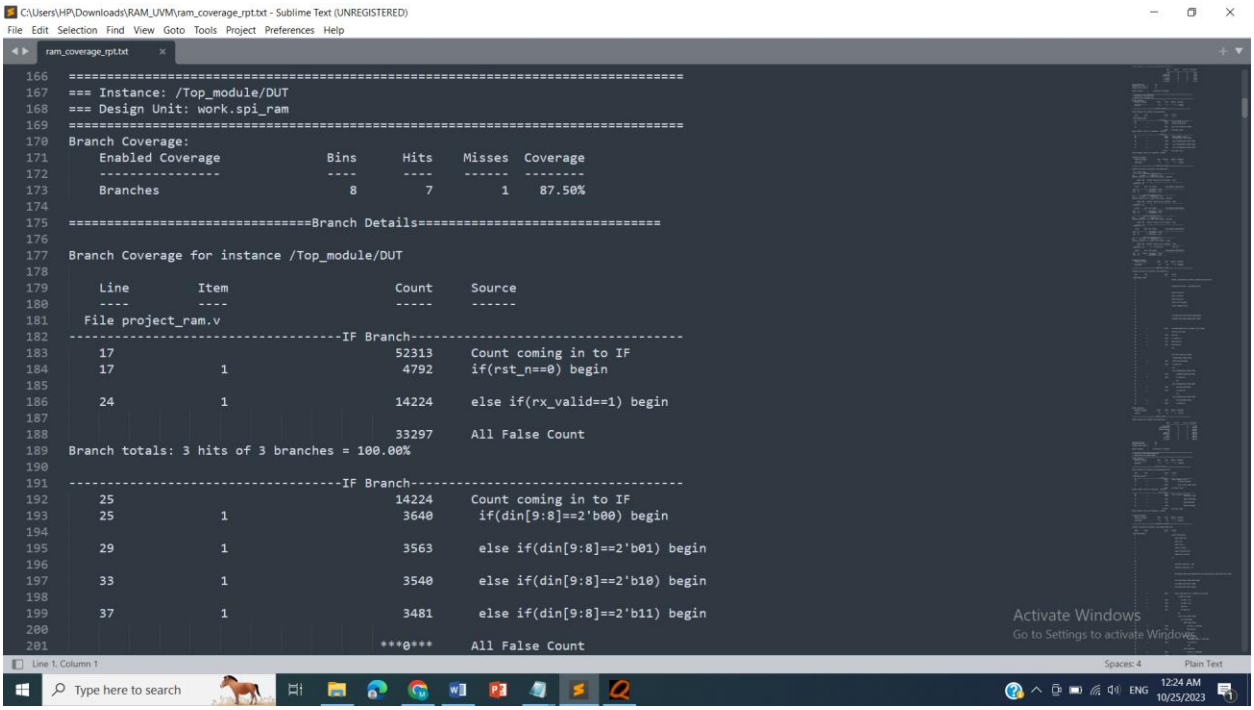
As you can see error is zero and assertions has no error:

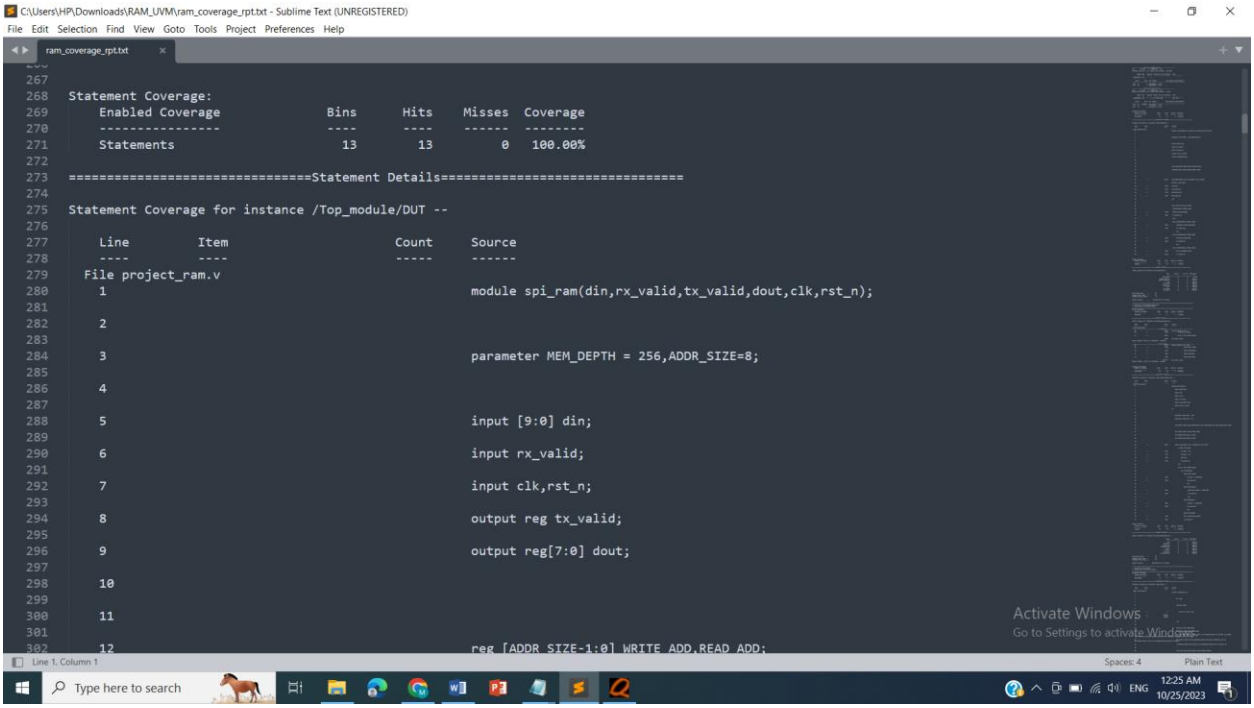


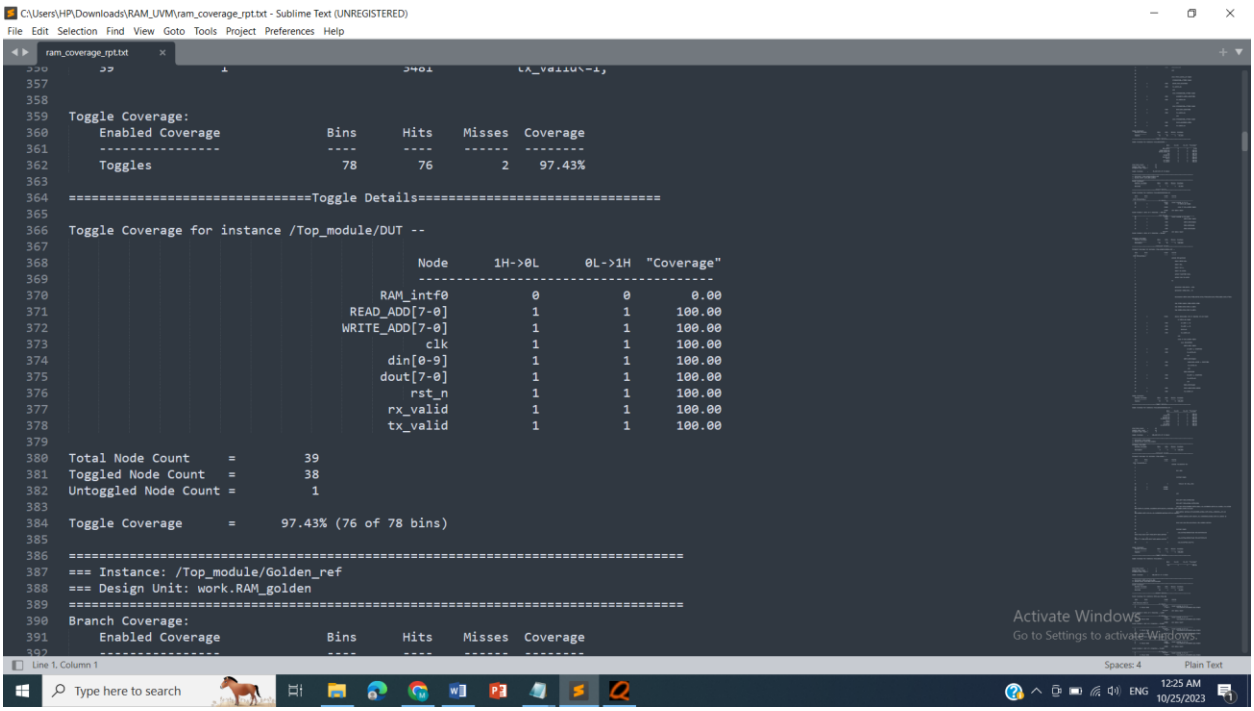
Functional coverage:



Code coverage:




C:\Users\HP\Downloads\RAM_UVM\ram_coverage_rpt.txt - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help
ram_coverage_rpt.txt
Statement Coverage:
Enabled Coverage Bins Hits Misses Coverage
Statements 13 13 0 100.00%
==========Statement Details==========
Statement Coverage for instance /Top_module/DUT --
Line Item Count Source
File project_ram.v
1 module spi_ram(din,rx_valid,tx_valid,dout,clk,rst_n);
2
3 parameter MEM_DEPTH = 256,ADDR_SIZE=8;
4
5 input [9:0] din;
6 input rx_valid;
7 input clk,rst_n;
8 output reg tx_valid;
9 output reg[7:0] dout;
10
11
12 reg [ADDR_SIZE-1:0] WRITE_ADD,READ_ADD;
Activate Windows
Go to Settings to activate Windows.
Line 1, Column 1
Spaces: 4
Plain Text
Type here to search
ENG
12:25 AM
10/25/2023

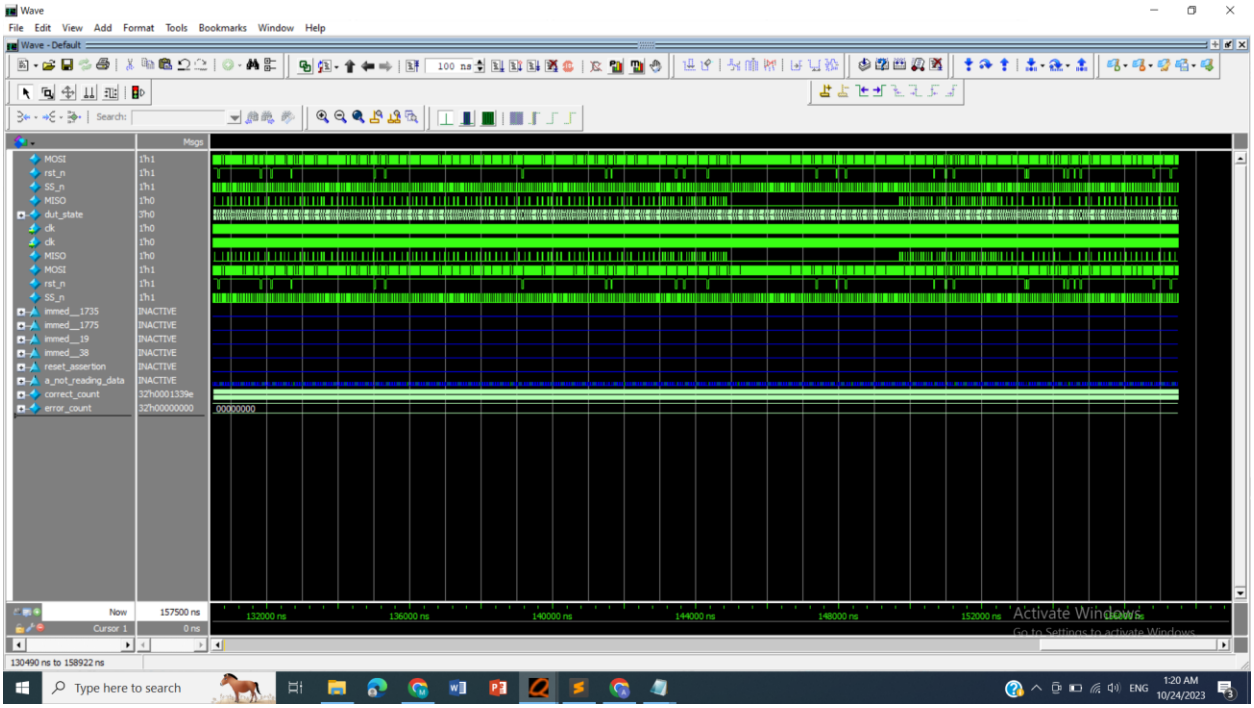

C:\Users\HP\Downloads\RAM_UVM\ram_coverage_rpt.txt - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help
ram_coverage_rpt.txt
Toggle Coverage:
Enabled Coverage Bins Hits Misses Coverage
Toggles 78 76 2 97.43%
==========Toggle Details==========
Toggle Coverage for instance /Top_module/DUT --
Node 1H->0L 0L->1H "Coverage"
RAM_intf0 0 0 0.00
READ_ADD[7-0] 1 1 100.00
WRITE_ADD[7-0] 1 1 100.00
clk 1 1 100.00
din[0-9] 1 1 100.00
dout[7-0] 1 1 100.00
rst_n 1 1 100.00
rx_valid 1 1 100.00
tx_valid 1 1 100.00
Total Node Count = 39
Toggled Node Count = 38
Untoggled Node Count = 1
Toggle Coverage = 97.43% (76 of 78 bins)
=== Instance: /Top_module/Golden_ref
=== Design Unit: work.RAM_golden
Branch Coverage:
Enabled Coverage Bins Hits Misses Coverage
Activate Windows
Go to Settings to activate Windows.
Line 1, Column 1
Spaces: 4
Plain Text
Type here to search
ENG
12:25 AM
10/25/2023

Part 2:

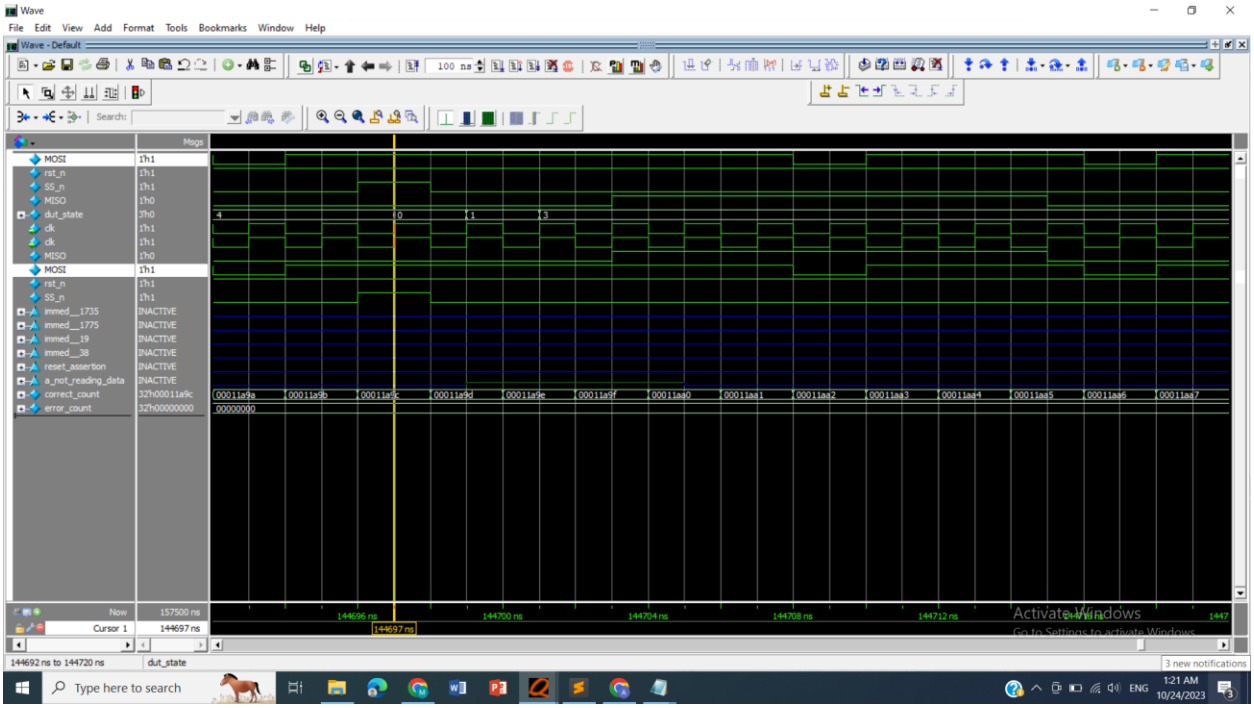
SPI:

Full Wv:

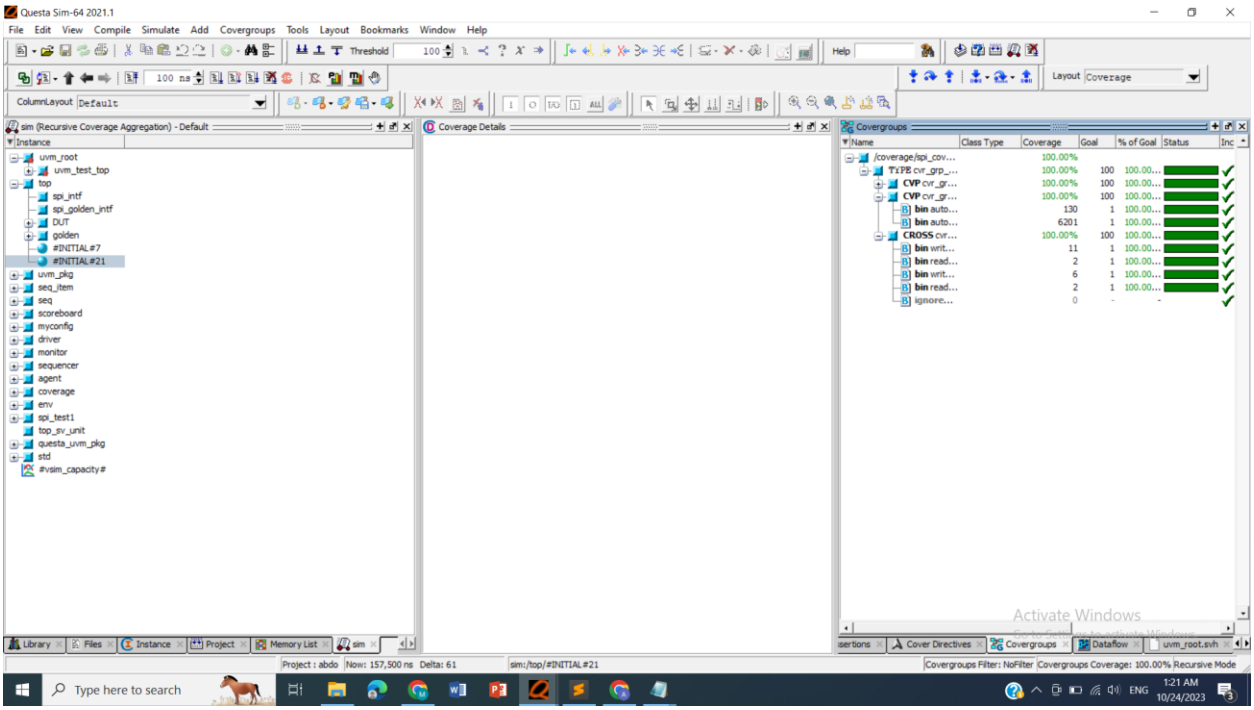
Error is zero and all assertions are fine

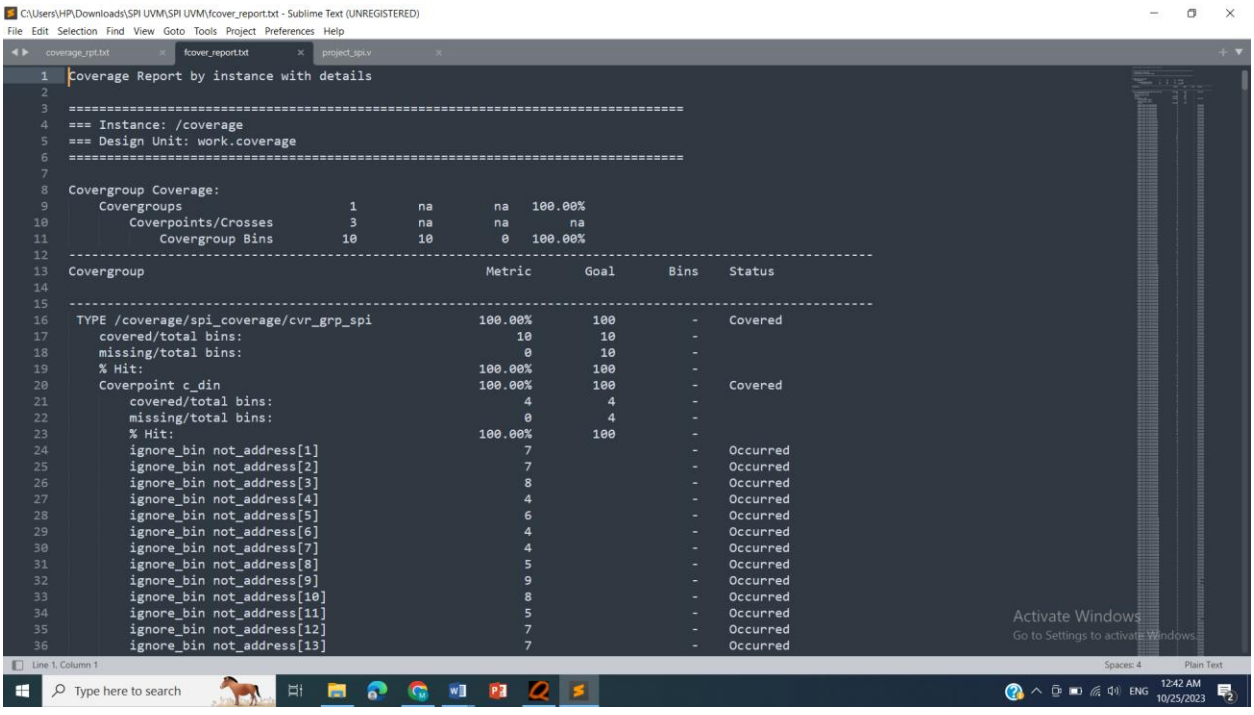


Zoom:


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
MOSI
rst_n
SS_n
MISO
dut_state
clk
clk
MISO
MOSI
rst_n
SS_n
immed__1735
immed__1775
immed__19
immed__38
reset_assertion
a_not_reading_data
correct_count
error_count
Now
Cursor 1
144696 ns
144700 ns
144704 ns
144708 ns
144712 ns
144697 ns
144692 ns to 144720 ns
dut_state
Activate Windows
Go to Settings to activate Windows.
3 new notifications
Type here to search
ENG
1:21 AM
10/24/2023

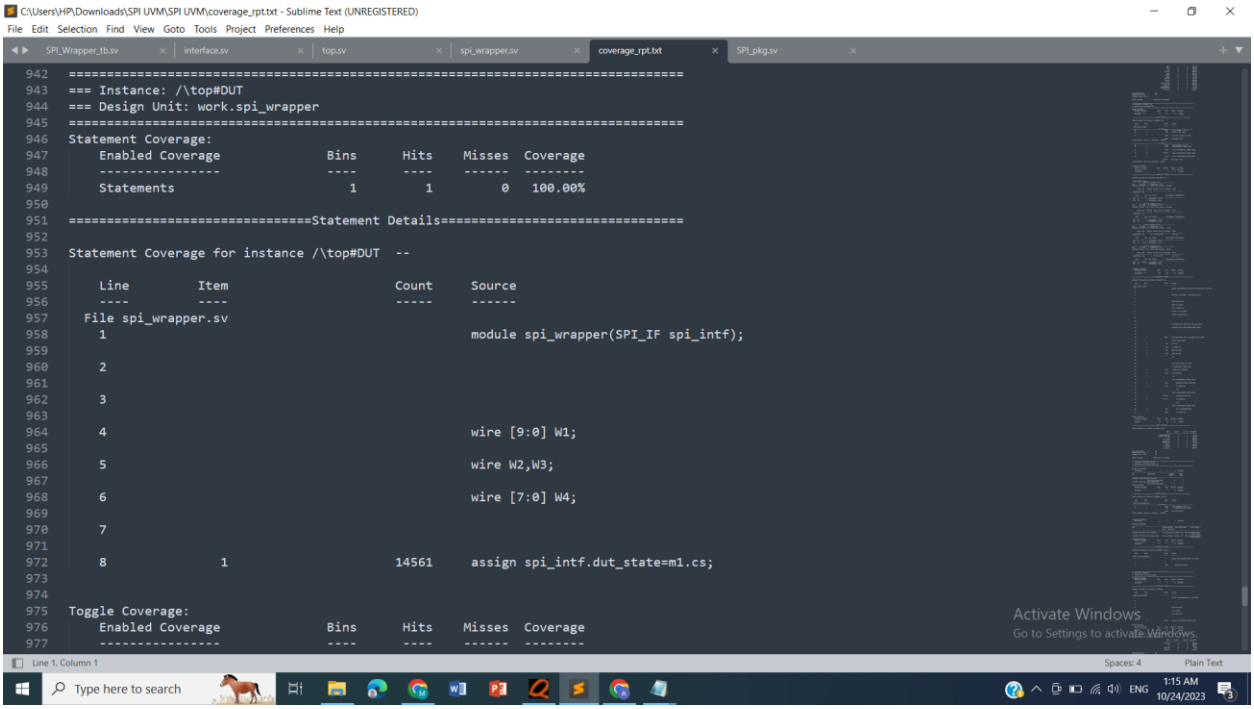
Functional coverage:



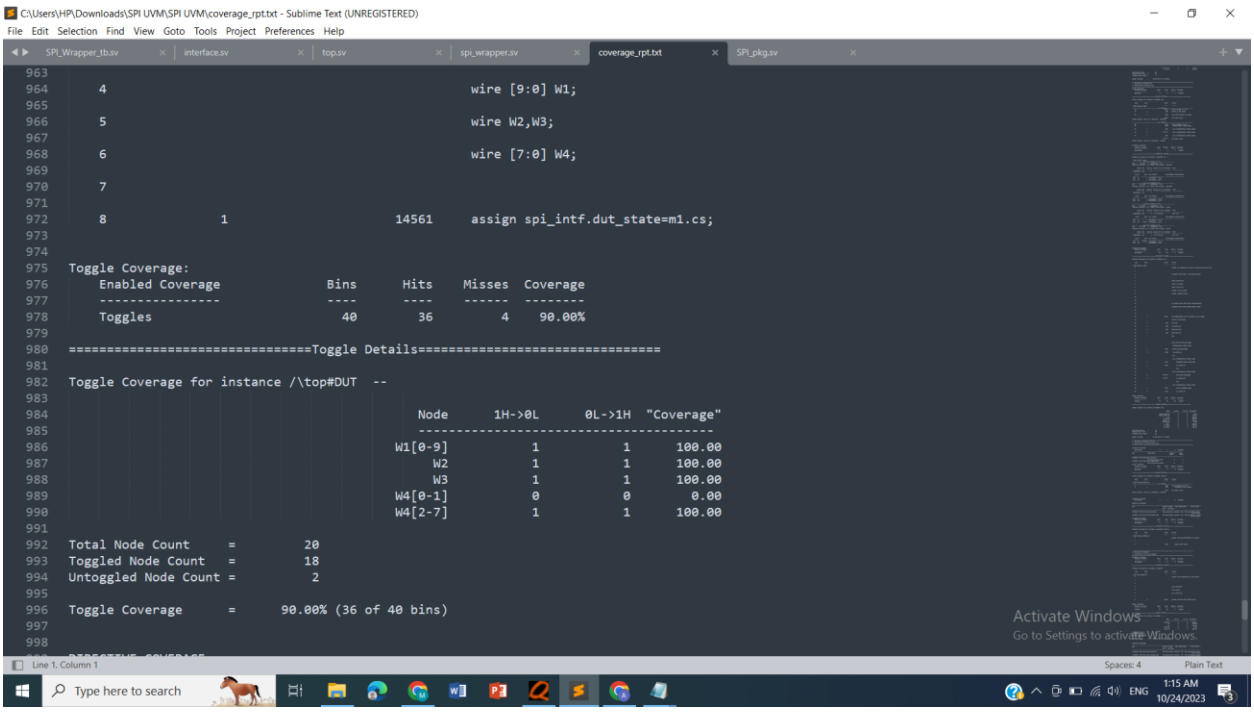



```
Coverage Report by instance with details

================================================================================
=== Instance: /coverage
=== Design Unit: work.coverage
================================================================================

Covergroup Coverage:
    Covergroups                 1        na        na   100.00%
        Coverpoints/Crosses     3        na        na        na
            Covergroup Bins    10        10         0   100.00%
----------------------------------------------------------------------------------------------------
Covergroup                                          Metric       Goal       Bins    Status

----------------------------------------------------------------------------------------------------
 TYPE /coverage/spi_coverage/cvr_grp_spi           100.00%        100          -    Covered
    covered/total bins:                                 10         10          -
    missing/total bins:                                  0         10          -
    % Hit:                                          100.00%        100          -
    Coverpoint c_din                                100.00%        100          -    Covered
        covered/total bins:                                4          4          -
        missing/total bins:                                0          4          -
        % Hit:                                      100.00%        100          -
        ignore_bin not_address[1]                          7                     -    Occurred
        ignore_bin not_address[2]                          7                     -    Occurred
        ignore_bin not_address[3]                          8                     -    Occurred
        ignore_bin not_address[4]                          4                     -    Occurred
        ignore_bin not_address[5]                          6                     -    Occurred
        ignore_bin not_address[6]                          4                     -    Occurred
        ignore_bin not_address[7]                          4                     -    Occurred
        ignore_bin not_address[8]                          5                     -    Occurred
        ignore_bin not_address[9]                          9                     -    Occurred
        ignore_bin not_address[10]                         8                     -    Occurred
        ignore_bin not_address[11]                         5                     -    Occurred
        ignore_bin not_address[12]                         7                     -    Occurred
        ignore_bin not_address[13]                         7                     -    Occurred
```

Code coverage:

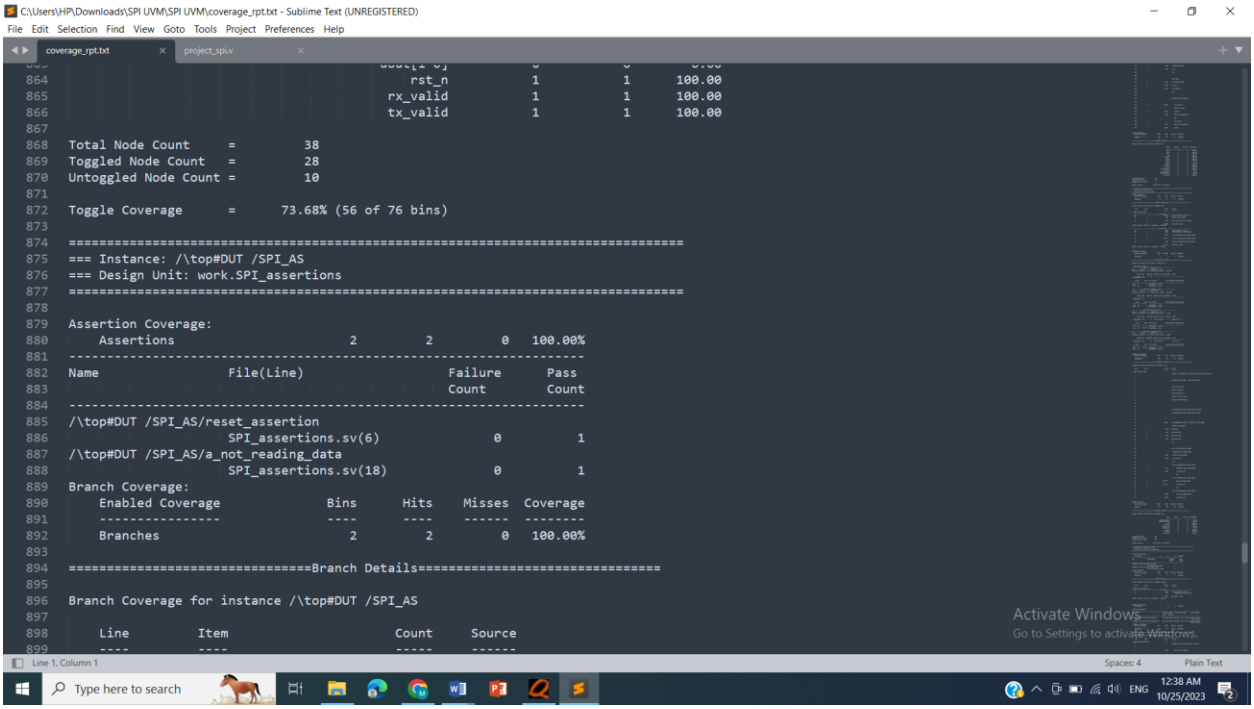


```
942  ================================================================================
943  === Instance: /\top#DUT
944  === Design Unit: work.spi_wrapper
945  ================================================================================
946  Statement Coverage:
947      Enabled Coverage             Bins      Hits    Misses  Coverage
948      ----------------             ----      ----    ------  --------
949      Statements                      1         1         0   100.00%
950
951  ================================Statement Details================================
952
953  Statement Coverage for instance /\top#DUT  --
954
955      Line         Item                    Count     Source
956      ----         ----                    -----     ------
957    File spi_wrapper.sv
958      1                                              module spi_wrapper(SPI_IF spi_intf);
959
960      2
961
962      3
963
964      4                                              wire [9:0] W1;
965
966      5                                              wire W2,W3;
967
968      6                                              wire [7:0] W4;
969
970      7
971
972      8              1                    14561     assign spi_intf.dut_state=m1.cs;
973
974
975  Toggle Coverage:
976      Enabled Coverage             Bins      Hits    Misses  Coverage
977      ----------------             ----      ----    ------  --------
```

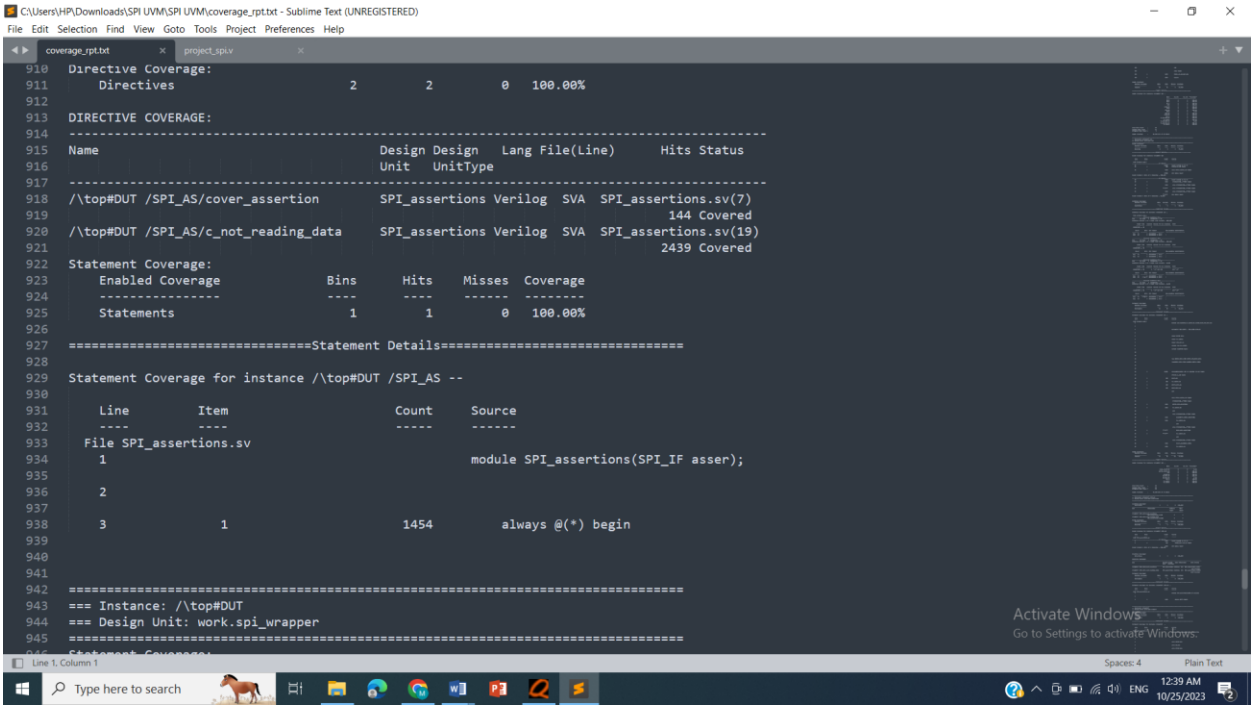


```
963
964      4                                              wire [9:0] W1;
965
966      5                                              wire W2,W3;
967
968      6                                              wire [7:0] W4;
969
970      7
971
972      8              1                    14561     assign spi_intf.dut_state=m1.cs;
973
974
975  Toggle Coverage:
976      Enabled Coverage             Bins      Hits    Misses  Coverage
977      ----------------             ----      ----    ------  --------
978      Toggles                        40        36         4    90.00%
979
980  ================================Toggle Details================================
981
982  Toggle Coverage for instance /\top#DUT  --
983
984                                          Node      1H->0L      0L->1H  "Coverage"
985                                          ----------------------------------------
986                                       W1[0-9]           1           1      100.00
987                                           W2            1           1      100.00
988                                           W3            1           1      100.00
989                                       W4[0-1]           0           0        0.00
990                                       W4[2-7]           1           1      100.00
991
992  Total Node Count     =         20
993  Toggled Node Count   =         18
994  Untoggled Node Count =          2
995
996  Toggle Coverage      =      90.00% (36 of 40 bins)
997
998
```

Assertions:

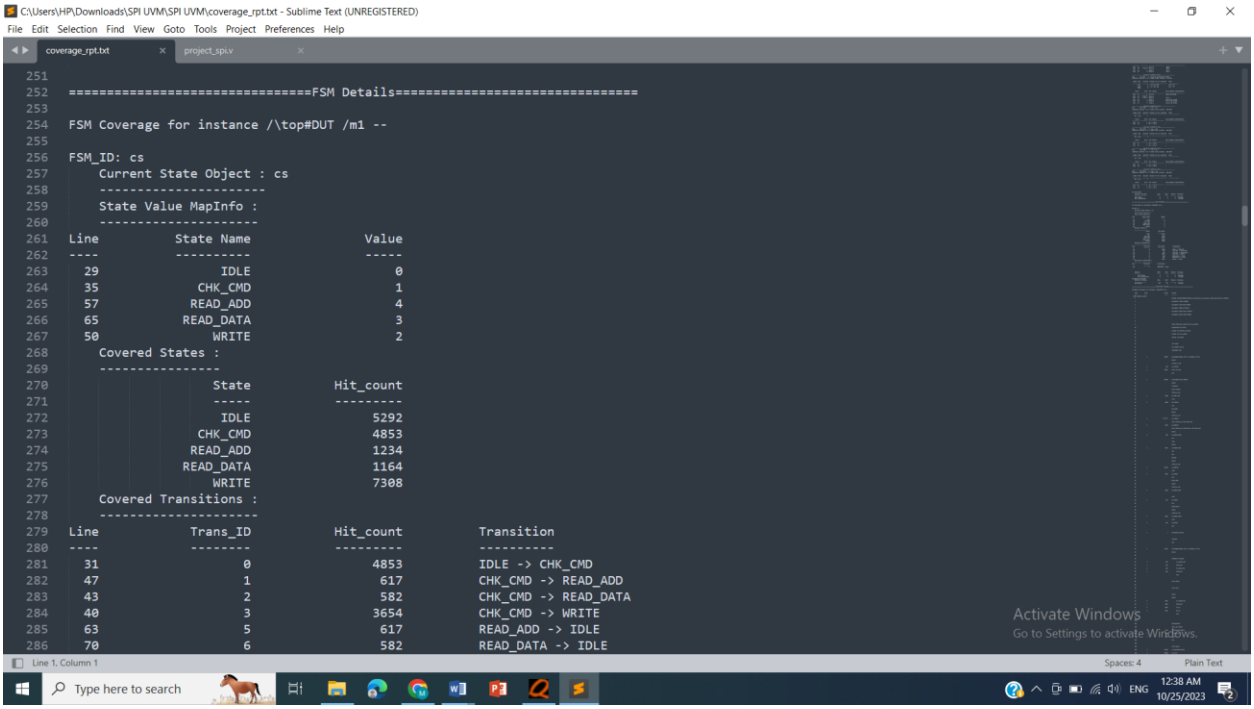


```
C:\Users\HP\Downloads\SPI UVM\SPI UVM\coverage_rpt.txt - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help
coverage_rpt.txt   project_spi.v

                                        rst_n           1          1      100.00
                                      rx_valid          1          1      100.00
                                      tx_valid          1          1      100.00

Total Node Count     =         38
Toggled Node Count   =         28
Untoggled Node Count =         10

Toggle Coverage      =      73.68% (56 of 76 bins)

================================================================================
=== Instance: /\top#DUT /SPI_AS
=== Design Unit: work.SPI_assertions
================================================================================

Assertion Coverage:
    Assertions                       2        2        0   100.00%
--------------------------------------------------------------------
Name                 File(Line)                   Failure      Pass
                                                  Count        Count
--------------------------------------------------------------------
/\top#DUT /SPI_AS/reset_assertion
                     SPI_assertions.sv(6)               0          1
/\top#DUT /SPI_AS/a_not_reading_data
                     SPI_assertions.sv(18)              0          1
Branch Coverage:
    Enabled Coverage             Bins      Hits    Misses  Coverage
    ----------------             ----      ----    ------  --------
    Branches                        2         2         0   100.00%

================================Branch Details================================

Branch Coverage for instance /\top#DUT /SPI_AS

    Line         Item                      Count     Source
    ----         ----                      -----     ------

Activate Windows
Go to Settings to activate Windows.
Line 1, Column 1                                                  Spaces: 4  Plain Text
Type here to search                                  ENG 12:38 AM 10/25/2023
```

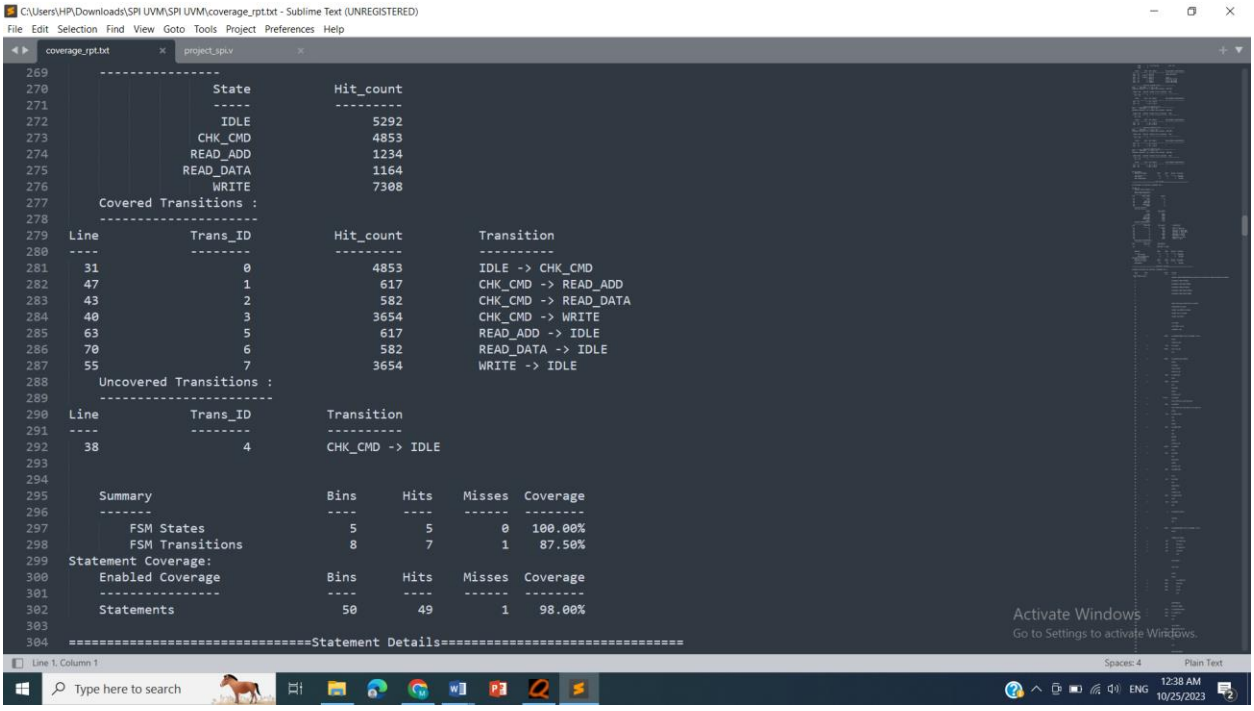


```
C:\Users\HP\Downloads\SPI UVM\SPI UVM\coverage_rpt.txt - Sublime Text (UNREGISTERED)
File Edit Selection Find View Goto Tools Project Preferences Help
coverage_rpt.txt   project_spi.v

Directive Coverage:
    Directives                       2        2        0   100.00%

DIRECTIVE COVERAGE:
--------------------------------------------------------------------------------------------
Name                                 Design Design   Lang File(Line)      Hits Status
                                     Unit   UnitType
--------------------------------------------------------------------------------------------
/\top#DUT /SPI_AS/cover_assertion    SPI_assertions Verilog  SVA  SPI_assertions.sv(7)
                                                                          144 Covered
/\top#DUT /SPI_AS/c_not_reading_data SPI_assertions Verilog  SVA  SPI_assertions.sv(19)
                                                                         2439 Covered
Statement Coverage:
    Enabled Coverage             Bins      Hits    Misses  Coverage
    ----------------             ----      ----    ------  --------
    Statements                      1         1         0   100.00%

================================Statement Details================================

Statement Coverage for instance /\top#DUT /SPI_AS --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File SPI_assertions.sv
    1                                                module SPI_assertions(SPI_IF asser);

    2

    3              1                        1454        always @(*) begin



================================================================================
=== Instance: /\top#DUT
=== Design Unit: work.spi_wrapper
================================================================================

Activate Windows
Go to Settings to activate Windows.
Line 1, Column 1                                                  Spaces: 4  Plain Text
Type here to search                                  ENG 12:39 AM 10/25/2023
```

FSM:



```
C:\Users\HP\Downloads\SPI UVM\SPI UVM\coverage_rpt.txt - Sublime Text (UNREGISTERED)
File  Edit  Selection  Find  View  Goto  Tools  Project  Preferences  Help
coverage_rpt.txt   project_spi.v

251
252  ================================FSM Details================================
253
254  FSM Coverage for instance /\top#DUT /m1 --
255
256  FSM_ID: cs
257      Current State Object : cs
258      ----------------------
259      State Value MapInfo :
260      ---------------------
261  Line          State Name              Value
262  ----          ----------              -----
263    29                IDLE                  0
264    35             CHK_CMD                  1
265    57            READ_ADD                  4
266    65           READ_DATA                  3
267    50               WRITE                  2
268      Covered States :
269      ---------------
270                      State          Hit_count
271                      -----          ---------
272                       IDLE               5292
273                    CHK_CMD               4853
274                   READ_ADD               1234
275                  READ_DATA               1164
276                      WRITE               7308
277      Covered Transitions :
278      --------------------
279  Line           Trans_ID          Hit_count          Transition
280  ----           --------          ---------          ----------
281    31                  0               4853          IDLE -> CHK_CMD
282    47                  1                617          CHK_CMD -> READ_ADD
283    43                  2                582          CHK_CMD -> READ_DATA
284    40                  3               3654          CHK_CMD -> WRITE
285    63                  5                617          READ_ADD -> IDLE
286    70                  6                582          READ_DATA -> IDLE
```

```
C:\Users\HP\Downloads\SPI UVM\SPI UVM\coverage_rpt.txt - Sublime Text (UNREGISTERED)
File  Edit  Selection  Find  View  Goto  Tools  Project  Preferences  Help
coverage_rpt.txt   project_spi.v

269      ---------------
270                      State          Hit_count
271                      -----          ---------
272                       IDLE               5292
273                    CHK_CMD               4853
274                   READ_ADD               1234
275                  READ_DATA               1164
276                      WRITE               7308
277      Covered Transitions :
278      --------------------
279  Line           Trans_ID          Hit_count          Transition
280  ----           --------          ---------          ----------
281    31                  0               4853          IDLE -> CHK_CMD
282    47                  1                617          CHK_CMD -> READ_ADD
283    43                  2                582          CHK_CMD -> READ_DATA
284    40                  3               3654          CHK_CMD -> WRITE
285    63                  5                617          READ_ADD -> IDLE
286    70                  6                582          READ_DATA -> IDLE
287    55                  7               3654          WRITE -> IDLE
288      Uncovered Transitions :
289      ----------------------
290  Line           Trans_ID          Transition
291  ----           --------          ----------
292    38                  4          CHK_CMD -> IDLE
293
294
295      Summary                     Bins      Hits    Misses  Coverage
296      -------                     ----      ----    ------  --------
297          FSM States                 5         5         0   100.00%
298          FSM Transitions            8         7         1    87.50%
299  Statement Coverage:
300      Enabled Coverage            Bins      Hits    Misses  Coverage
301      ----------------            ----      ----    ------  --------
302      Statements                   50        49         1    98.00%
303
304  ================================Statement Details================================
```