Distributed Computing and Introduction to High Performance Computing

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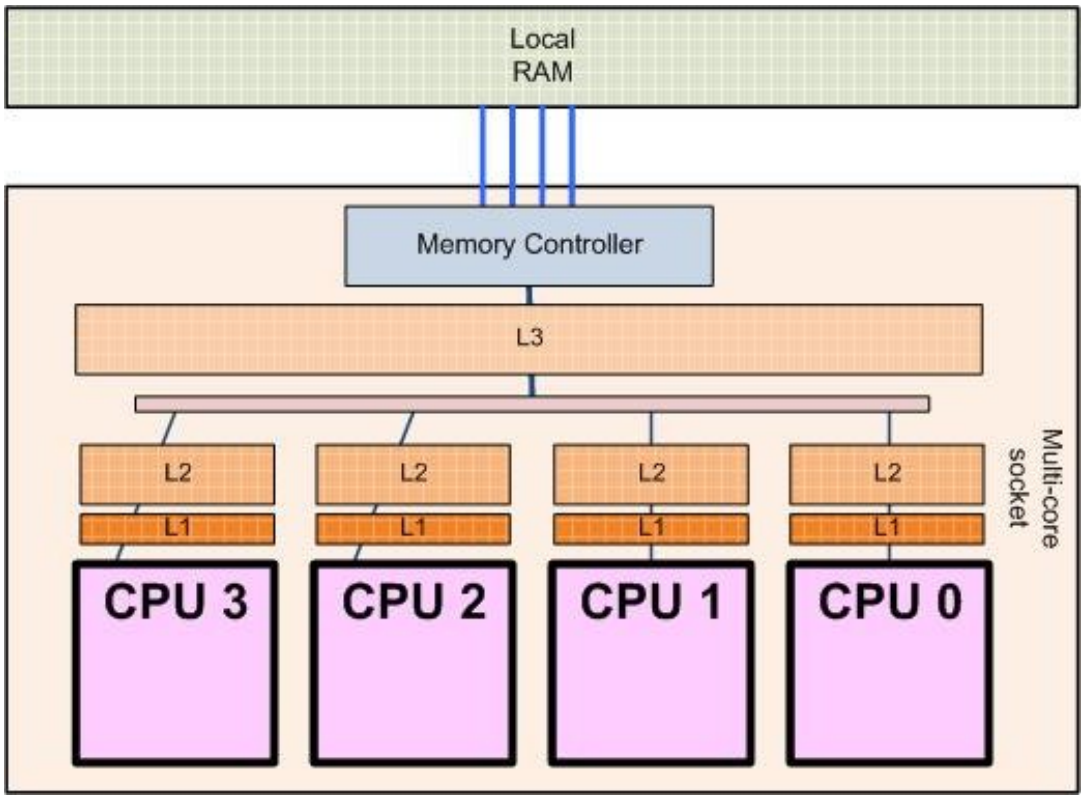
Outline of this lecture

- A brief introduction on hardwares
- Modern supercomputers
- Overview of Parallel Programming models
- Walls of modern supercomputers

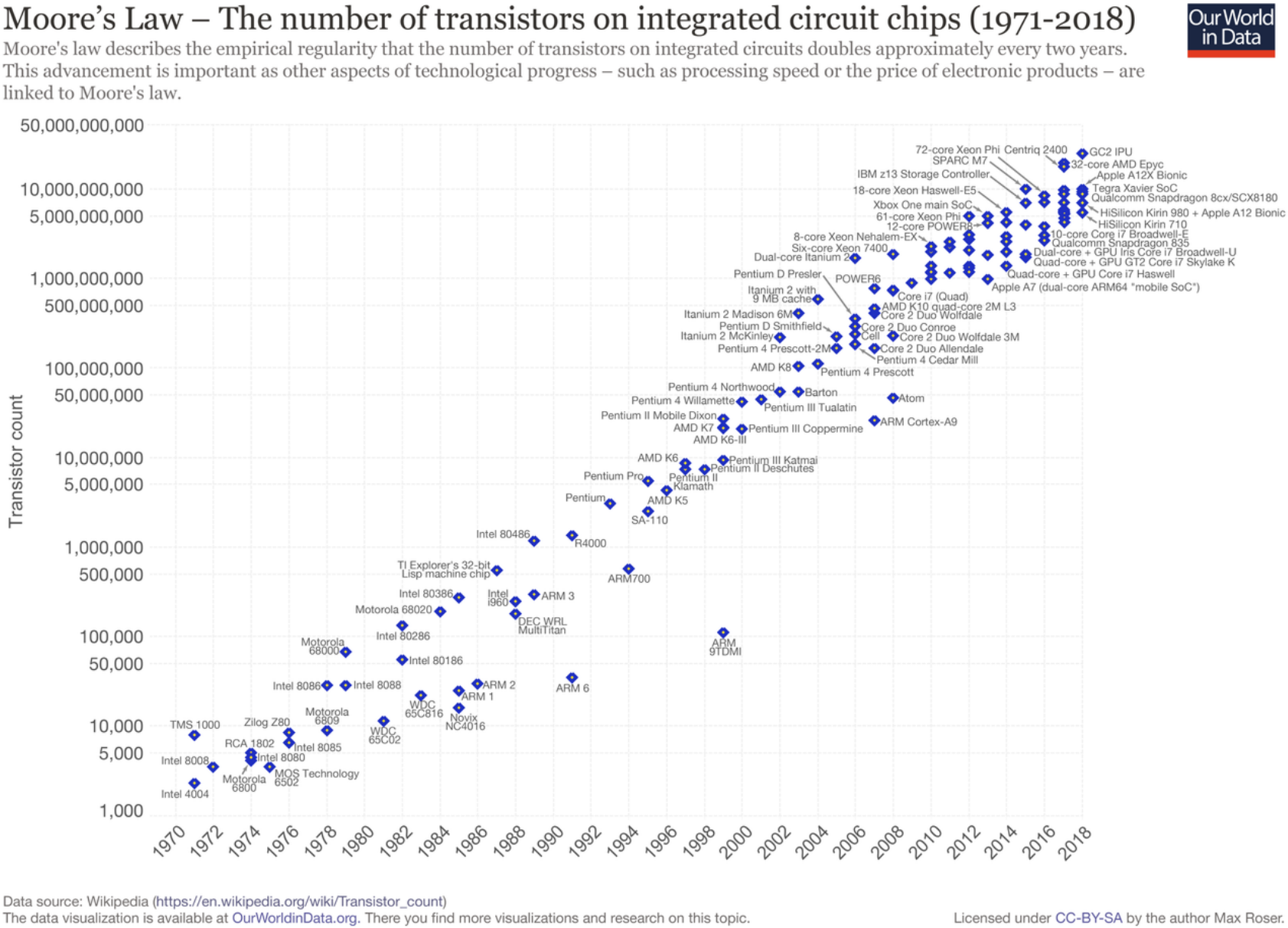
A brief introduction on hardwares

Modern architecture (CPU)



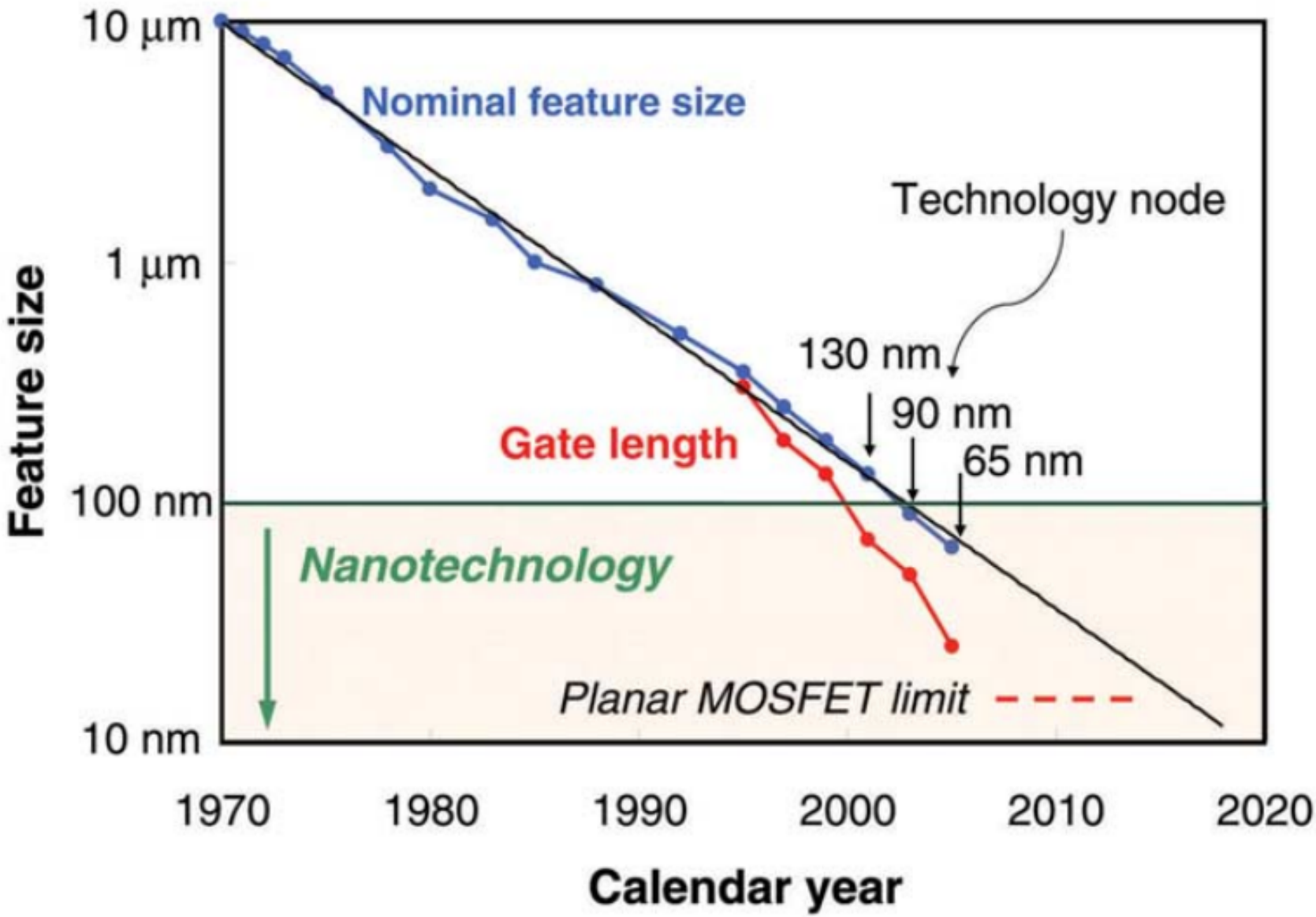
A brief introduction on hardwares

Moore's Law



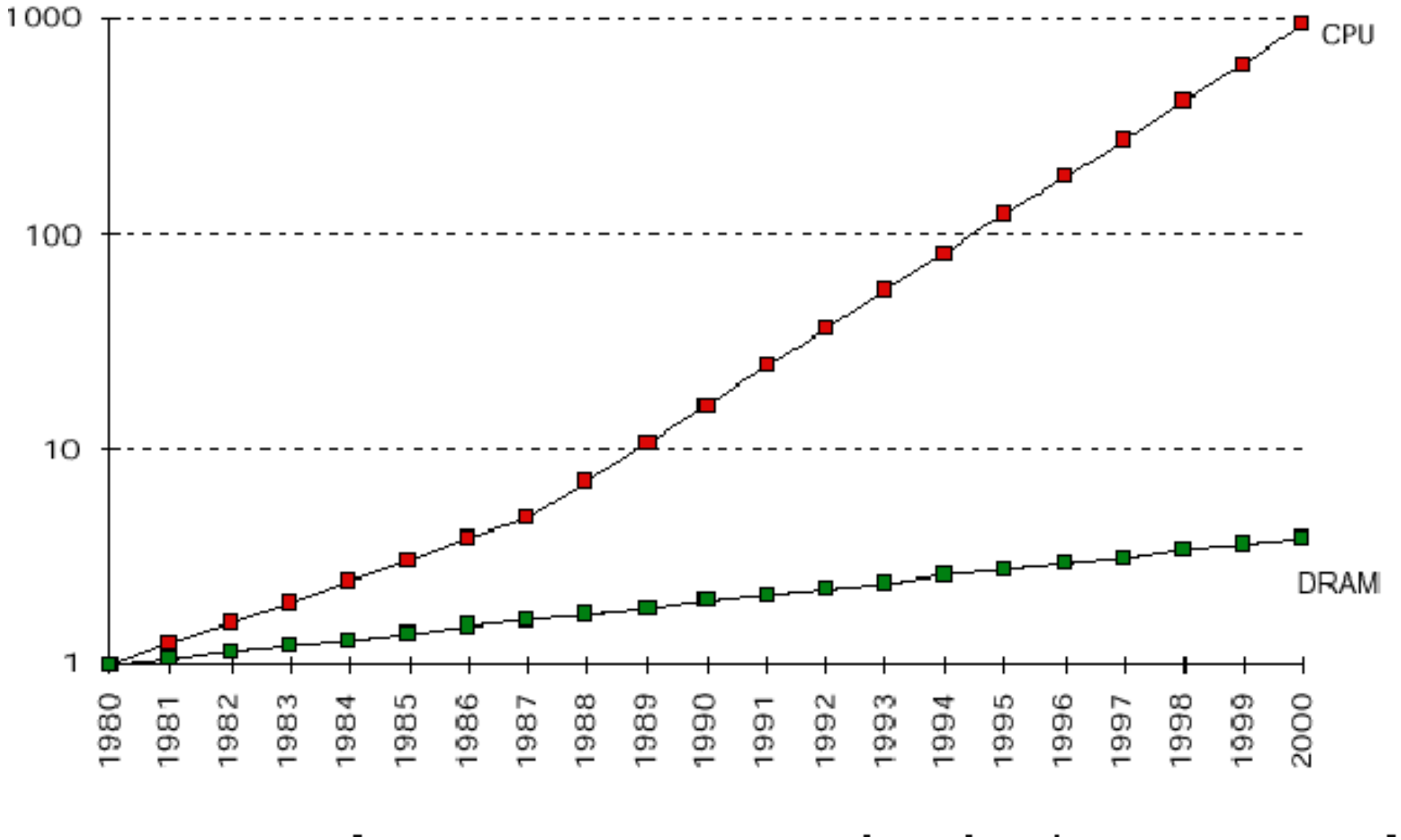
A brief introduction on hardwares

Moore's Law



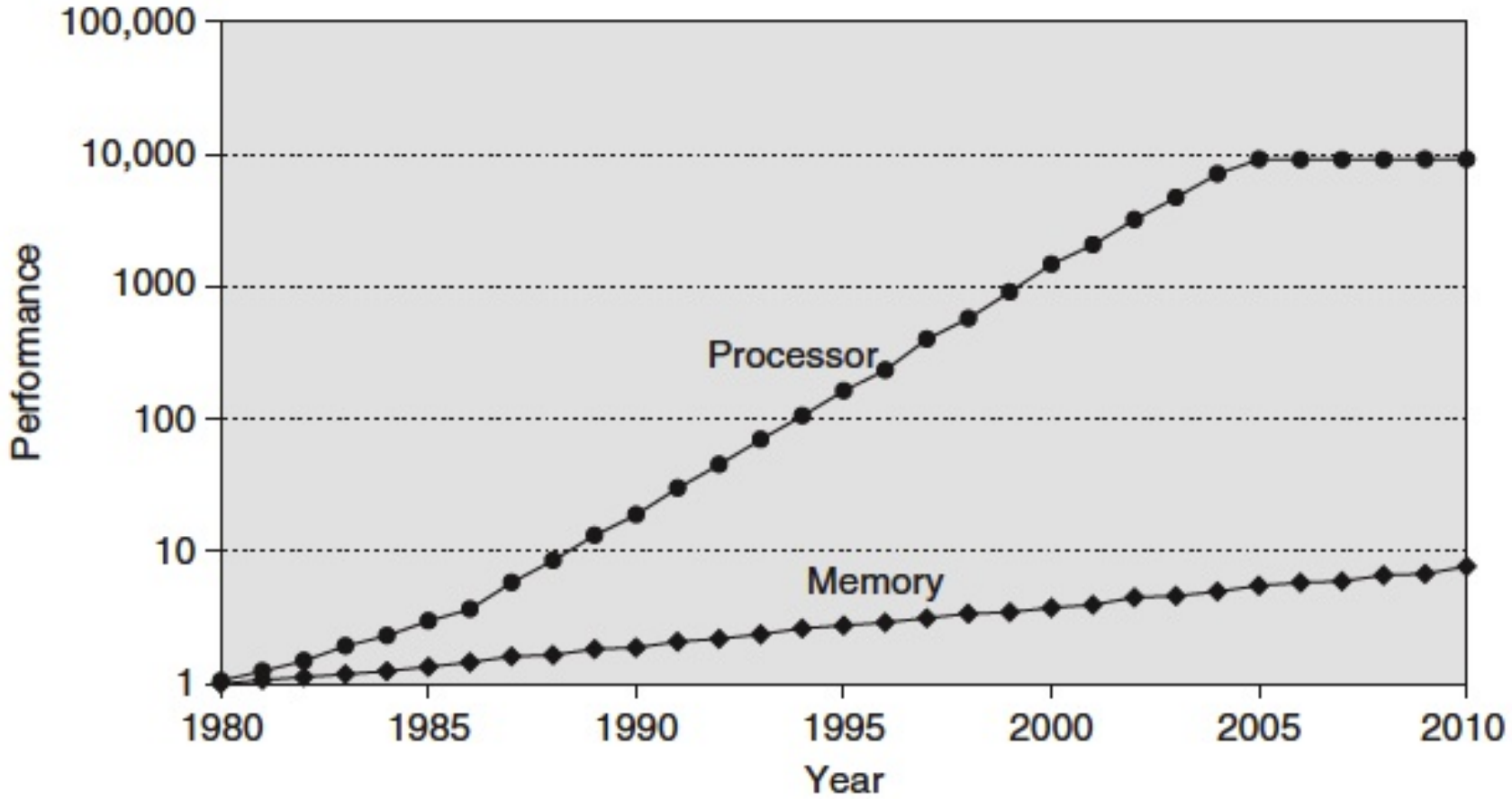
A brief introduction on hardwares

CPU vs RAM speeds



A brief introduction on hardwares

CPU vs RAM speeds



A brief introduction on hardwares

Common Processors

Processor	Launched	Number of Cores	Freq.
Xeon Platinum 9282 (formerly Cascade Lake)	2019-Q2	4-56	2.3-3.6 Ghz
E3-1500 v6 (Mobile, 7th generation)	2017-Q1	2-4	2.1-3.0 Ghz
Xeon D-1500 (formerly Broadwell)	2016-Q1	8-10	1.6-2.4 Ghz
E3-1200 v5 (Desktop, 6th generation)	2015-Q4	2-8	1.5-2.2 Ghz
Xeon E5-2600 v3 (formerly Haxwell)	2015-Q3	4	2-2.8 Ghz

Table: Some Intel processors

Processor	L2 cache	Number of Cores	Freq.
Opteron 6386 SE	16 MB	16	2.8-3.5 Ghz
Athlon X4 880K (Desktop)	4 MB	4	4.0-4.2 Ghz
Athlon X2 450K (Desktop)	1 MB	2	3.5-3.9 Ghz

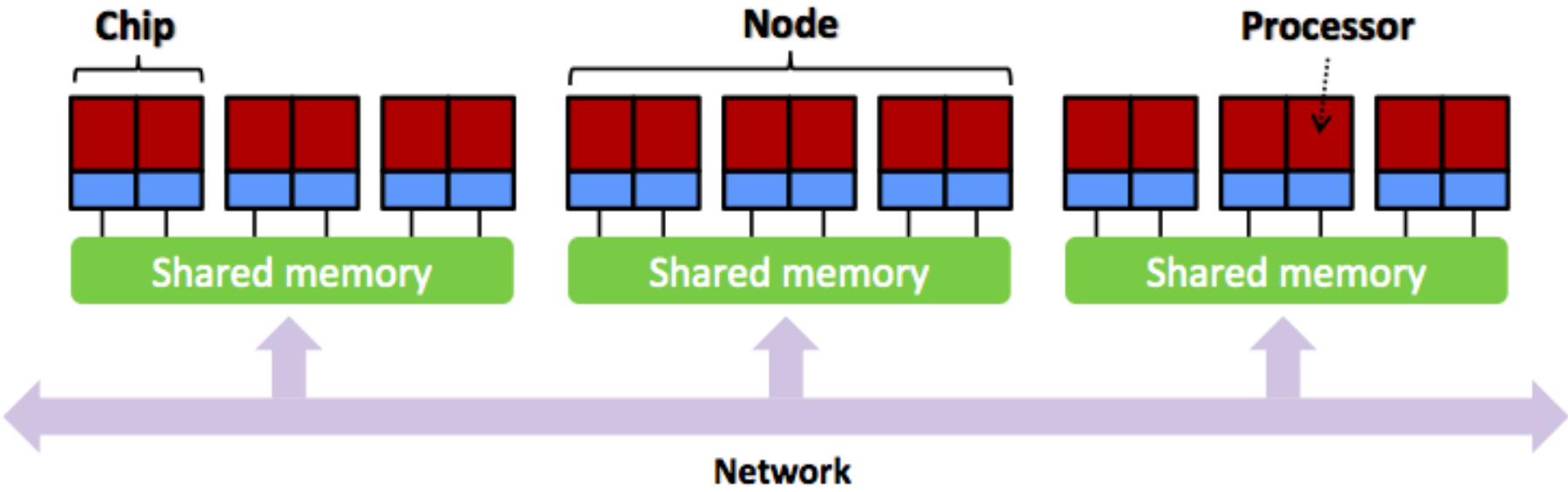
Table: Some AMD processors

➠ others: ARM (cortex, . . .), FPGA, . . .

Modern supercomputers

What is a supercomputer?

Cluster



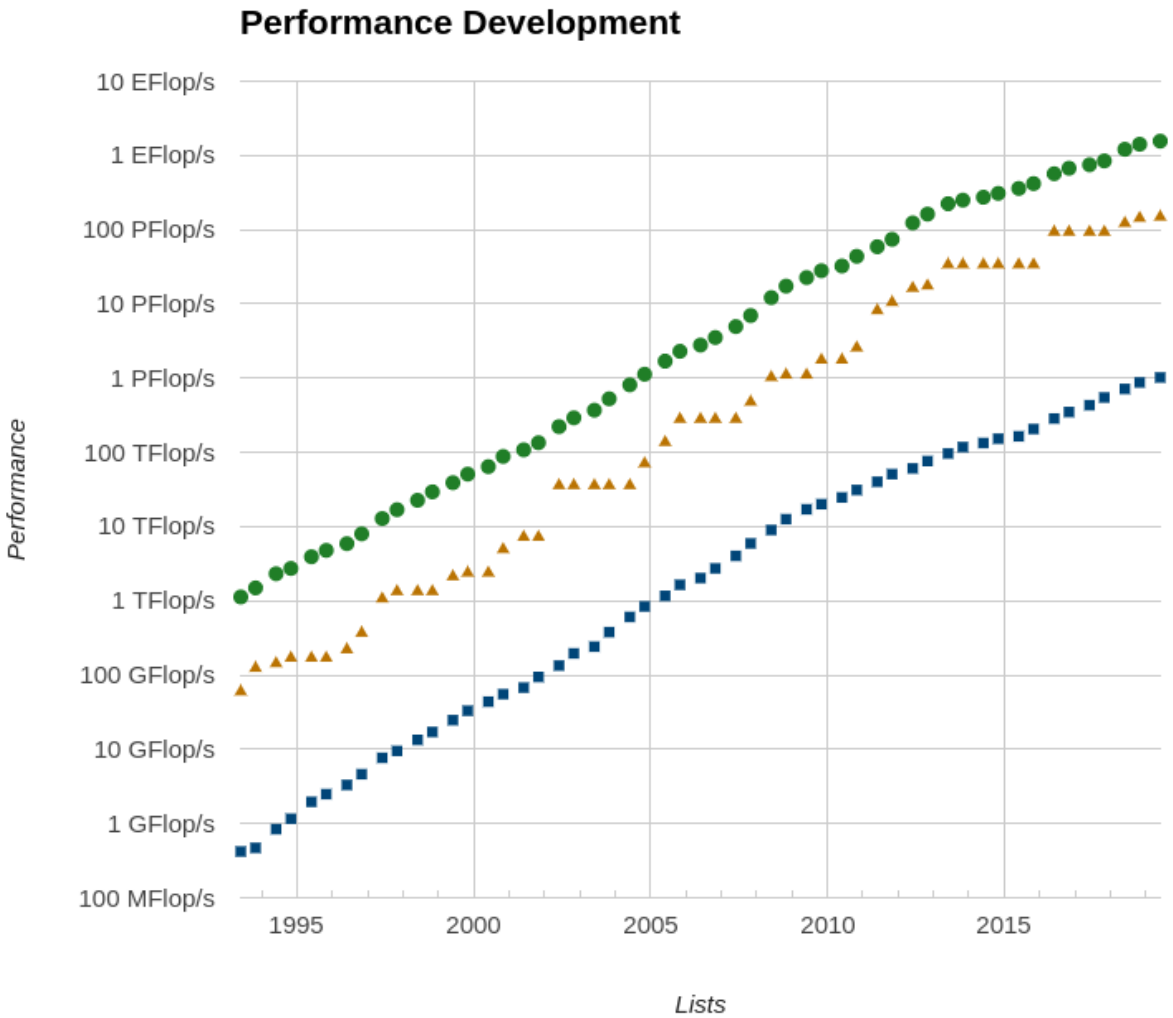
Modern supercomputers

What is a supercomputer?

Summit ORNL (USA)

Modern supercomputers

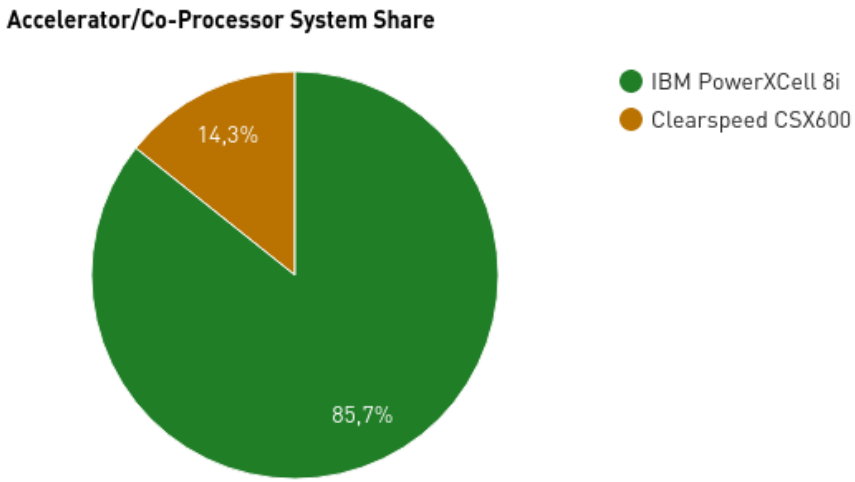
Top 500



Modern supercomputers

Top 500 Family system share evolution

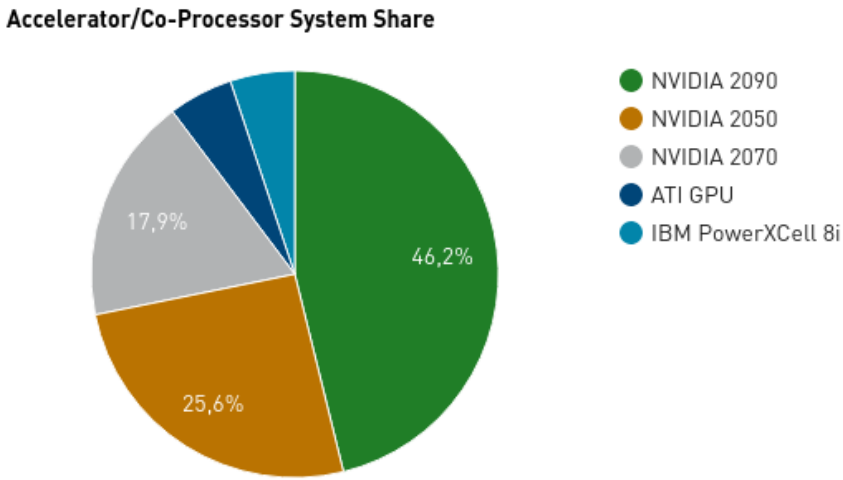
November 2009



Modern supercomputers

Top 500 Family system share evolution

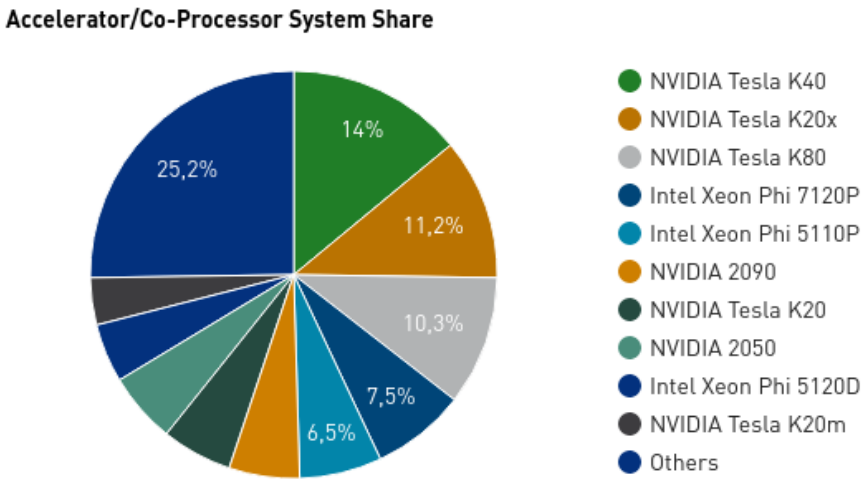
November 2011



Modern supercomputers

Top 500 Family system share evolution

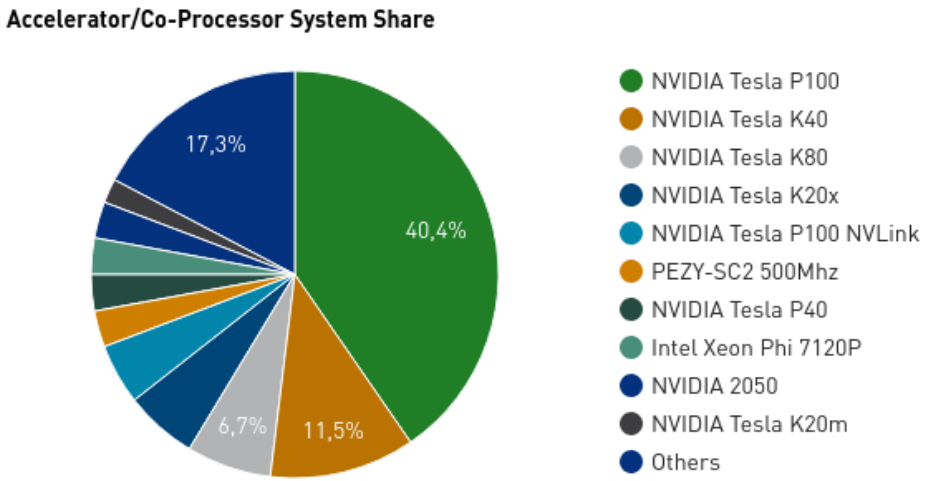
November 2015



Modern supercomputers

Top 500 Family system share evolution

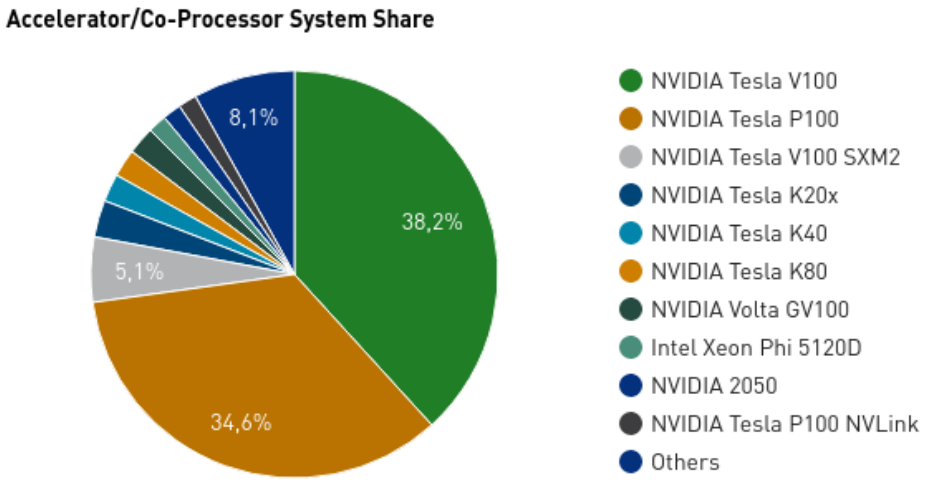
November 2017



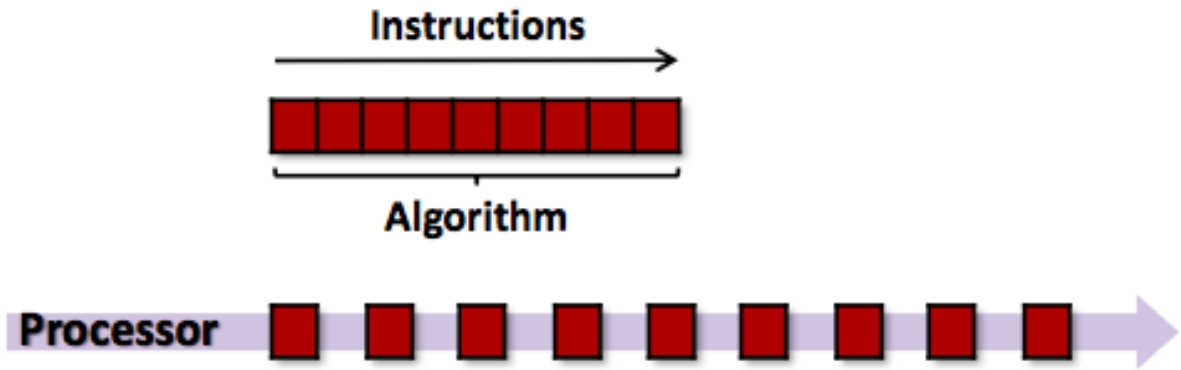
Modern supercomputers

Top 500 Family system share evolution

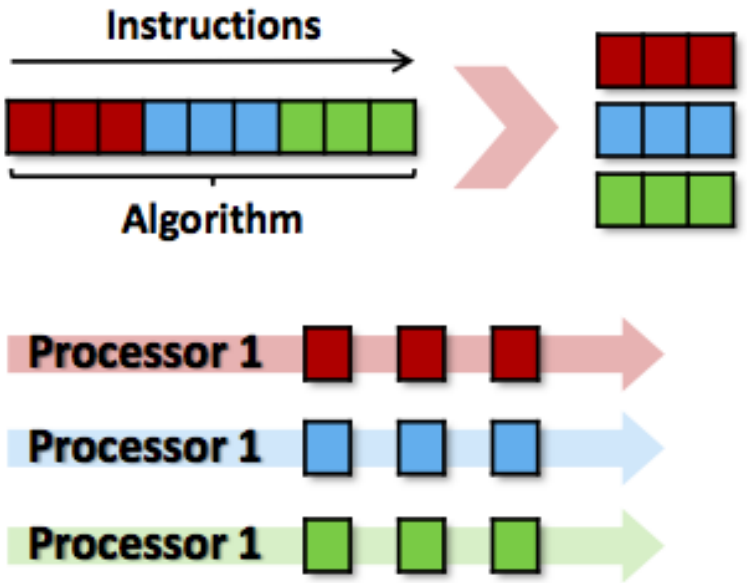
Juin 2019



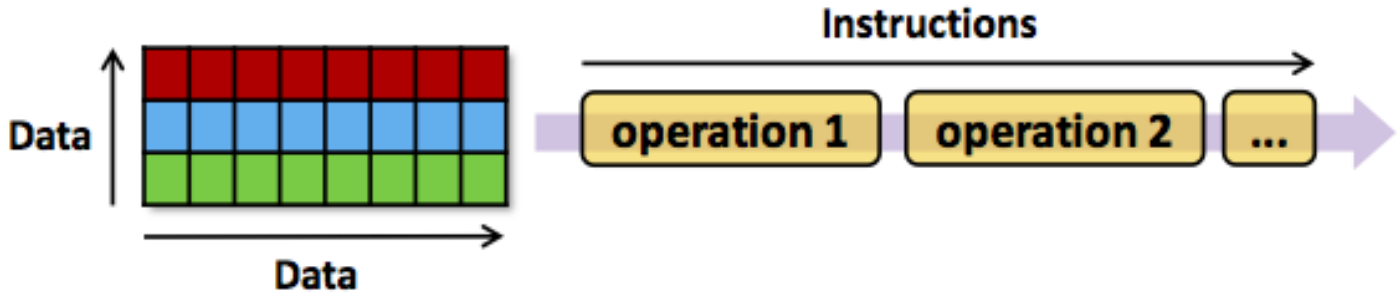
Serial problem



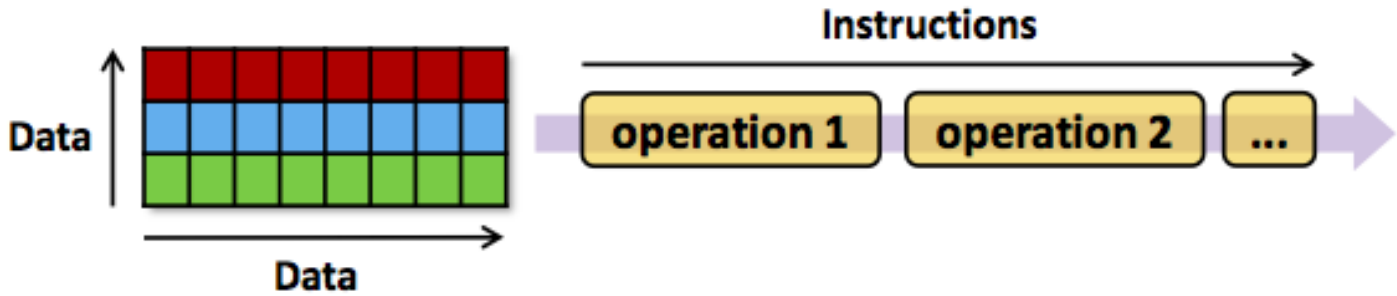
Parallel problem



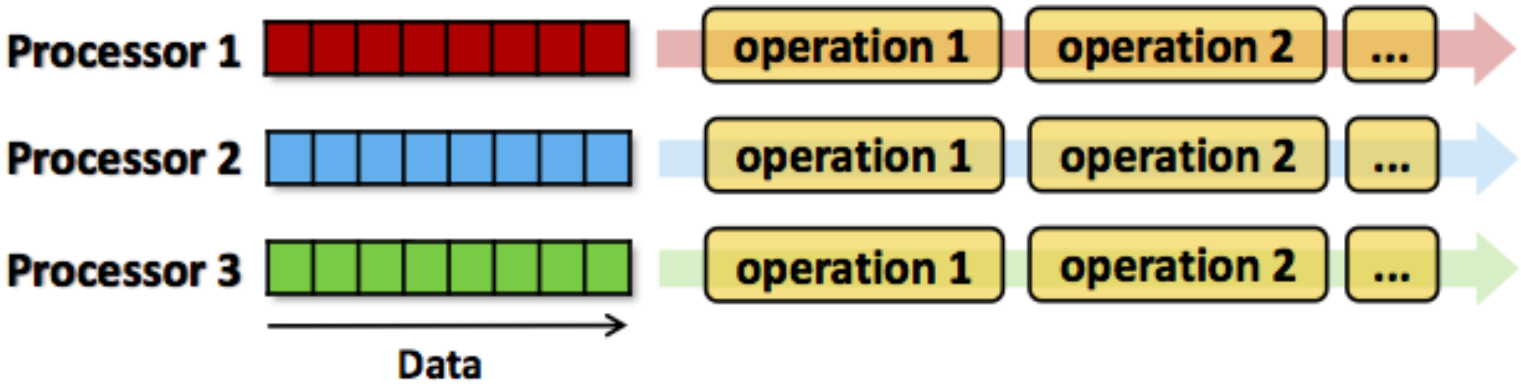
Setting



Setting

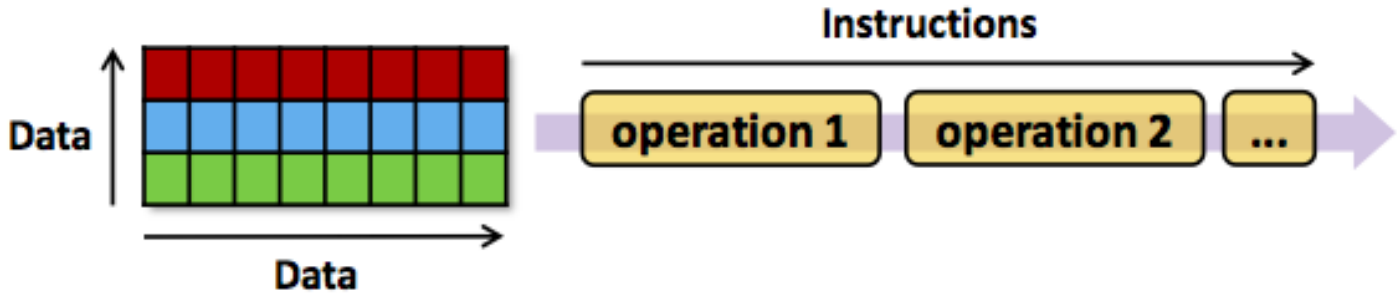


data parallelism

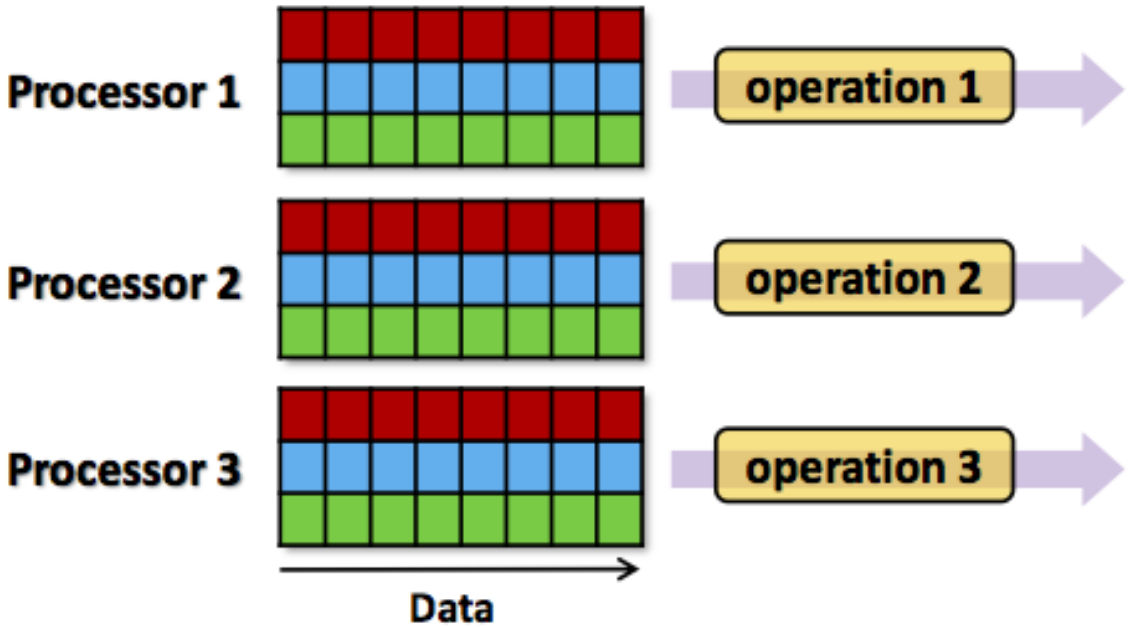


Parallel strategies

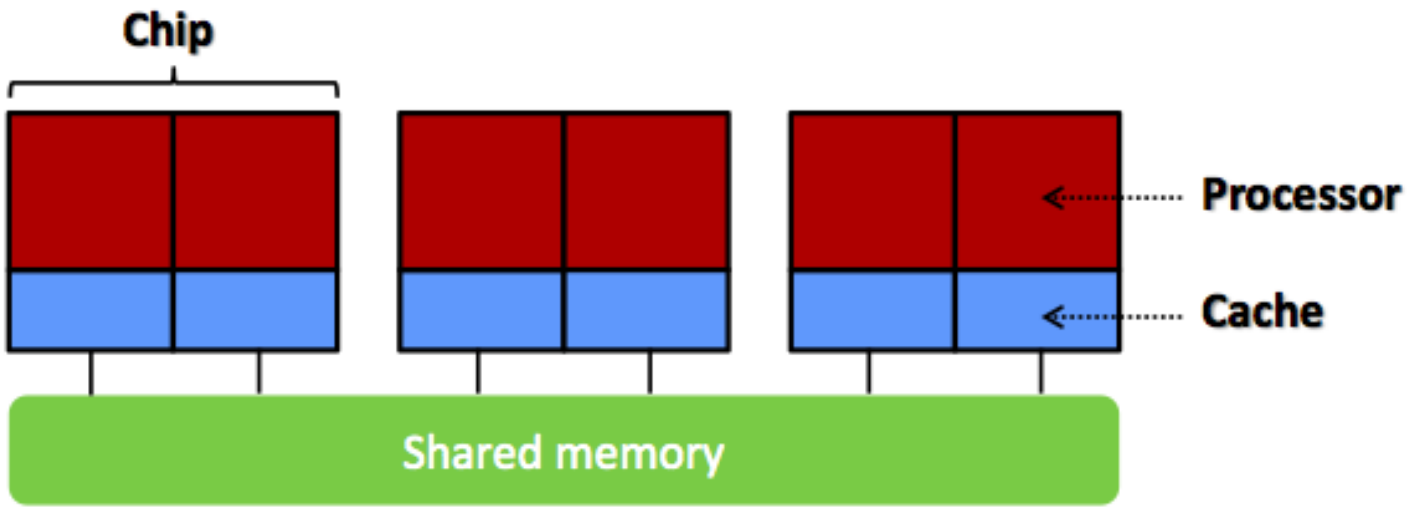
Setting



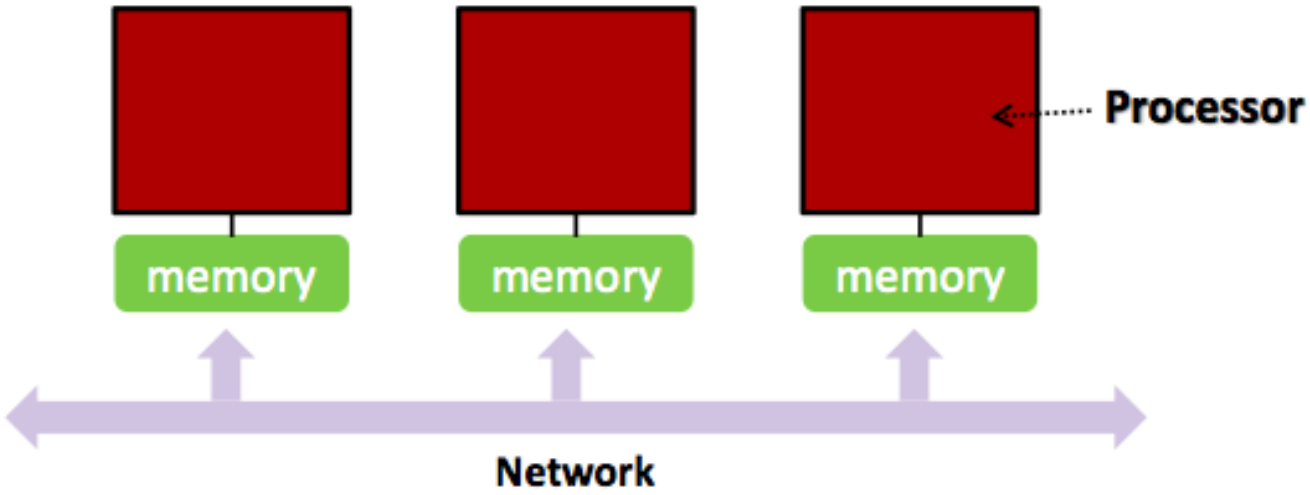
task parallelism



shared memory



distributed memory



Walls of modern supercomputers

- Programming wall
  - writing parallel codes is time-consuming
- Memory wall
  - Latency of the memory is decreasing very slowly
  - Concurence: number of cores per memory module is increasing
  - Technological advances on memory are very slow
- Portability wall
  - CPUs, GPUs, FPGAs
  - Portability is mandatory
- Power wall
  - Dissipated power $\sim \omega^3$ (freq.)
  - Dissipated power per cm^2 is limited by the cooling system
  - Power costs are expensive (critical for Exascales)

Walls of modern supercomputers

- The computing power of supercomputers is doubling every year (faster than Moore's Law, but electrical consumption is also increasing).
- The number of cores is increasing rapidly (massively parallel (IBM Blue Gene Q) and many-cores architectures (Intel Xeon Phi, GPUs)).
- Emergence of heterogeneous accelerated architectures (standard processors coupled with GPU).
- Machine architecture is becoming more complex and the number of layers increasing (processors/cores, memory access, network and I/O).
- Memory per core has been stagnating and is beginning to decrease.
- Performance per core is stagnating and is much lower on some machines than on a simple laptop (IBM Blue Gene).
- Throughput towards the disk and memory is increasing more slowly than the computing power.

Walls of modern supercomputers

Consequences

Consequences for the applications

- It is necessary to exploit a large number of relatively slow cores.
- Tendancy for individual core memory to decrease: Necessity to not waste memory.
- Higher level of parallelism continually needed for the efficient usage of modern architectures (regarding both computing power and memory size).
- The I/O also becoming an increasingly current problem.

Consequences for the developers

- The time has ended when you only needed to wait a while to obtain better performance (i.e. stagnation of computing power per core).
- Increased necessity to understand the hardware architecture.
- More and more difficult to develop codes on your own (need for experts in HPC as well as multi-disciplinary teams).