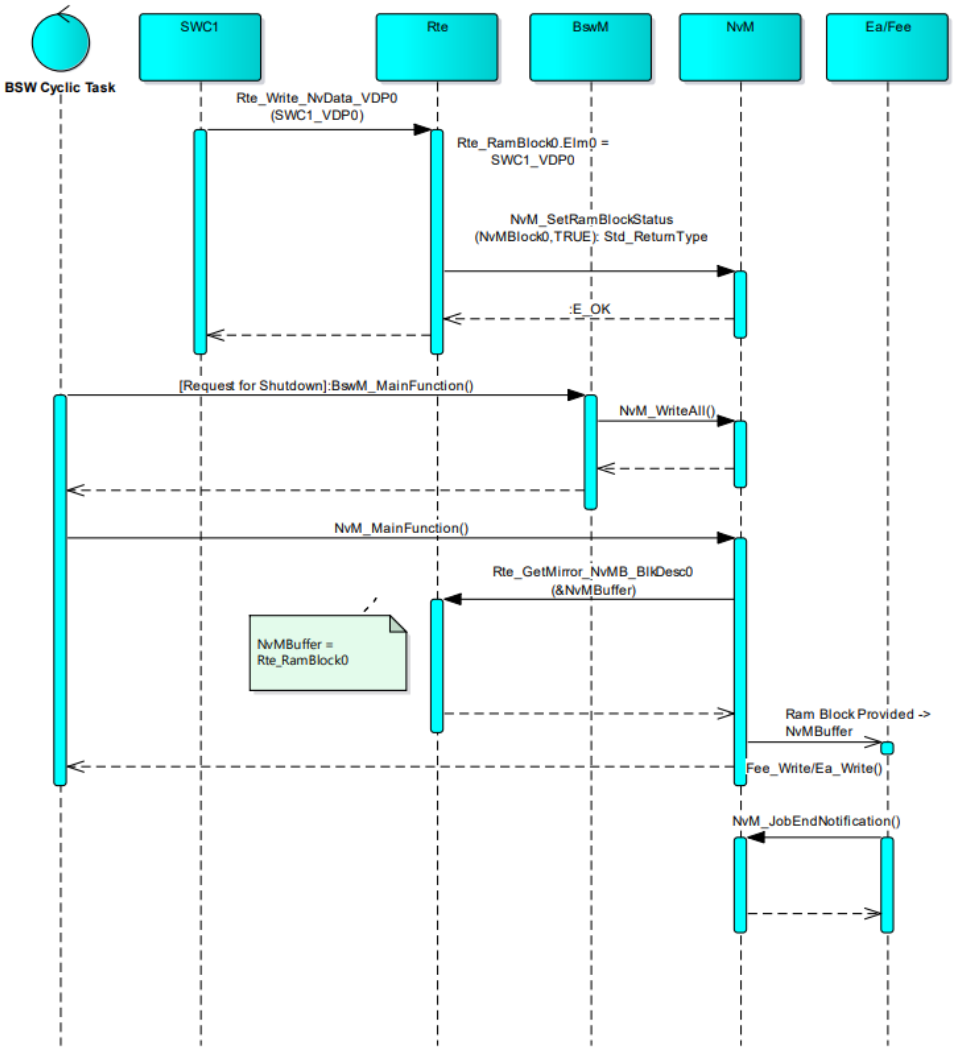
Write all Sequence



Read All Sequence

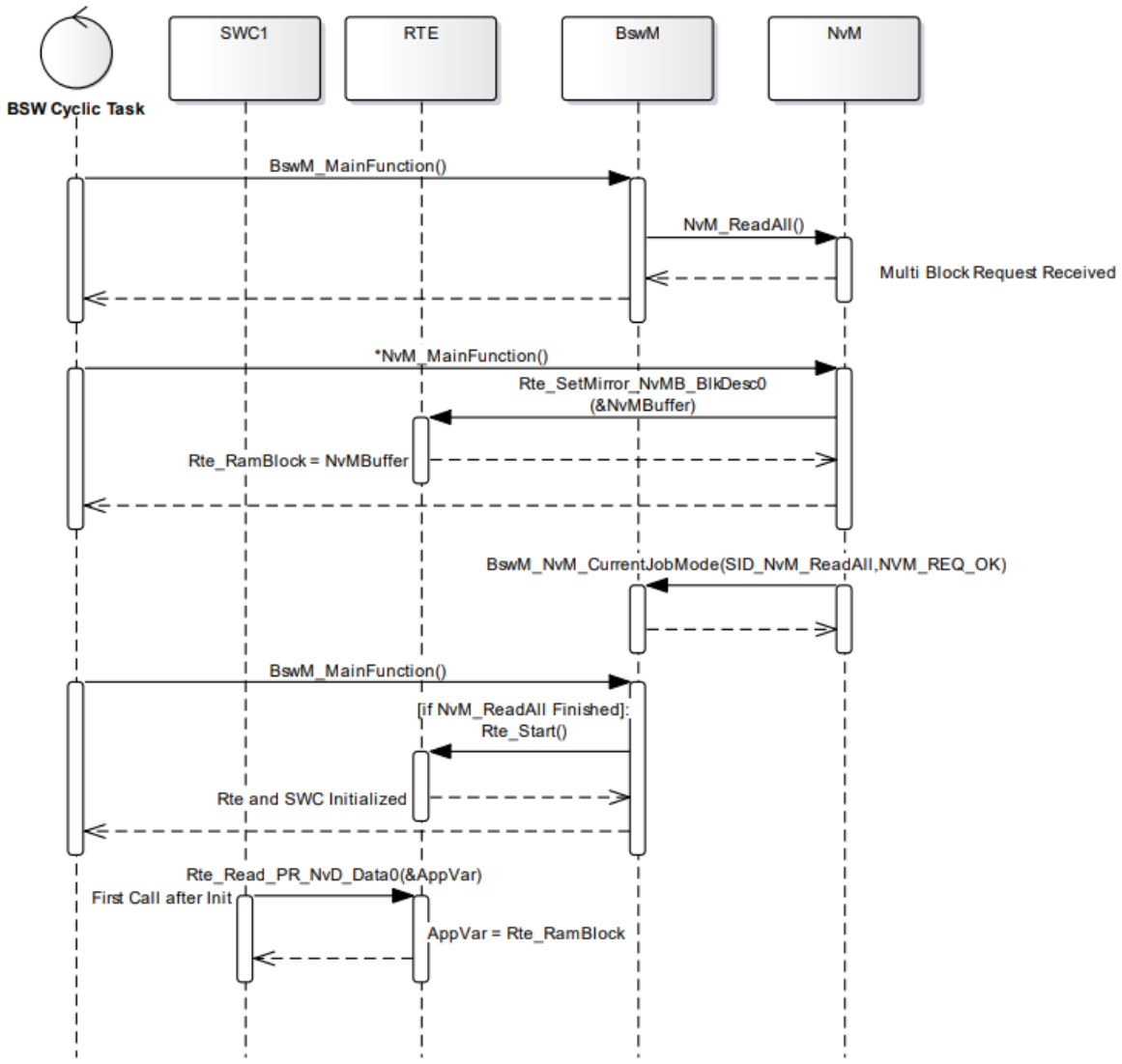


Figure 4: Sequence diagram for Initialization of RAM block