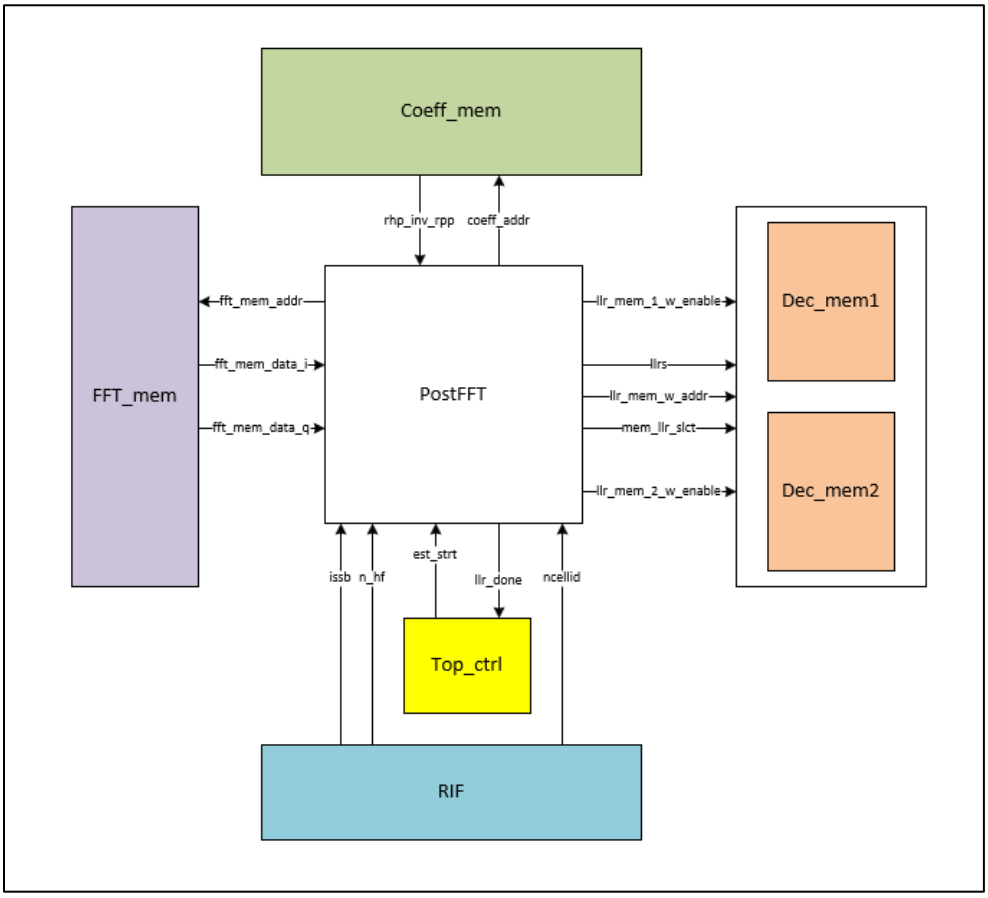
PostFFT Interfaces



Ports Description

Port Name	Port Direc.	Port Width	Active Low/ High	Port Description
issb	input	2	NA	The index of the SSB in the half frame. Range 0→3.
ncellid	input	10	NA	Cell identifier number. 0→1007.
n_hf	input	1	NA	0→ SSB in the first half in the frame. 1→ second half.
clk	input	1	NA	System clock = 61.44 MHz
rst	input	1	Low	Asynchronous reset.
fft_mem_addr	output	10	NA	The address of the data stored in the fft_mem. It may be DMRS or PBCH address (selected internally).

fft_mem_data_i	input	12	NA	The real part of the data stored in fft_mem. It may be DMRS or PBCH data (selected internally).
fft_mem_data_q	input	12	NA	The imaginary part. Same as above
llrs	output	8	NA	The channel LLRs stored in the dec_mem.
llr_mem_w_addr	output	6	NA	The address of the channel LLRs that will be stored in the dec_mem.
llr_mem_1_w_enable	output	1	High	Write Enable Level of the first decoder memory. Decoder has 2 memories each of width 32 bits and depth 64 bits.
llr_mem_2_w_enable	output	1	High	Write Enable Level of the second decoder memory.
mem_llr_slct	output	2	NA	Selects which part of the word in the decoder memory will be write into.
est_strt	input	1	High	Pulse allows postFFT to start.
llr_done	output	1	High	Pulse informs top_ctrl that all LLRs are stored in the dec_mem
coeff_addr	output	11	NA	Coefficients address which are needed for MMSE calculations.
rhp_inv_rpp	input	8*12	NA	This signal is the data comes from the coeff_mem to the MMSE.