RAM Verification Plan

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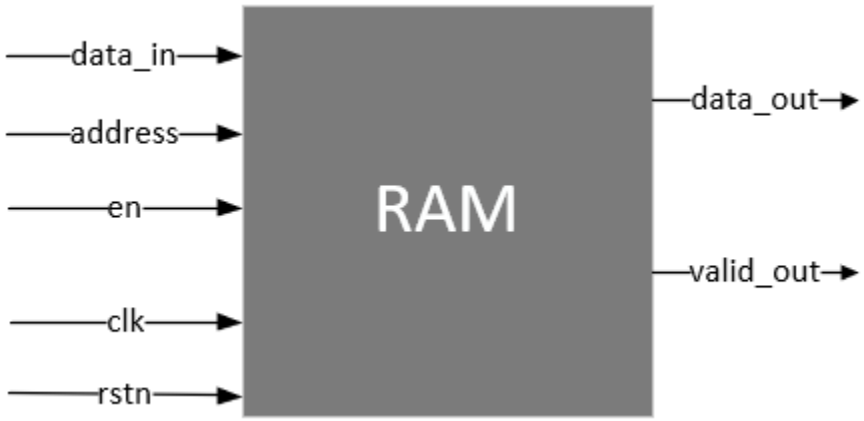
v1.1

1. Introduction

Overview:
This document outlines the verification process for Random-Access Memory (RAM) design. It describes the design functionality, verification strategy, test-cases, coverage results, and exit criteria.

2. Design Details

- **Description:** RAM is a synchronous single port memory block that supports read and write operations. It is used to store data based on a specified address.
- **IO Ports:**



Port Name	Direction	Width	Active	Description
clk	Input	1	NA	Clock signal
rstn	Input	1	Low	Asynchronous reset
data_in	Input	32	NA	Data to be written into the memory when en is high.
en	Input	1	High	Write enable. If high, data is written to RAM. If low, data is read out.
address	Input	4	NA	Address for both write and read operations.
data_out	Output	32	NA	Data read from the RAM when en is low.
valid_out	Output	1	High	Valid signal indicates data_out is valid and can be read.

- **Latency:**
  Write Operation: 0 clock cycle.
  Read Operation: 1 clock cycle.

3. Verification Strategy

- **Methodology:** UVM verification.

4. Exit Criteria

Metric	Target Value
Functional Coverage	100%
Code Coverage	100%
Number of bugs	0

5. Test Items

1. Reset behavior.
   - Verify all the outputs are zero when reset.
2. Write-Read.
3. Write-Read at the lowest address.
4. Write-Read at the highest address.
5. Back-to-Back Write-Read for Full Memory.
6. Back-to-Back Write-Write-Read for Full Memory.
7. Back-to-Back Write-Read-Read for Full Memory.
8. Write-Read all-zero pattern.
9. Write-Read all-one pattern.
10. Write-Read one-zero pattern.
11. Reset-Read to check data is unchanged.
12. Random writes, reads and resets until 100% functional coverage.

6. Test Case Table

Test Case ID	Feature Verified	Status
1	Reset behavior	Pass
2	Write operation	Pass
3	Write-Read at the lowest address	Pass
4	Write-Read at the highest address	Pass
5	Back-to-Back Write-Read	Pass
6	Back-to-Back Write-Write-Read	Pass
7	Back-to-Back Write-Read-Read	Pass
8	Write-Read all-zero pattern	Pass
9	Write-Read all-one pattern	Pass
10	Write-Read one-zero pattern	Pass

11	Reset-Read to check data is unchanged	Pass
12	Random writes, reads and resets	Pass

7. Traceability Matrix

Test Item	rst	en	addr	Data_in	Data_out	expected output
Reset behavior	✓	✗	✗	✗	✓	Data_out = 0
Write operation	✗	✓	✓	✓	✗	NA
Write-Read at the lowest address	✗	✓/✗	✓	✓	✓	Data_out = Data_in
Write-Read at the highest address	✗	✓/✗	✓	✓	✓	Data_out = Data_in
Back-to-Back Write-Read	✗	✓/✗	✓	✓	✓	Data_out = last Data_in
Back-to-Back Write-Write-Read	✗	✓	✓	✓	✓	Data_out = 2nd Data_in
Back-to-Back Write-Read-Read	✗	✓/✗	✓	✓	✓	repeated Data_out
Write-Read all-zero pattern	✗	✓/✗	✓	0	✓	Data_out = 0
Write-Read all-one pattern	✗	✓/✗	✓	all 1s	✓	Data_out = all 1s
Write-Read one-zero pattern	✗	✓/✗	✓	10101…	✓	Data_out = 10101...
Reset-Read to check data is unchanged	✓	✗	✓	✗	✓	Data_out = before reset

8. Coverage Results

Coverage Type	Percentage
Functional Coverage	100%
Code Coverage	100%

9. Open Issues

Bug ID	Description	Severity	Status	Owner
#1	NA	NA	NA	NA