مدينة زويل للعلوم والتكنولوچيا
Zewail City of Science and Technology

Nanotechnology and Nano-electronics Engineering Program Fall 2022

NANENG 501

Advanced Digital ASIC Design

Project Phase 2

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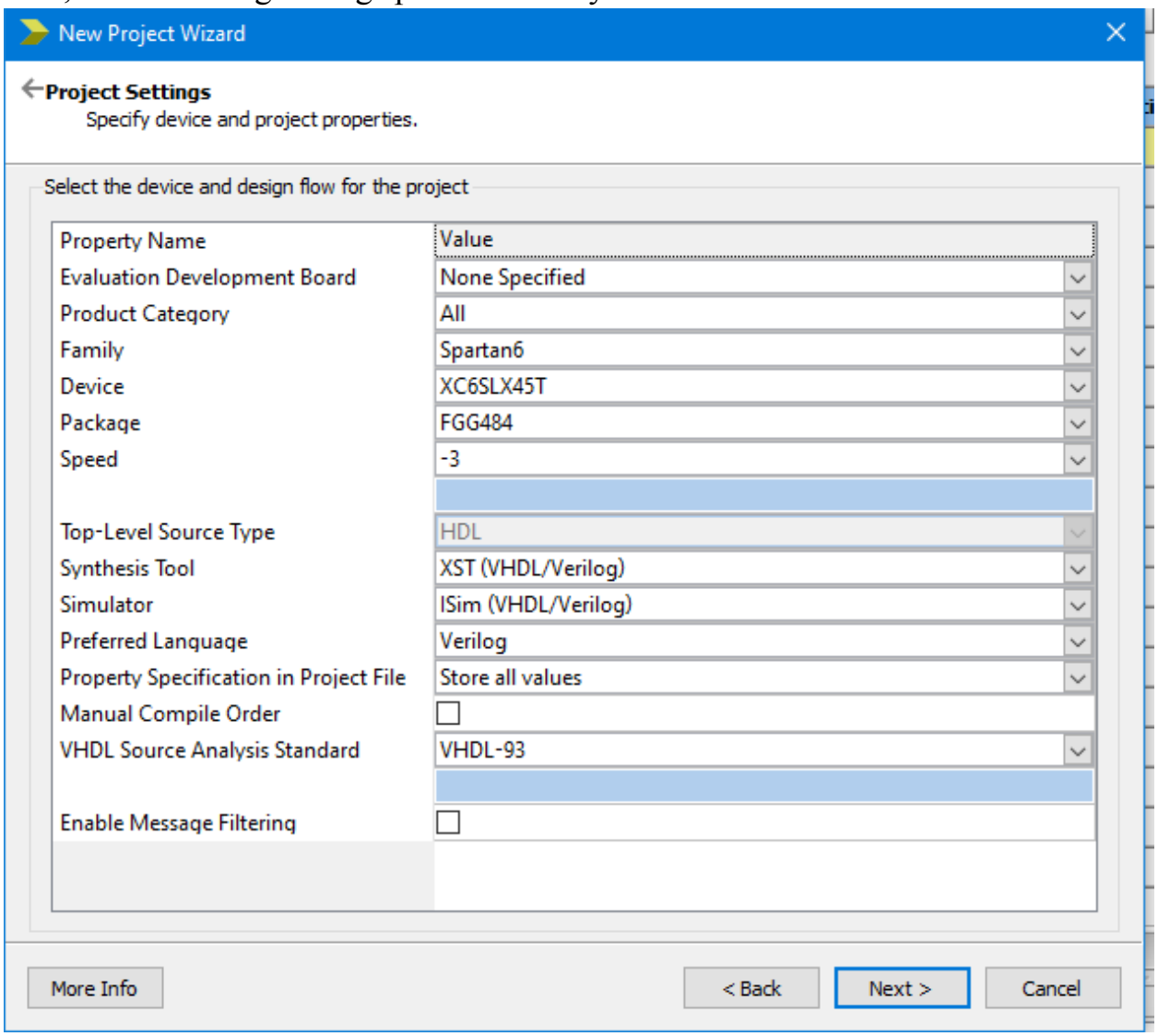
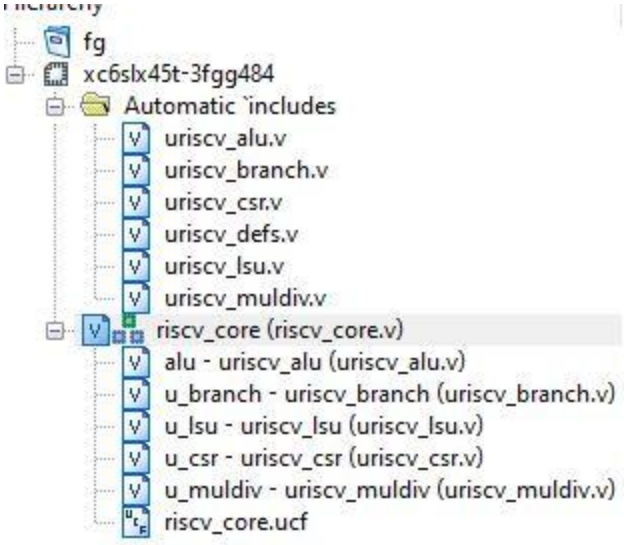
First, start the design using spartan 6 family: xc6slx45t kit



Then insert the design verilog files:



Setting the core as a top module and run the PFGA flow.
Adjust the clock period to be 20ns and using the regular 50% duty cycle condition.

Finish synthesis, flolrplaning and implementation with no errors:

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0, Component Switching Limit: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports	[-]

All constraints met.

The utaliztion is small due to relatively advanced kit:

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	478	54,576	1%	
Number used as Flip Flops	478			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	1,580	27,288	5%	
Number used as logic	1,533	27,288	5%	
Number using O6 output only	1,174			
Number using O5 output only	110			
Number using O5 and O6	249			
Number used as ROM	0			
Number used as Memory	44	6,408	1%	
Number used as Dual Port RAM	44			
Number using O6 output only	0			
Number using O5 output only	0			
Number using O5 and O6	44			
Number used as Single Port RAM	0			
Number used as Shift Register	0			
Number used exclusively as route-thrus	3			

The used clock is 20ns while the minimum clock allowed is around 16.5ns

```
---------------+---------+---------+---------+---------+
clk_i          |  16.481 |         |         |         |
---------------+---------+---------+---------+---------+


Timing summary:
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Timing errors: 0  Score: 0  (Setup/Max: 0, Hold: 0)

Constraints cover 4786477 paths, 0 nets, and 6312 connections

Design statistics:
   Minimum period:  16.481ns{1}   (Maximum frequency:  60.676MHz)


------------------------------------Footnotes-----------------------------------
1)  The minimum period statistic assumes all single cycle delays.

Analysis completed Tue Jan 10 22:34:36 2023
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Trace Settings:
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Trace Settings

Peak Memory Usage: 4667 MB
```

The power consumption is:

```
2.  Summary
2.1.  On-Chip Power Summary
--------------------------------------------------------------------------------
|                          On-Chip Power Summary                               |
--------------------------------------------------------------------------------
|        On-Chip        | Power (mW) |  Used  | Available | Utilization (%) |
--------------------------------------------------------------------------------
| Clocks                |       3.94 |      2 |    ---    |       ---       |
| Logic                 |       3.85 |   1580 |     27288 |               6 |
| Signals               |       6.31 |   2090 |    ---    |       ---       |
| IOs                   |      24.97 |    254 |       296 |              86 |
| DSPs                  |       0.00 |      4 |        58 |               7 |
| Quiescent             |      36.64 |        |           |                 |
| Total                 |      75.71 |        |           |                 |
--------------------------------------------------------------------------------
```

Comparison between the ASIC and FPGA flow:

ASIC	2.78 mW
FPGA	75.71 mW

ASIC is better for power consumption optimization.