M2 Integration circuits and systems

Cell Design For Digital Integrated Circuits

CD2IC PROJECT

TSPCFF D flip-flop Characterization

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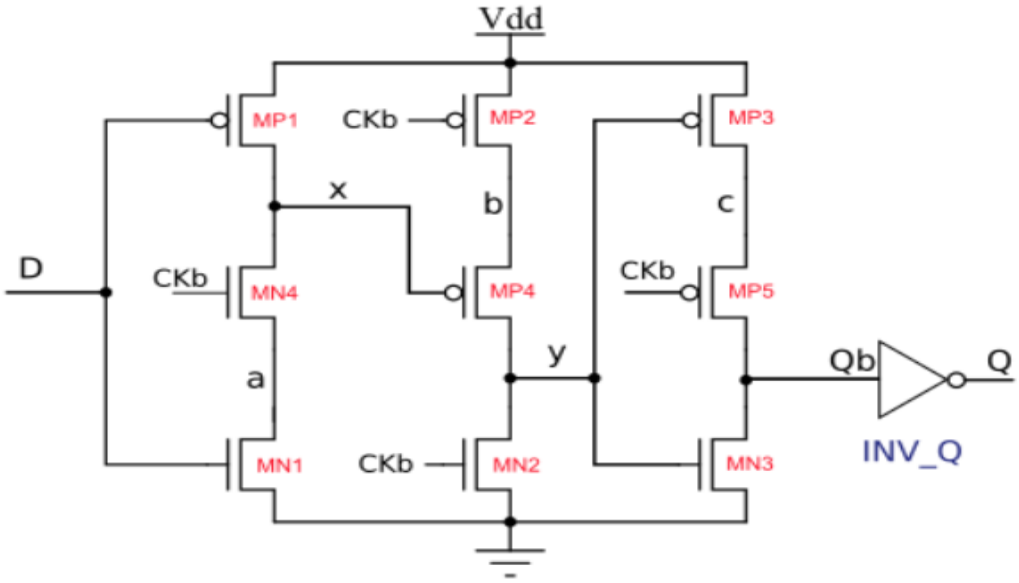
1- Cell Functionality :

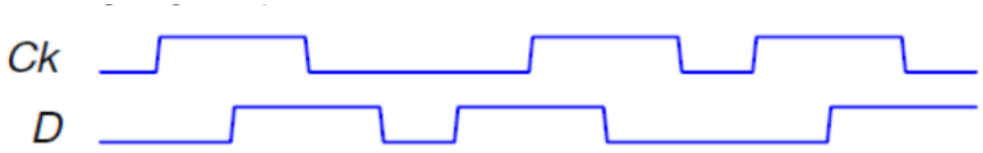
The true single-phase clock (TSPC) logic is based on designing basic circuit elements with only one phase of the clock, instead of the original designs that use the clock signal and its inverted value for master and slave operations in high and low clock value triggering. This results in a positive edge of the clock triggering a universal tick operation in the chip. The logic is helpful in optimizing the clock tree synthesis (CTS) during physical implementation by reducing the number of clock nets and ultimately reducing power consumption. Since it uses dynamic logic, it is fast.



The TSPC D flip-flop consists of three stages of logic as follows:

- **1st Stage:** A TSPC latch acting as the master, an inverter based on the dynamic logic family for high speed, triggered when the clock phase is low. It is a dynamic logic that pulls the master input to a low logic level during the low phase and pulls it to a high voltage depending on the input value.
- **2nd Stage:** An intermediate stage to capture the value and avoid phase transition issues. The stage has two MOSFETs controlled by the clock phase to enable data holding during specific phases. Since the MP4 is a PMOS driving logic high to y when x is low and open circuits the path when x is logic high, this requires inverting the resultant signal to get the Q output.
- **3rd Stage:** A TSPC latch acting as the slave, similar to the first stage, with a PMOS controlling the MOSFET to enable capturing the input during the high clock phase.

  For a more detailed analysis of the functionality of the flip-flop, we propose testing it with the given input waveforms:



-To apply circuit analysis assuming MOSFETs as ideal voltage-controlled switches, ignoring signal noise, clock skew, and clock jitter for simplicity:

It is triggered by the clock's positive edge, and Q follows the input D. This verifies the stage's functionality as discussed above.

C"	C	D	a	x	b	y	c	Q"	Q	P1	N1	N4	P2	P5	N2	N3	P4	P3
1	0	0	1	1	zu	0	1	zu	zu	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	ON
0	1	0	z1	1	1	z0	1	1	0	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
0	1	1	0	z1	1	z0	z1	z1	z0	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	ON
1	0	1	0	0	0	0	1	z1	z0	OFF	ON	ON	OFF	OFF	ON	OFF	ON	ON
1	0	0	1	1	z0	0	1	z1	z0	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	ON
1	0	1	0	0	0	0	1	z1	z0	OFF	ON	ON	OFF	OFF	ON	OFF	ON	ON
0	1	1	0	z0	1	1	0	0	1	OFF	ON	OFF	ON	ON	OFF	ON	ON	OFF
0	1	0	0	1	z1	0	1	z0	z1	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	ON
1	0	0	0	1	z1	0	1	z0	z1	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	ON
0	1	0	z0	1	1	z0	1	1	0	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON
0	1	1	0	z1	1	z0	1	1	0	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	ON
1	0	0	0	1	z1	0	1	z1	z0	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	ON

The design passes the functionality test and we can proceed to the Layout part.

2- Layout

Floorplaining: The constraint of the floorplan is the height of the standard cell. Since the global VDD and VSS routes and rails are distributed uniformly throughout the chip, the standard cells should be positioned in rows between successive rails to ensure an acceptable IR drop, usually around 2% of the VDD supply. The floorplan should feature a linear ordering, with a maximum of one PMOS and one NMOS in each column, minimizing connection congestion and hence the IR drop. Consideration for possible shared wells should be prioritized.

The MOSFETs are sized according to the given dimensions obtained from the analysis of the standard cell:

- **Clock Inverter**: widths are 145 nm for the NMOS and 215 nm for the PMOS, that is β of 1.47.
- **Q Inverter**: widths are 260 nm for the NMOS and 390 nm for the PMOS, that is β ratio of 1.5 which is, similar to the Clock Inverter, almost the square of r for that technology, around 2 to 3, thus minimizing the overall delay.

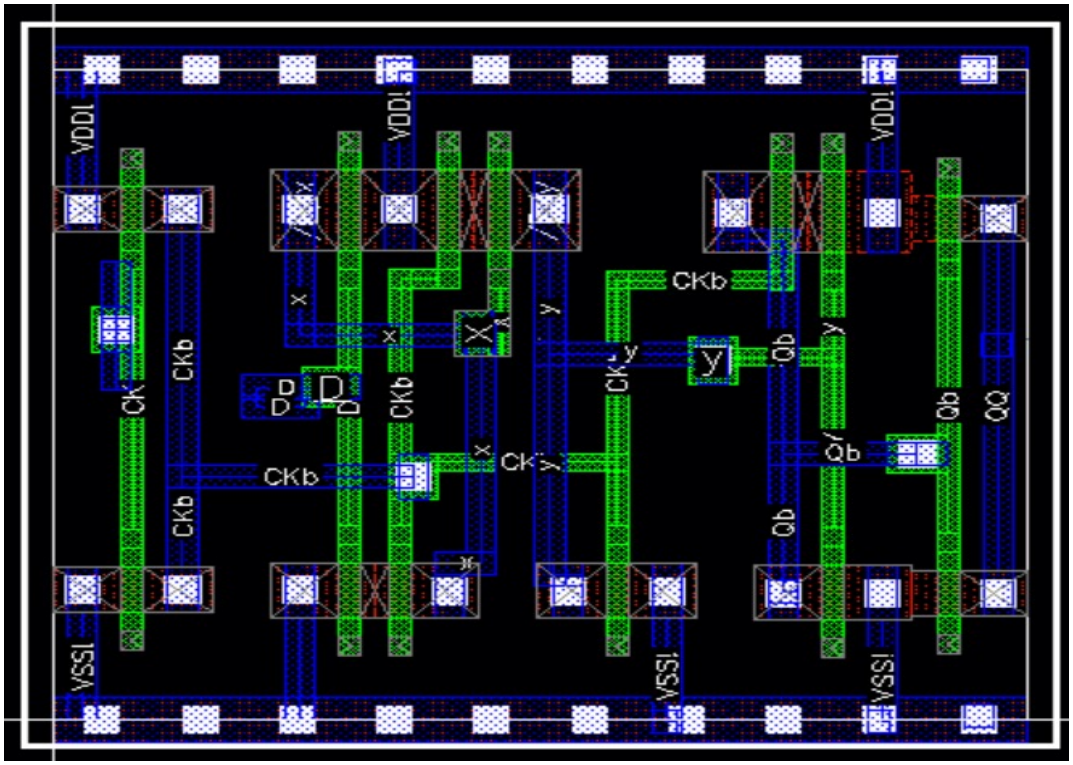
$$r = \frac{\mu_e}{\mu_h} \quad and \quad \beta = \frac{W_p}{W_n}$$

for the minimum average delay:

$$\frac{\partial t_p}{\partial \beta} = 0 \quad then \quad \beta_{opt} = \sqrt{r\left(1 + \frac{C_w}{C_{dn1} + C_{gn1}}\right)} \approx \sqrt{r}$$

– **Flip-Flop**: The NMOS is sized to 145 nm, which is a multiple of the minimum length, to drive a high current and thus ensure a fast response. The PMOS transistors are sized to 214 nm. It is essential to have a PMOS with a larger width to compensate for the difference in current that a PMOS can drive compared to the NMOS, due to its lower mobility, as the effective mass of holes is larger than the effective mass of electrons

The layout of 2μM width was implemented as follows:



It passes both design rule checks and layout versus schematic checks:

Match Statistics

Cell/Device	Total schematic	Total layout	Unmatched schematic	Unmatched layout
(g45n1svt) MOS	4	4	0	0
(g45p1svt) MOS	3	3	0	0
(g45n1svt:SerMos2#1) MosBlk	1	1	0	0
(g45p1svt:SerMos2#1) MosBlk	2	2	0	0
Total	10	10	0	0
Match Statistics for Nets	9	9	0	0

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Proposed enhancements:

- implementing the clock's inverter in the middle of the cell so the inverted clock signal experiences less polysilicon resistance.
- usage of higher metals such as M2 for it is low resistance so it would enhance the delay which is proportional to RC product
- It is recommended by the fab to use each metal either horizontally or vertically not a mix of both directions to avoid crosstalk added resistance and improve yield and less post-layout parasitics.
- A matching between up and down MOSFETs can be enhanced by forcing more symmetrical connections.
- moving Mosfets controlled by the clock signal closer to each other to ensure no clock skewing due to different path lengths resulting in different delays.
- moving the input pin to the edge of the cell to enhance compatibility for physical implementation tools.
- For a more reliable design, a minimum metal width is to be increased to ensure resisting electromigration over time.

3- Characterization

Inverter

Propagation time: Fall and Rise

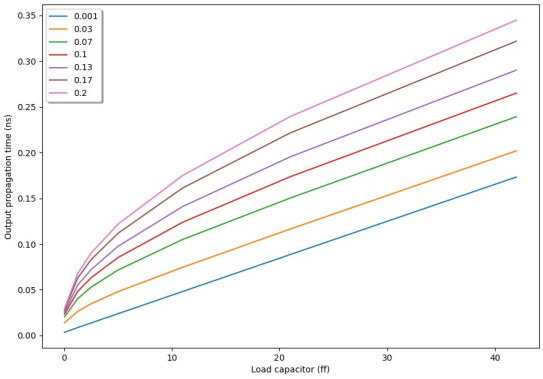


Figure 1: Rise Propgation

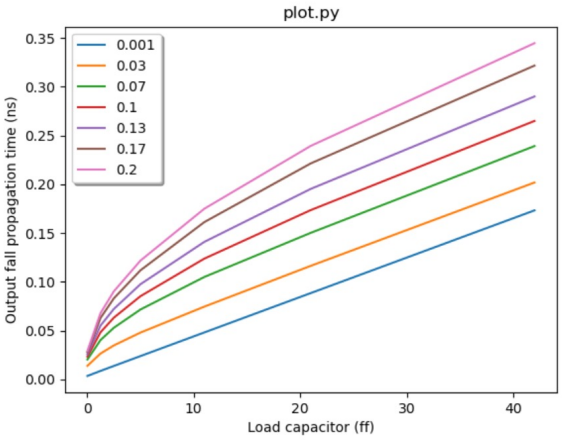


Figure 2: Fall Propgation

Increasing the load capacitance increases the propagation time for both fall and rise transitions.

load capacitance:

The increase in load capacitance at the output of the inverter increases the output propagation time.

TSPCFF

Propagation Time of TSPCFF

- Rise

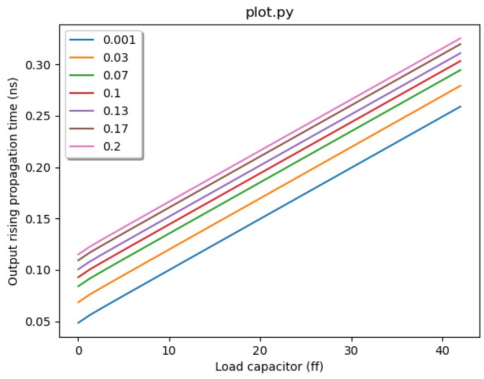


Figure 3: Propagation time increases with increased load

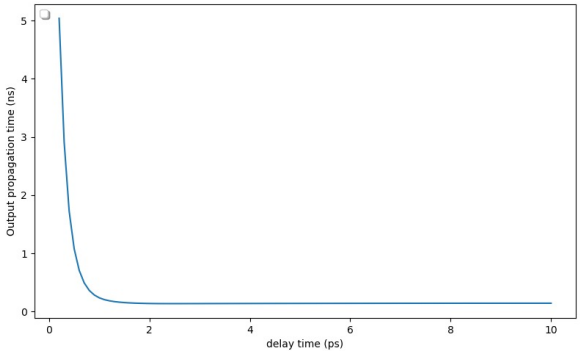


Figure 4: Increasing delay time reduces propagation of the output

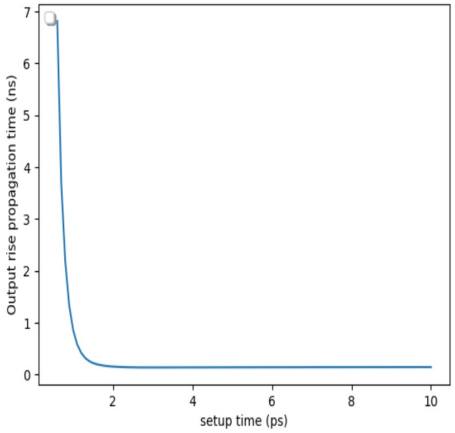


Figure 5: Propgation time decreases when increasing Setup time

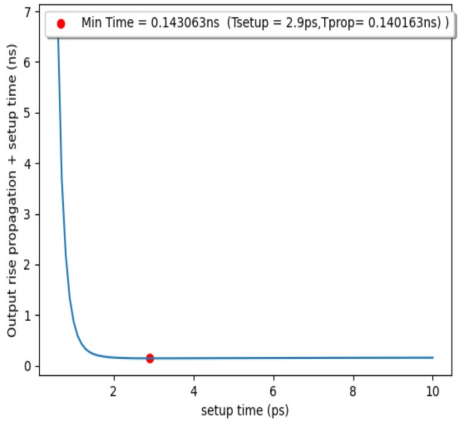


Figure 6: an optimum point occurs at Tsetup = 2.9 ps

- Fall

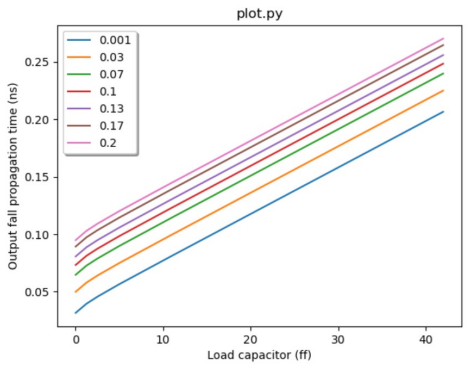


Figure 7: Propagation time increases with increased load

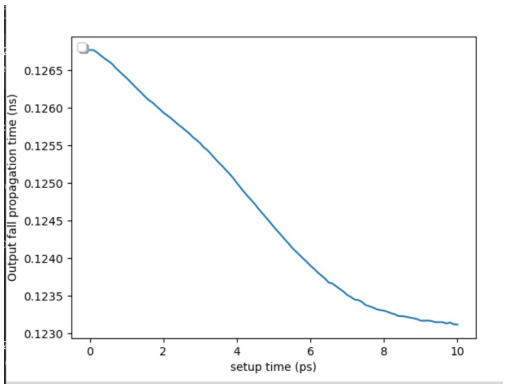
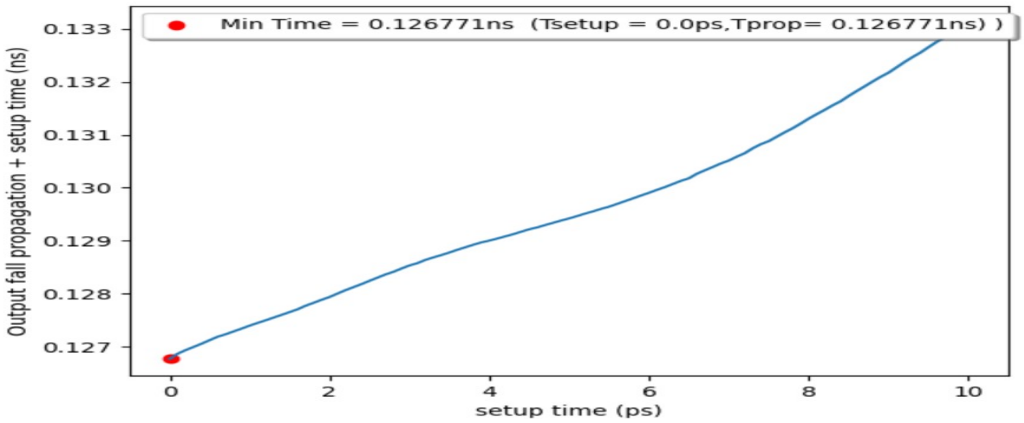


Figure 8: Increasing delay time reduces propagation of the output



an optimum point occurs at Tsetup = 0 ps The setup + Propagation are crucial as it controls the operating frequency of the Flip-Flop

4- Hold Time

The hold time is the time input that must be maintained staple after the clock edge. The hold time of the TSPCFF circuit can be calculated to be the time needed for the slave, the first stage, to capture the signal and send it to the intermediate, the second, stage. In that sense, the hold time of the TSPCFF can be seen as the propagation time of the first stage, until its output, net x, propagates when the D input changes.

Testbench updates

- Assign the output signal to be the x net instead of the Q net
- adjust the code to behave in the mode of calculating the propagation time.
- change the clock from zero to one to get a rising edge.
- Force the input D value to change.
- Calculate the time until the output x Fall/rise.