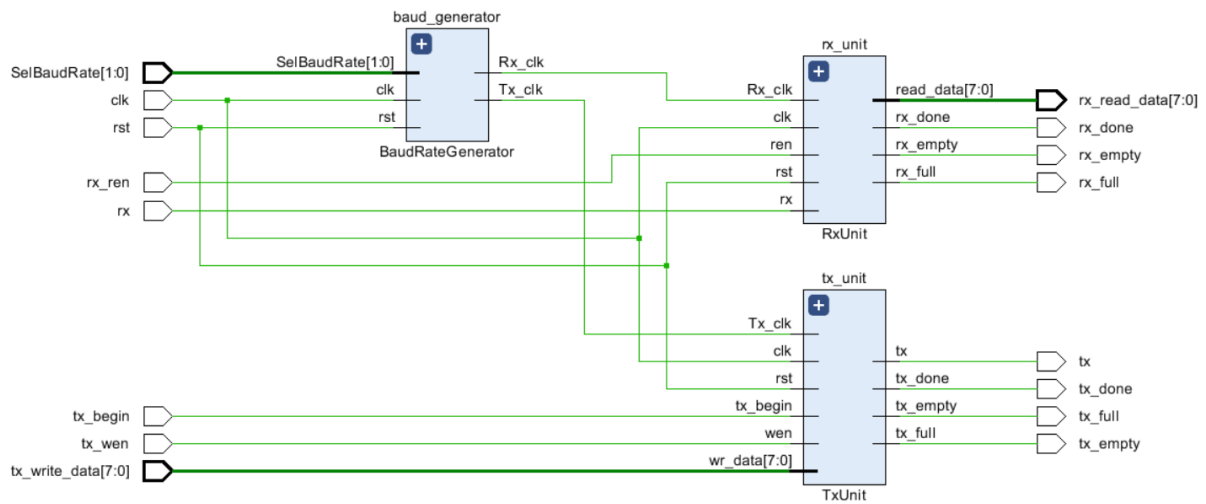
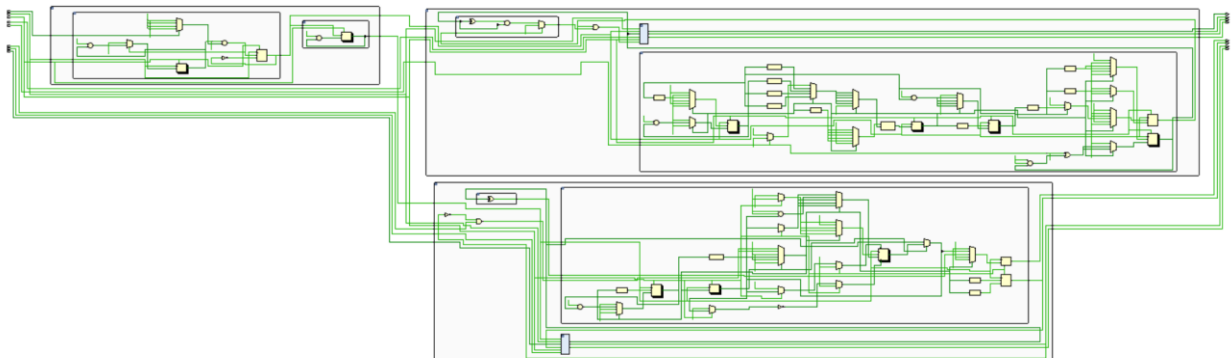


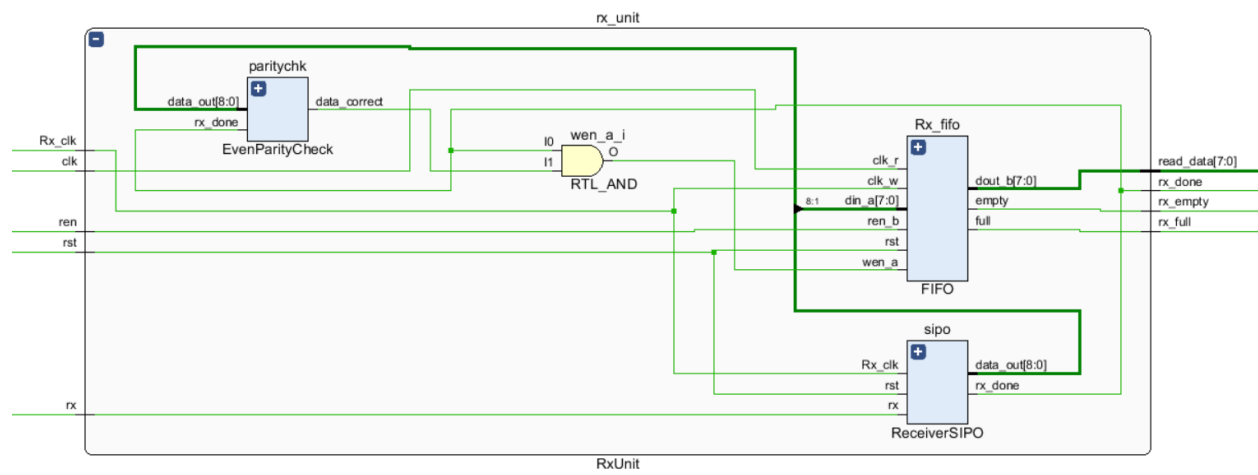
Elaboration schematic_1



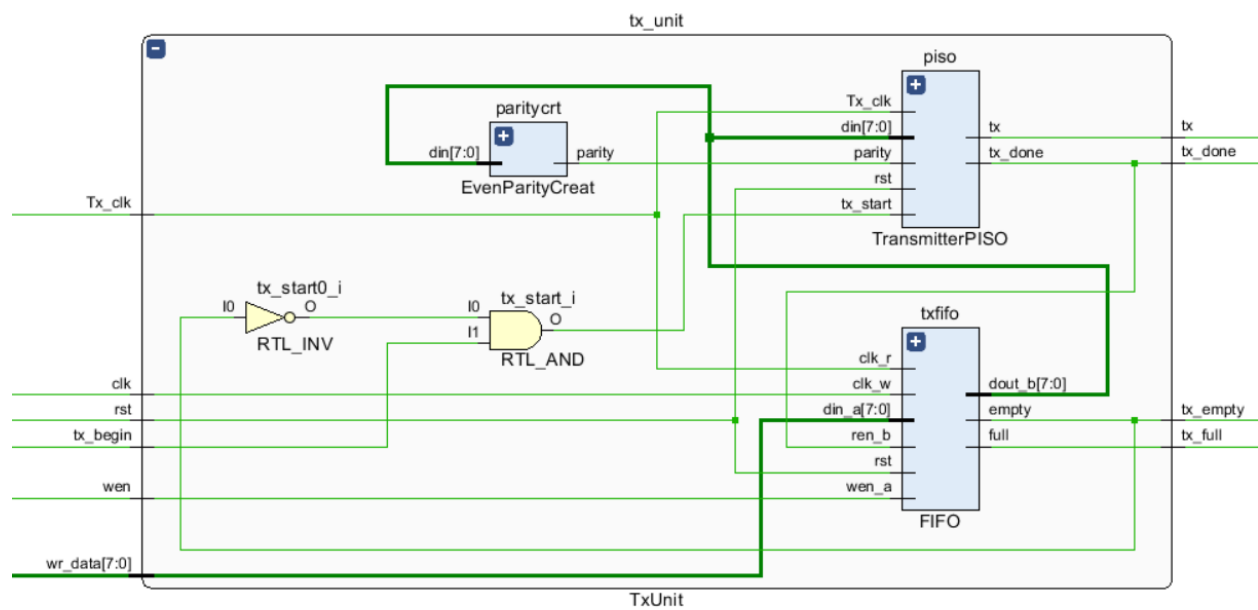
Elaboration schematic_2



rx_unit



tx_unit



The diagram illustrates the internal structure of a 16-bit parallel adder, specifically focusing on the ALU (Arithmetic Logic Unit) components. It shows two 8-bit ALU chips (74LS181) connected to form a 16-bit adder. The inputs include two 16-bit numbers (A and B) and a carry-in. The outputs are a 16-bit sum and a carry-out. The diagram is color-coded with green for data paths and blue for control paths.

Inputs:

- in_0[15:0]**: 16-bit input A
- in_1[15:0]**: 16-bit input B
- in_carryin[0]**: Carry-in

Internal Components:

- 8-bit ALU Chips (74LS181)**: Two chips are used to perform the addition. The first chip handles the lower 8 bits, and the second chip handles the upper 8 bits, taking the carry-out of the first chip as its carry-in.
- Multiplexers (MUX)**: Used to select between different operations (addition, subtraction, etc.) based on control signals.
- Carry Logic**: The carry-out of the first 8-bit ALU is connected to the carry-in of the second 8-bit ALU.

Outputs:

- out_0[15:0]**: 16-bit sum output
- out_carryout[0]**: Carry-out

| Setup | Hold | Pulse Width |
|---------------------------------------|----------------------------------|---|
| Worst Negative Slack (WNS): 15.593 ns | Worst Hold Slack (WHS): 0.148 ns | Worst Pulse Width Slack (WPWS): 9.500 ns |
| Total Negative Slack (TNS): 0.000 ns | Total Hold Slack (THS): 0.000 ns | Total Pulse Width Negative Slack (TPWS): 0.000 ns |
| Number of Failing Endpoints: 0 | Number of Failing Endpoints: 0 | Number of Failing Endpoints: 0 |
| Total Number of Endpoints: 60 | Total Number of Endpoints: 60 | Total Number of Endpoints: 38 |

All user specified timing constraints are met.