

# System

You have to go through the digital backend flow including: -

- Synthesis
- Formality post-synthesis
- DFT
- Formality post-dft

Steps: -

1. Create **Projects** folder inside IC directory
2. Copy **System** folder from your computer into the virtual machine inside **Projects** folder
  - Synthesis Stage: -
    - i. Add the following constraints in **cons.tcl** file.
      - Create your master clocks
        - REF\_CLK (50 MHz)
        - UART\_CLK (3.686 MHz)
      - Create your generated clocks
        - ALU\_CLK (master\_clk = REF\_CLK , div\_ratio = 1)
        - RX\_CLK (master\_clk = UART\_CLK , div\_ratio = 1)
        - TX\_CLK (master\_clk = UART\_CLK , div\_ratio = 32)
      - Create a clock uncertainty with 0.2 ns for setup (master & generated clocks)
      - Create a clock uncertainty with 0.1 ns for hold (master & generated clocks)
      - Create a clock transition with 0.05 ns for all master clocks
      - Set\_dont\_touch on all the master and generated clocks
      - Clock Grouping
      - Input delays on all input ports except (CLK & RST) with 20% clock period
      - output delays on all output ports with 20% clock period
      - Add Buffer driving cell for all input ports except (CLK & RST)
      - Add load of 0.1 pf on all output ports
      - Set operation condition using slow and fast libraries
    - ii. Run synthesis and check the followings
      - No Errors, loops and latches in syn.log file
      - Check Setup timing analysis report for Violating paths
      - Check Hold timing analysis report for Violating paths
  - Formality post-synthesis Stage: -
    - i. Run Formality and check it is succeeded with no failing points

- DFT Stage: -

- i. Define a new file with name **SYS\_TOP\_dft.v** inside SYS\_TOP folder

- ii. Do the rtl preparation in **SYS\_TOP\_dft.v** including:-

- 1. Adding scan ports with the exact names as shown: -

```
module SYS_TOP # ( parameter DATA_WIDTH = 8 , RF_ADDR = 4 , NUM_OF_CHAINS = 3)
(
  input  wire          scan_clk ,
  input  wire          scan_rst ,
  input  wire          test_mode ,
  input  wire          SE ,
  input  wire [NUM_OF_CHAINS-1:0] SI ,
  output wire [NUM_OF_CHAINS-1:0] SO ,
  input  wire          RST_N,
  input  wire          UART_CLK,
  input  wire          REF_CLK,
  input  wire          UART_RX_IN,
  output wire          UART_TX_O,
  output wire          parity_error,
  output wire          framing_error
);
```

- 2. adding Muxs on clocks and resets ports

- iii. Add the following constraints inside the **cons.tcl**

- 1. Add scan clock constraint using create\_clock
        - 2. Add SCAN\_CLK group in clock grouping command
        - 3. Input delays on scan input ports (SI,SE) with 20% clock period
        - 4. output delays on scan output ports (SO) with 20% clock period
        - 5. Add Buffer driving cell on scan input ports (SI,SE)
        - 6. Add load of 0.1 pf on scan output ports (SO)
        - 7. Add set\_case\_analysis 1 [get\_port test\_mode] command to run timing analysis using scan clock

- iv. Add all the dft sections: -

- 1. Archirecture Scan Chains
        - 2. Define DFT Signals
        - 3. Create Test Protocol
        - 4. Pre-DFT Design Rule Checking
        - 5. Preview DFT
        - 6. Insert DFT
        - 7. Design Rule Checking post dft insertion

- v. Run dft and check the followings

- No Errors, loops and latches in dft.log file
          - Check Setup timing analysis report for Violating paths
          - Check Hold timing analysis report for Violating paths
          - Check dft coverage > 98 %

- Formality post-dft Stage: -

- i. Run Formality and check it is succeeded with no failing points