Abdelrahman Ahmed Esmat

Electronics and Communication Engineering Student

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Military Status: Exemption | Cairo, Egypt

Summary

Electronics engineering student with hands-on experience in RTL and FPGA design, actively pursuing advanced ASIC training and continuously working to improve.

Education

Helwan University — Cairo, Egypt
B.Sc. in Electronics and Communications Engineering
Graduation Year: 2026
Cumulative Grade: 71.65 % (Good)

Training and Courses

- **Digital Design Using FPGA | National Telecommunication Institute (NTI)** (August 2025 – ongoing)

  Content: -

  - State-of-the-Art Programmable Logic and FPGA Technology
  - FPGA vs. ASIC Designs
  - Digital Design Techniques
  - Static Timing Analysis
  - Efficient RTL Coding using VHDL and Verilog Language
  - Building Advanced Self-checking Verilog testbench
  - Finite State Machines
  - Attributes, functions, and procedures
  - RTL Synthesis on Xilinx ISE and Vivado

  Final Project: I2C Master (Verilog) **| 8-bit Microprocessor** (VHDL)

- **Digital IC Design Diploma** (Under supervision of **Eng.** Ali El Temsah) (July 2025 – Ongoing)

  Content: -

  - Efficient RTL Coding Using Verilog language
  - Building Advanced Self-checking Verilog Test-bench
  - TCL Scripting Language
  - Static Timing Analysis
  - Low Power Design Techniques
  - Clock Domain Crossing
  - RTL Synthesis on Design Compiler
  - Design For Testing (DFT) Insertion
  - Formal Verification Post-Synthesis & Post-DFT & Post-PnR
  - ASIC Flow including (Floorplanning, Pin Placement, Clock Tree Synthesis,
  - Placement, Routing, Timing Closure, Chip Finishing, Sign Off)
  - Post-Layout Verification (Gate Level Simulation)

  Final Project: "RTL to GDS Implementation of Low Power Configurable Multi Clock Digital System"

Description: It is responsible of receiving commands through UART receiver to do different system functions as register file reading/writing or doing some processing using ALU block and send result to UART transmitter through asynchronous FIFO for handling different clock rates and avoid data loss.

Project phases: -

- RTL Design from Scratch of system blocks (ALU, Register File, Synchronous FIFO, Integer Clock Divider, Clock Gating, Synchronizers, Main Controller, UART TX, UART RX).
- Integrate and verify functionality through self-checking testbench.
- Constraining the system using synthesis TCL scripts.
- Synthesize and optimize the design using design compiler tool.
- Analyze Timing paths and fix setup and hold violations.
- Verify Functionality equivalence using Formality tool
- Physical implementation of the system passing through ASIC flow phases and generate the GDS File.
- Verify functionality post-layout considering the actual delays.

➢ **FPGA Prototyping Summer Trainee | Electronics Research Institute (ERI)** (July 2024 – August 2024)

FPGA Prototyping with Practical Implementation Using VHDL and Xilinx Design Tools

- Introduction to Digital Design, FPGA, and VHDL
- Built and tested VHDL modules for FPGA-based designs
- Structural Design using "Component" – Generate Statement
- Implementation of ALU on FPGA
- Test Benches - Generic Statement - Arrays
- Implementation of Finite State Machine

Final Project: VERIRISC CPU – RISC-based CPU on FPGA

Projects

- **RTL to GDS Implementation of Low Power Configurable Multi Clock Digital System** (Ongoing)
- **Clock divider**
- **FIFO**
- **UART TX \RX**
- **I2C Master**
- **CRC**
- **VERIRISC CPU – RISC-based CPU on FPGA**
- **8-bit Microprocessor**
- **16-bit ALU**

Skills

Technical:
- Verilog / VHDL / SystemVerilog
- Modelsim /Questasim / Xilinx ISE/ Vivado
- Design Compiler / Formality (Synopsys Tools)
- MATLAB
- TCL / C++
- Protues

Non-Technical:
- Self-Learning Skills
- Communication Skills
- Active Listening
- Mindfulness
- Problem Solving
- Team-Work Skills
- Leadership
- Microsoft Office
- Adaptability
- Time Management

Languages:
- Arabic: (Native)
- English: (B1)