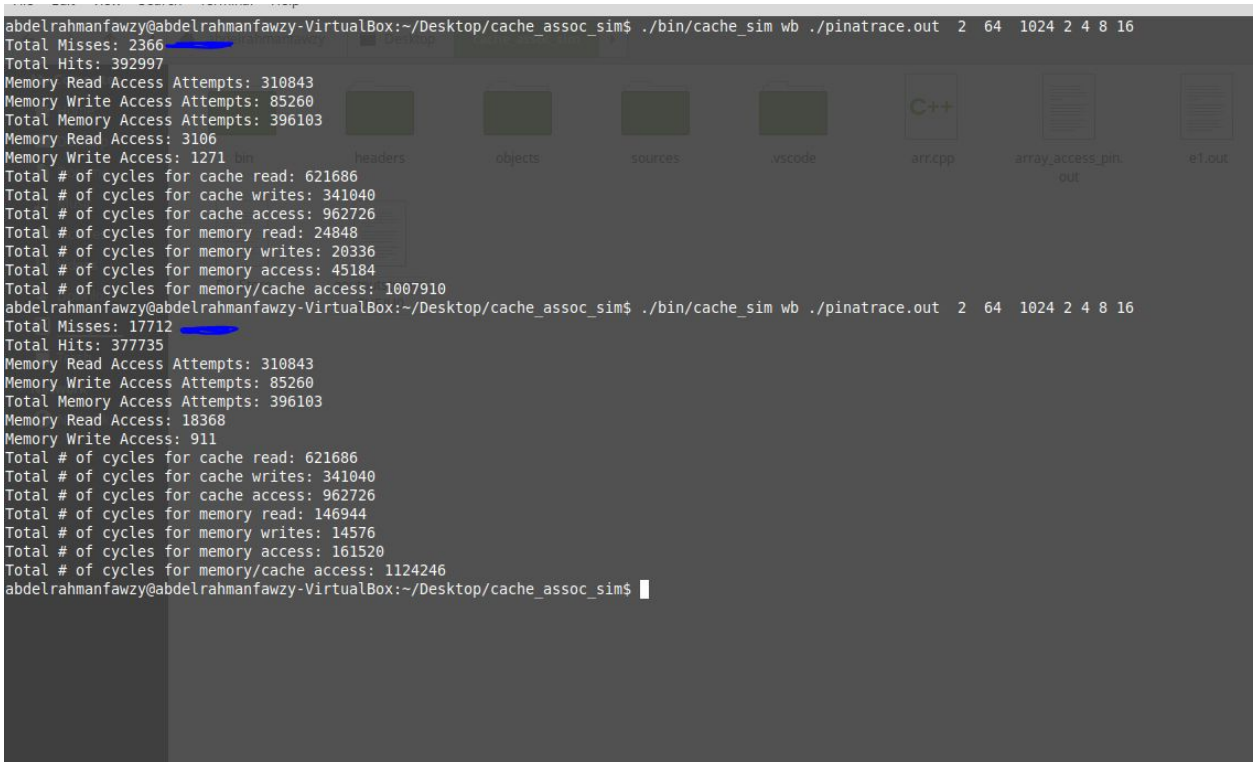
Report

In this assignment, I am working on simulating a set-associative cache with its two writing modes write back and write through, and using the aging algorithm for addresses' replacement. This simulation should read tons of addresses that represent a specific piece of code and return, the number of hits and misses, number of memory reads and writes, number of cache reads and writes, and all of their cycles.

In this report, I am going to compare the situation of cache and how it works in different cases:
1-Comparing how effective it is by respecting the spatial locality and how it is not while we don't.
2- Comparing different Cache Sizes
3- Comparing Different Block Sizes

1-Comparing how effective it is by respecting the spatial locality and how it is not while we don't.
In this comparison I want to see how respecting the spatial locality in accessing arrays row by row for example is cache-friendly causing it to avoid a bulk of misses and have a better performance, while not respecting it by accessing the arrays column by column result in cache thrashing with a very big number of misses as shown.



2- Comparing the different cache sizes:

As the cache size increases, the number of indexes that are available for the addresses to be assigned to also increases which effectively reduce the number of misses and consequently a better performance.

It is shown below cases of using different cache sizes.

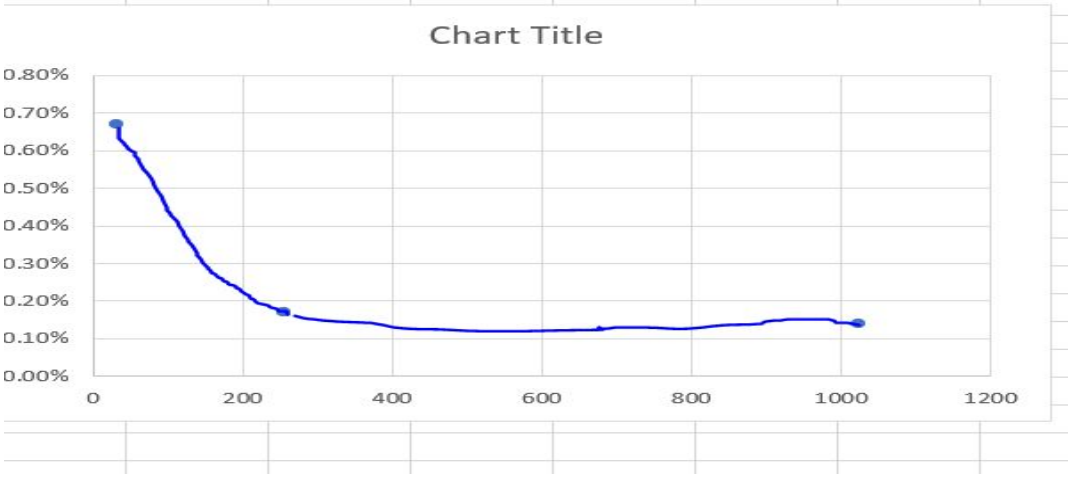
```
abdelrahmanfawzy@abdelrahmanfawzy-VirtualBox:~/Desktop/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out  4  256 1024 2 4 8 16
Total Misses: 684
Total Hits: 394934
Memory Read Access Attempts: 310843
Memory Write Access Attempts: 85260
Total Memory Access Attempts: 396103
Memory Read Access: 1169
Memory Write Access: 69
Total # of cycles for cache read: 621686
Total # of cycles for cache writes: 341040
Total # of cycles for cache access: 962726
Total # of cycles for memory read: 9352
Total # of cycles for memory writes: 1104
Total # of cycles for memory access: 10456
Total # of cycles for memory/cache access: 973182
abdelrahmanfawzy@abdelrahmanfawzy-VirtualBox:~/Desktop/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out  4  32 1024 2 4 8 16
Total Misses: 2648
Total Hits: 392828
Memory Read Access Attempts: 310843
Memory Write Access Attempts: 85260
Total Memory Access Attempts: 396103
Memory Read Access: 3275
Memory Write Access: 806
Total # of cycles for cache read: 621686
Total # of cycles for cache writes: 341040
Total # of cycles for cache access: 962726
Total # of cycles for memory read: 26200
Total # of cycles for memory writes: 12896
Total # of cycles for memory access: 39096
Total # of cycles for memory/cache access: 1001822
abdelrahmanfawzy@abdelrahmanfawzy-VirtualBox:~/Desktop/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out  4  1024 1024 2 4 8 16
Total Misses: 542
Total Hits: 395068
Memory Read Access Attempts: 310843
Memory Write Access Attempts: 85260
Total Memory Access Attempts: 396103
Memory Read Access: 1035
Memory Write Access: 0
Total # of cycles for cache read: 621686
Total # of cycles for cache writes: 341040
Total # of cycles for cache access: 962726
Total # of cycles for memory read: 8280
Total # of cycles for memory writes: 0
Total # of cycles for memory access: 8280
Total # of cycles for memory/cache access: 971006
abdelrahmanfawzy@abdelrahmanfawzy-VirtualBox:~/Desktop/cache_assoc_sim$
```

Calculating the miss rate for the three conditions and making the graph:

Cach size	Miss Rate
32	0.67%
256	0.17%
1024	0.14

It appears how big the cache size is gives less miss rate.

32	0.67%
256	0.17%
1024	0.14%



3- Comparing Different Block Sizes:

By increasing the block size of the cache for the spatial and sequential localities, the cache will have a high miss penalty for replacement; copying more data from DRAM upon misses However, it has relatively less Miss Rate..

Calculating the miss rate for the three conditions and making the graph:

blocksize	**Miss Rate**
64	**1.3%**
256	**0.6%**
2048	**0.09%**

```
abdelrahmanfawzy@abdelrahmanfawzy-VirtualBox:~/Desktop/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out  4  256 64 2 4 8 16
Total Misses: 5053
Total Hits: 387858
Memory Read Access Attempts: 310843
Memory Write Access Attempts: 85260
Total Memory Access Attempts: 396103
Memory Read Access: 8245
Memory Write Access: 3095
Total # of cycles for cache read: 621686
Total # of cycles for cache writes: 341040
Total # of cycles for cache access: 962726
Total # of cycles for memory read: 65960
Total # of cycles for memory writes: 49520
Total # of cycles for memory access: 115480
Total # of cycles for memory/cache access: 1078206
abdelrahmanfawzy@abdelrahmanfawzy-VirtualBox:~/Desktop/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out  4  256 256 2 4 8 16
Total Misses: 2353
Total Hits: 392550
Memory Read Access Attempts: 310843
Memory Write Access Attempts: 85260
Total Memory Access Attempts: 396103
Memory Read Access: 3553
Memory Write Access: 938
Total # of cycles for cache read: 621686
Total # of cycles for cache writes: 341040
Total # of cycles for cache access: 962726
Total # of cycles for memory read: 28424
Total # of cycles for memory writes: 15008
Total # of cycles for memory access: 43432
Total # of cycles for memory/cache access: 1006158
abdelrahmanfawzy@abdelrahmanfawzy-VirtualBox:~/Desktop/cache_assoc_sim$ ./bin/cache_sim wb ./pinatrace.out  4  256 2048 2 4 8 16
Total Misses: 357
Total Hits: 395489
Memory Read Access Attempts: 310843
Memory Write Access Attempts: 85260
Total Memory Access Attempts: 396103
Memory Read Access: 614
Memory Write Access: 30
Total # of cycles for cache read: 621686
Total # of cycles for cache writes: 341040
Total # of cycles for cache access: 962726
Total # of cycles for memory read: 4912
Total # of cycles for memory writes: 480
Total # of cycles for memory access: 5392
Total # of cycles for memory/cache access: 968118
abdelrahmanfawzy@abdelrahmanfawzy-VirtualBox:~/Desktop/cache_assoc_sim$
```

64	1.30%
256	0.60%
2048	0.09%