Analog Integrated Systems Design

Lecture 10
Digital-to-Analog Conversion (2)

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DAC Architectures

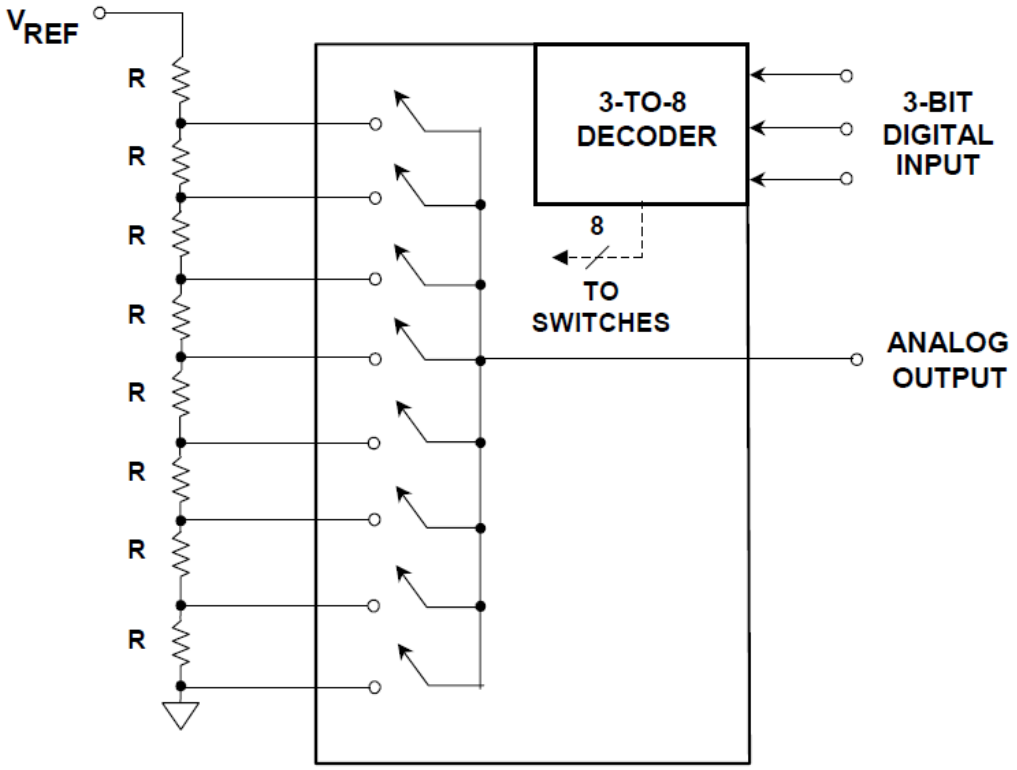
	Unary	Binary
Voltage	Resistor string *Flash ADC*	R-2R *Low-performance DAC*
Current	Current matrix	Current splitting
	High bandwidth DAC	
Charge/capacitor	Capacitor bank *Low power DAC*	Capacitor bank
Time	PWM, ΣΔ mod *Low bandwidth DAC*	Limited by distortion

In italic the main application area is indicated

[M. Pelgrom, 2017]

Resistor String (Ladder) DAC

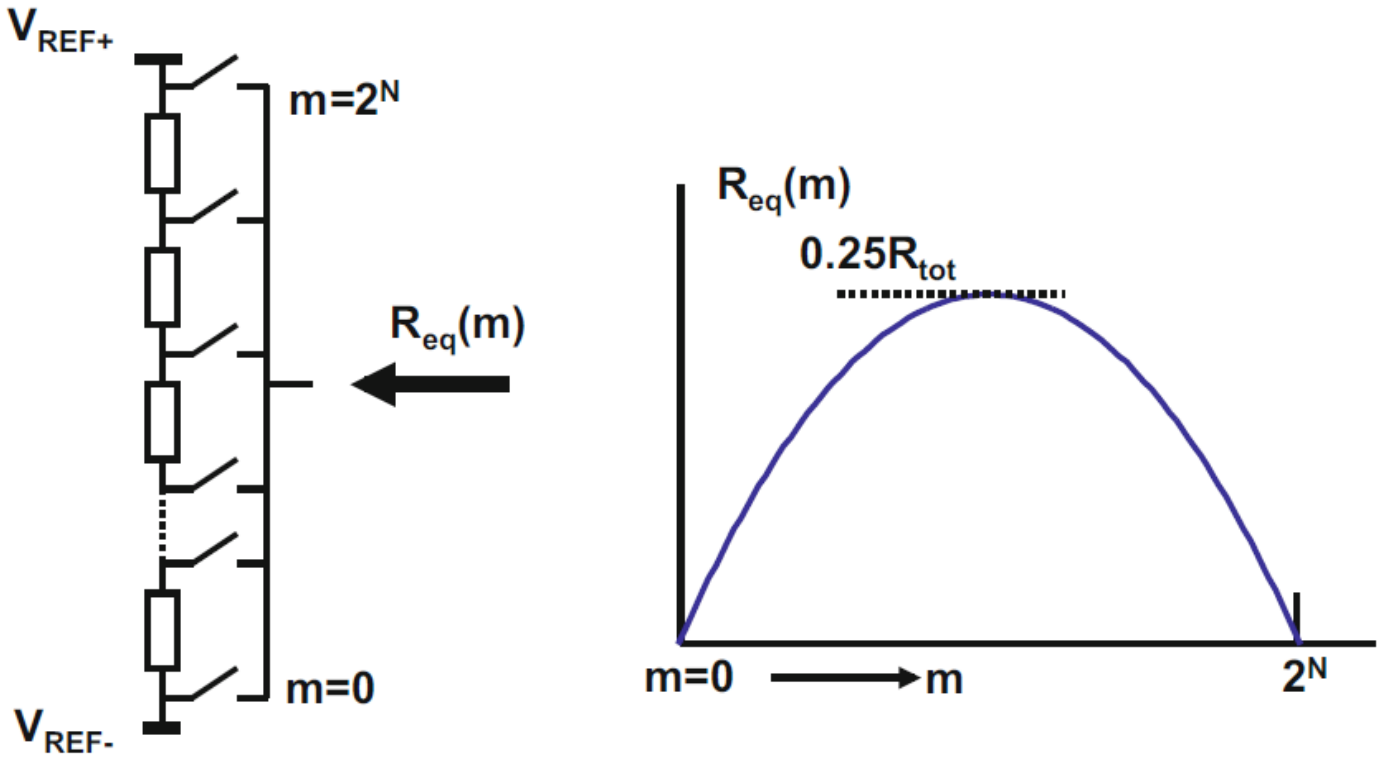
- Simply a voltage divider using 2^N identical unit resistors
- No. of switches = 2^N (**every** unit element needs a switch)
  - This is an example of a **unary** (thermometer) DAC
- Monotonicity is guaranteed
- The decoder is a bit complex



[W. Kester, ADI, 2005]

Resistor String (Ladder) DAC

- The resistor ladder impedance varies according to the tap position
  - Min at ends and max at the middle
  - The ladder output voltage must be buffered



[M. Pelgrom, 2017]

Resistor String (Ladder) DAC

- Transitions will cause spurious charges that disturbs the tap voltages of the string
  - A rough estimate for the time constant that assumes middle tap disturbance

$$\tau \approx \left(\frac{R_{tot}}{2} // \frac{R_{tot}}{2}\right) \times \frac{C_{tot}}{2} = \frac{R_{tot}C_{tot}}{8}$$

  - R_{tot} is total resistance and C_{tot} is total parasitic capacitance
  - We use $C_{tot}/2$ because not all parasitic caps are fully charged
  - Exact solution yields: $\tau = \frac{R_{tot}C_{tot}}{\pi^2}$
  - τ must be significantly smaller than the DAC sample rate

How Many Time Constants Are Enough?

- Assume linear settling of first order system

$$V(t) = V_i + (V_f - V_i)(1 - e^{-\frac{t}{\tau}})$$

$$T = \tau \ln\left(\frac{V_f - V_i}{V_f - V(T)}\right) = \tau \ln\left(\frac{\Delta V}{\epsilon}\right)$$

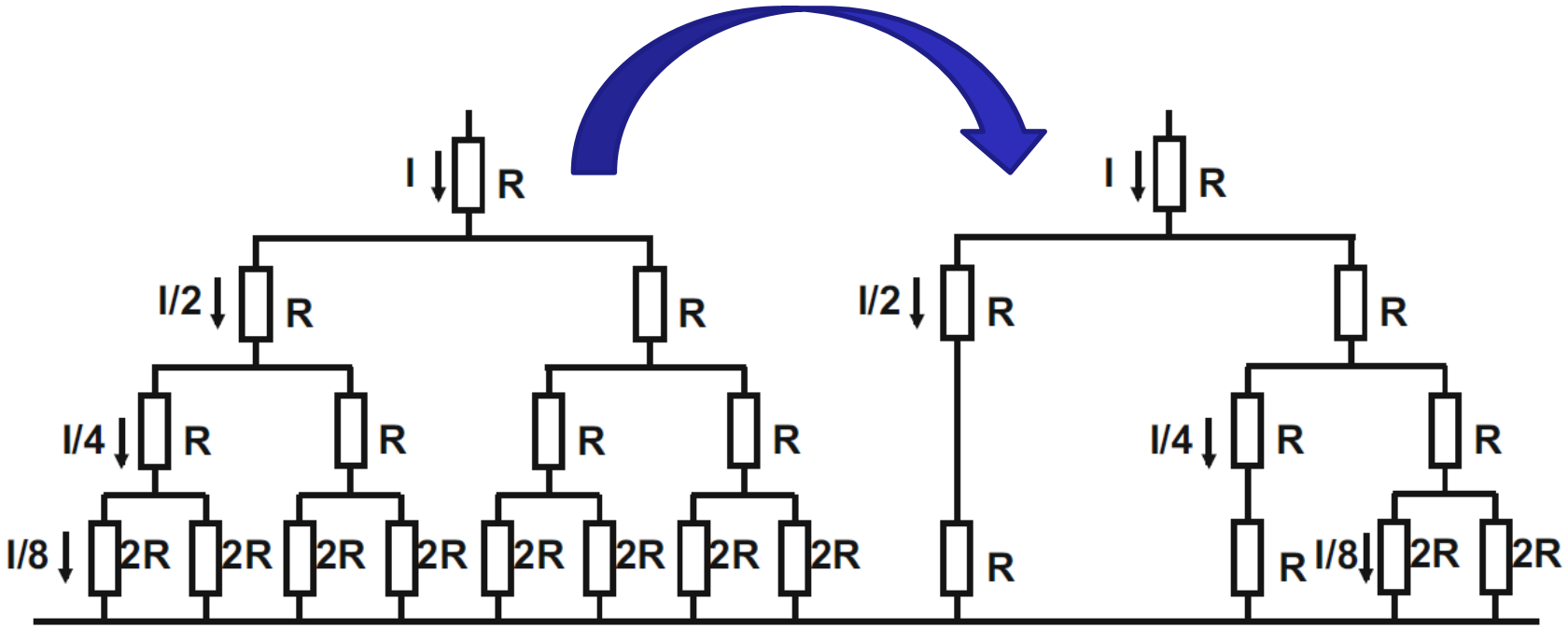
- If $\Delta V = FS$ and $\epsilon < 1LSB = \frac{FS}{2^N}$

$$T = \tau \ln(2^N) = 0.69N\tau$$

Resolution (N-bit)	No. of time constants
4	2.8
8	5.5
12	8.3
16	11.1
20	13.9
24	16.6

R-2R Ladder DAC

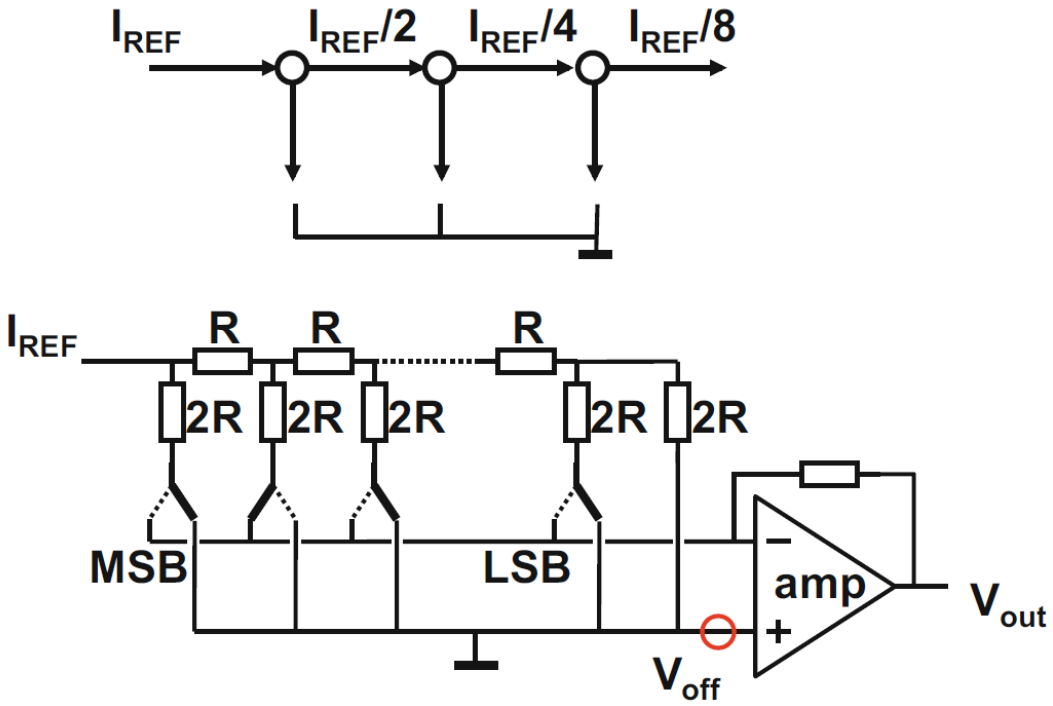
- Current splits equally at each level → Binary weighted currents
- At each node, looking downward the equivalent impedance is R
  - Each branch can be replaced by a resistance R with no effect on current splitting
- Current splits equally at each node between the "R" branch and the "2R" branch



[M. Pelgrom, 2017]

R-2R Ladder DAC

- Performance limited to 8-10-bit at low/medium speed
- Limitations
  - Buffer offset (virtual ground is not 0V)
  - Switches resistance (must be $\ll R$, or is made part of the 2R)
  - Buffer bandwidth



[M. Pelgrom, 2017]

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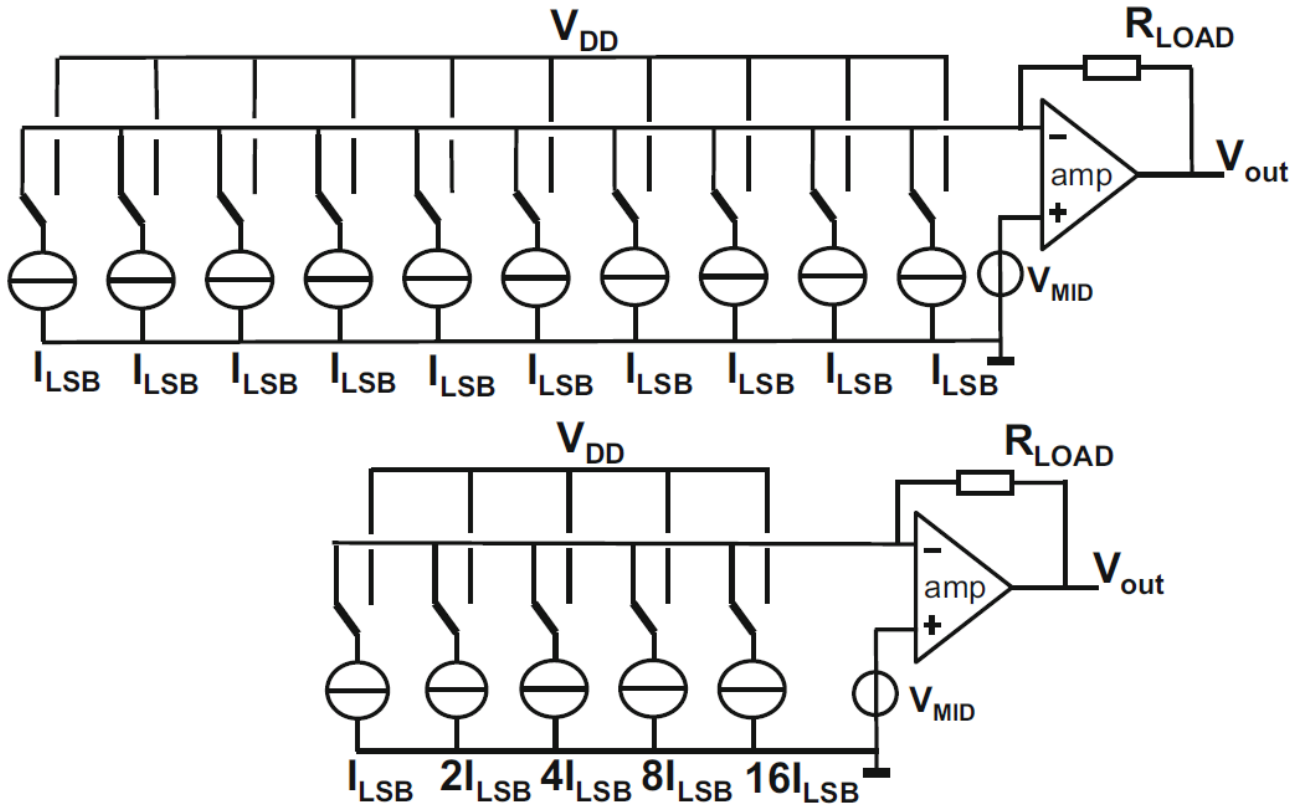
[M. Pelgrom, 2017]

Buffered Current Domain DAC

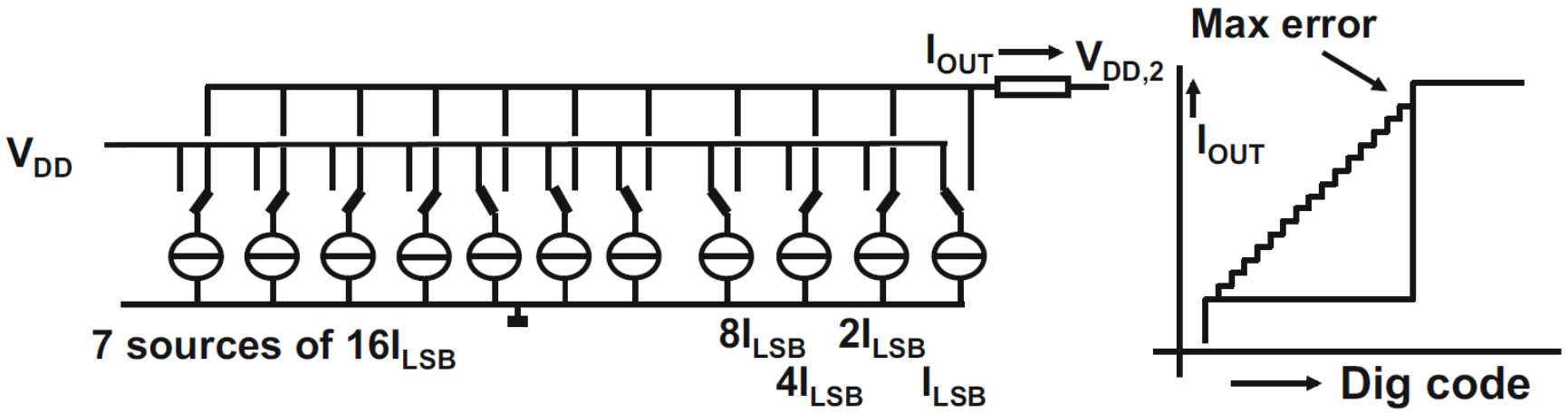
- Currents sources designed with relatively large area for good matching
- Current always active: steered to output or dumped to rail
- Op-amp keeps voltage across CS fixed, but limits speed



[M. Pelgrom, 2017]

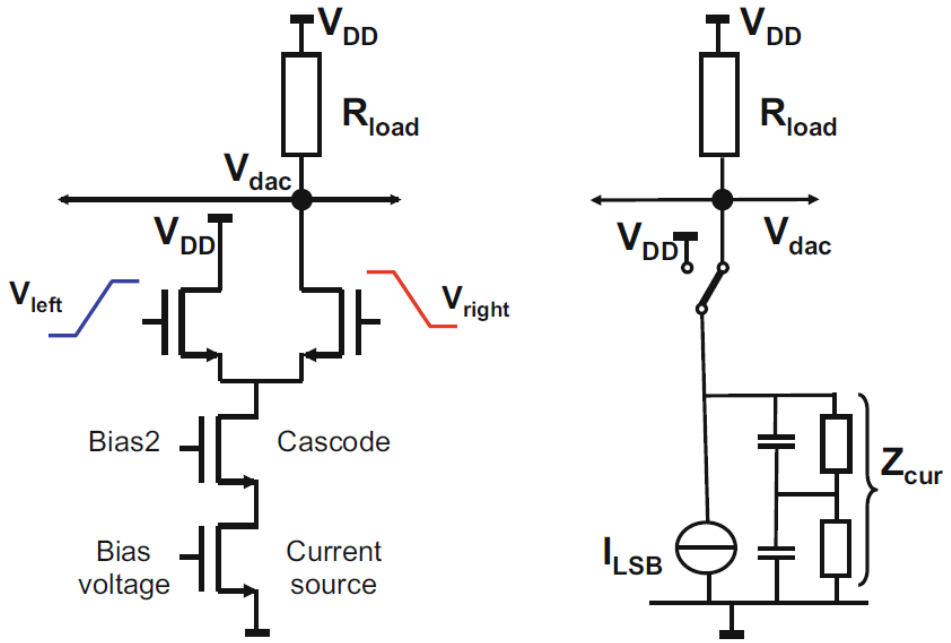
Current Steering DAC

- No bandwidth-limiting buffer ➔ High-speed architecture
  - Voltage across CS varies: Current modulation due to finite CS output impedance is a major problem
- Directly supplies current into 50-75 Ohm load
- Usually a segmented architecture is used
- The most popular high performance DAC architecture



Current Steering Unit Cell

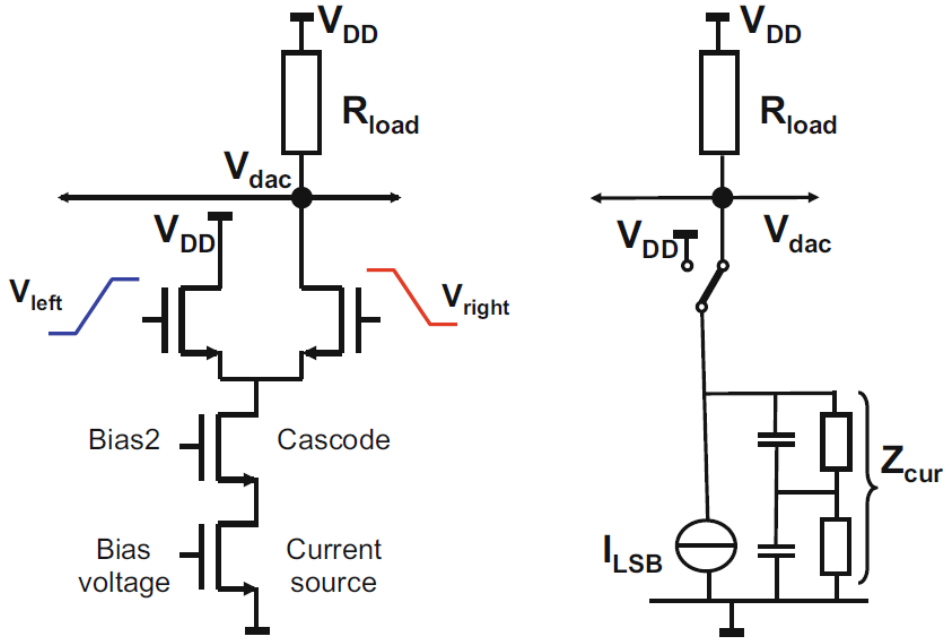
- Current is steered (not switched off). Why?
  - Avoid discharging the caps
    - Takes extra delay to build charge back (lower speed and more distortion)
  - Need small differential voltage to steer the current using the diff pair
- Max current consumption independent of digital input



[M. Pelgrom, 2017]

Current Steering Unit Cell

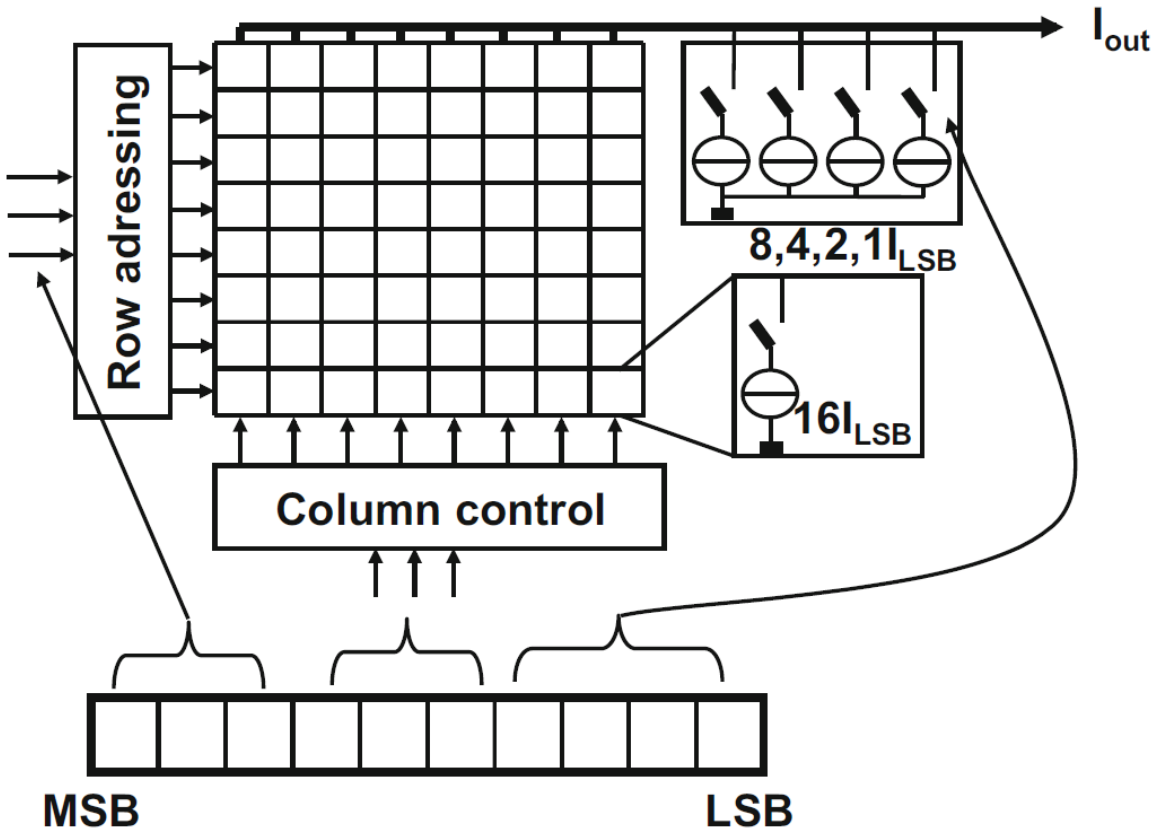
- Current is modulated by V_{dac} due to finite Z_{cur}
  - Current source cascoded to improve accuracy
- Non-linear distortion mitigated by making $Z_{cur}/2^N \gg R_{load}$
- 2^N current cells typically decomposed into a ($2^{N/2}\times 2^{N/2}$) matrix



[M. Pelgrom, 2017]

Matrix Decoded Current DAC

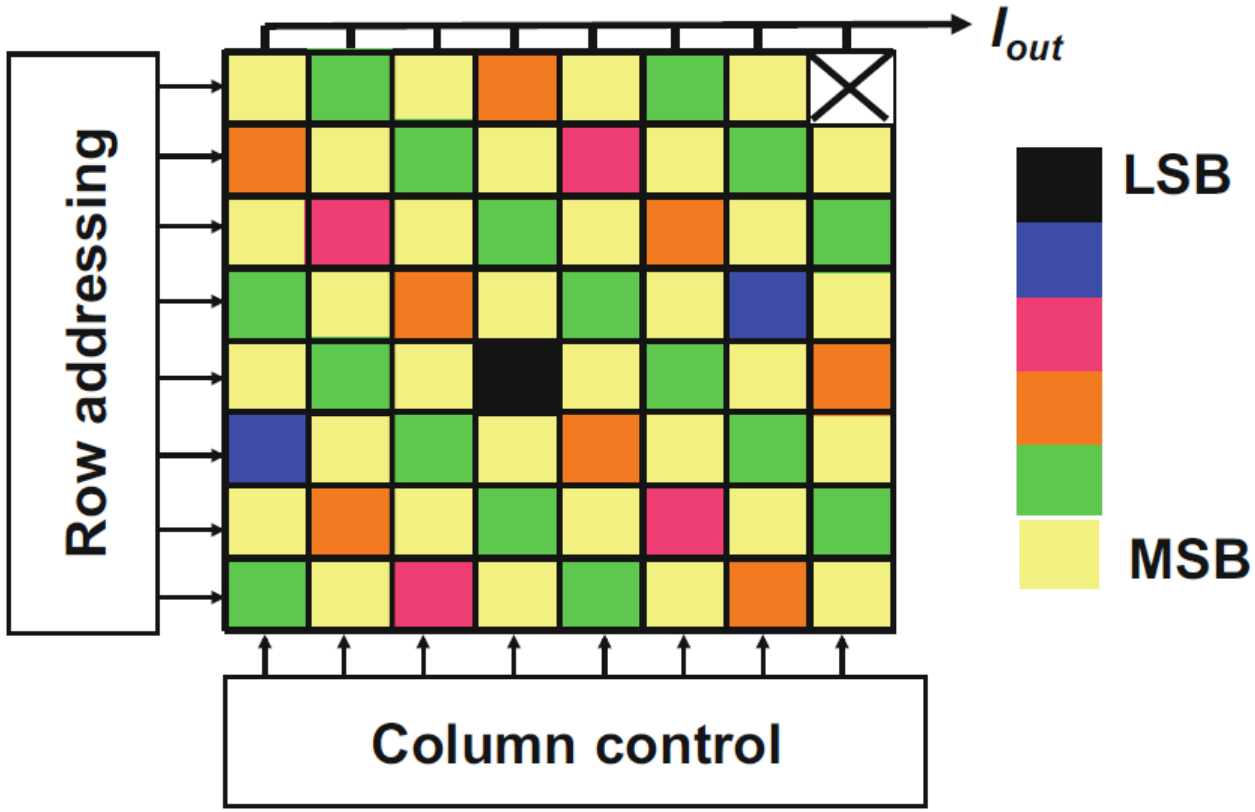
- 10-bit digital-to-analog converter:
  - Six MSBs are implemented as 64 unary current sources in a matrix configuration
    - Gradient effects mitigated
  - Four LSBs are designed in a binary series



[M. Pelgrom, 2017]

Matrix Decoded Current DAC

- Matrix decoding can be used as well for binary arrays
  - Common-centroid layout mitigates process gradients
  - Addresses first-order (linear) gradients only



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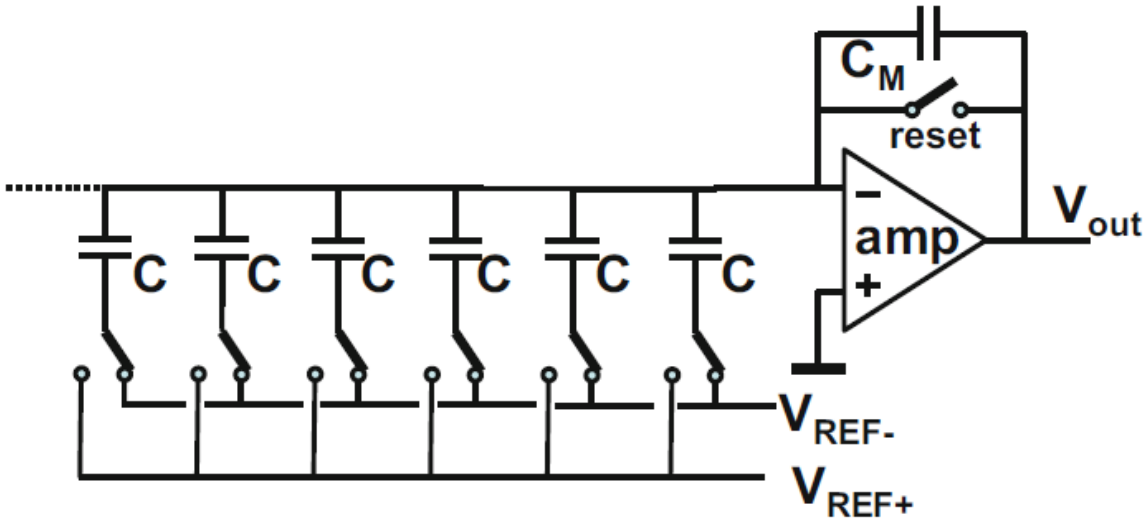
[M. Pelgrom, 2017]

SC Charge Domain DAC (1)

- Parasitic (stray) insensitive architecture
  - Bottom plate connected to ref voltage (bottom plate sampling)
  - Top plate connected to virtual ground
- Assume m unit capacitors are switched from V_{REF+} to V_{REF-}

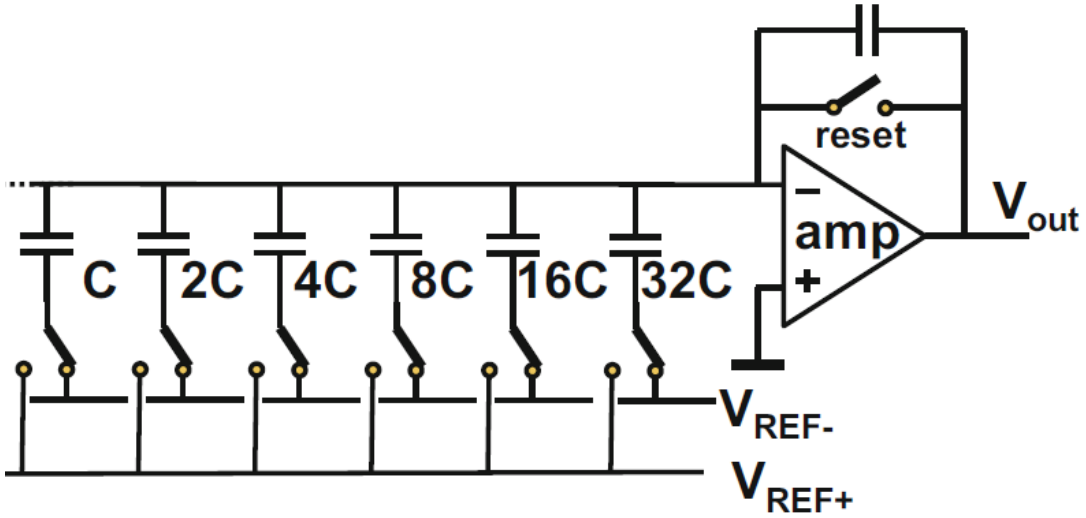
$$V_{out} = -\frac{mC(V_{REF-} - V_{REF+})}{C_M}$$



[M. Pelgrom, 2017]

SC Charge Domain DAC (2)

- Key advantage: No static power (except in OTA)
  - Excellent energy efficiency
- A.k.a. charge redistribution DAC, capacitive DAC
- Charge transfer (redistribution) is insensitive to jitter
- Capacitor array is usually binary or segmented
  - Unary capacitor array wiring and switches are impractical
- INL and DNL limited by capacitor array mismatch



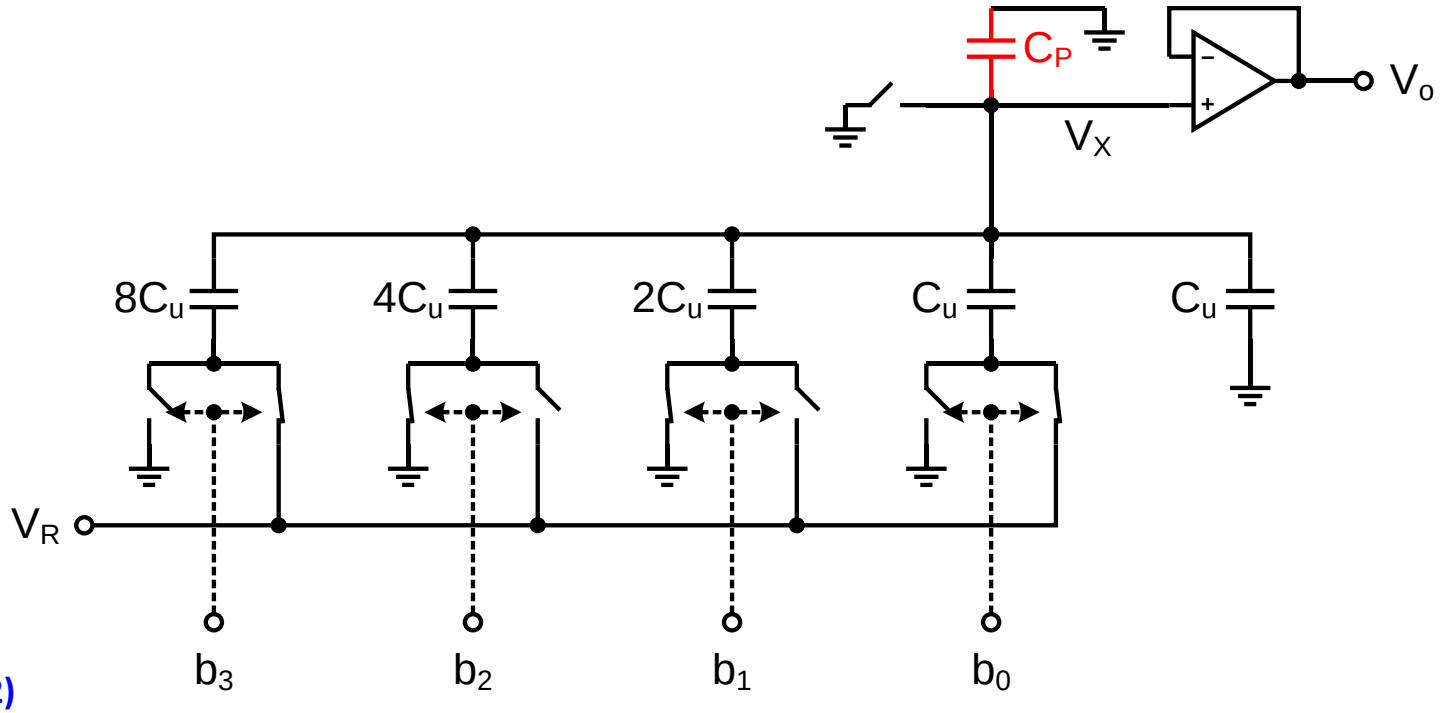
[M. Pelgrom, 2017]

SC Charge Domain DAC (3)

- Stray sensitive architecture
- Assume m unit capacitors are switched from 0 to V_R

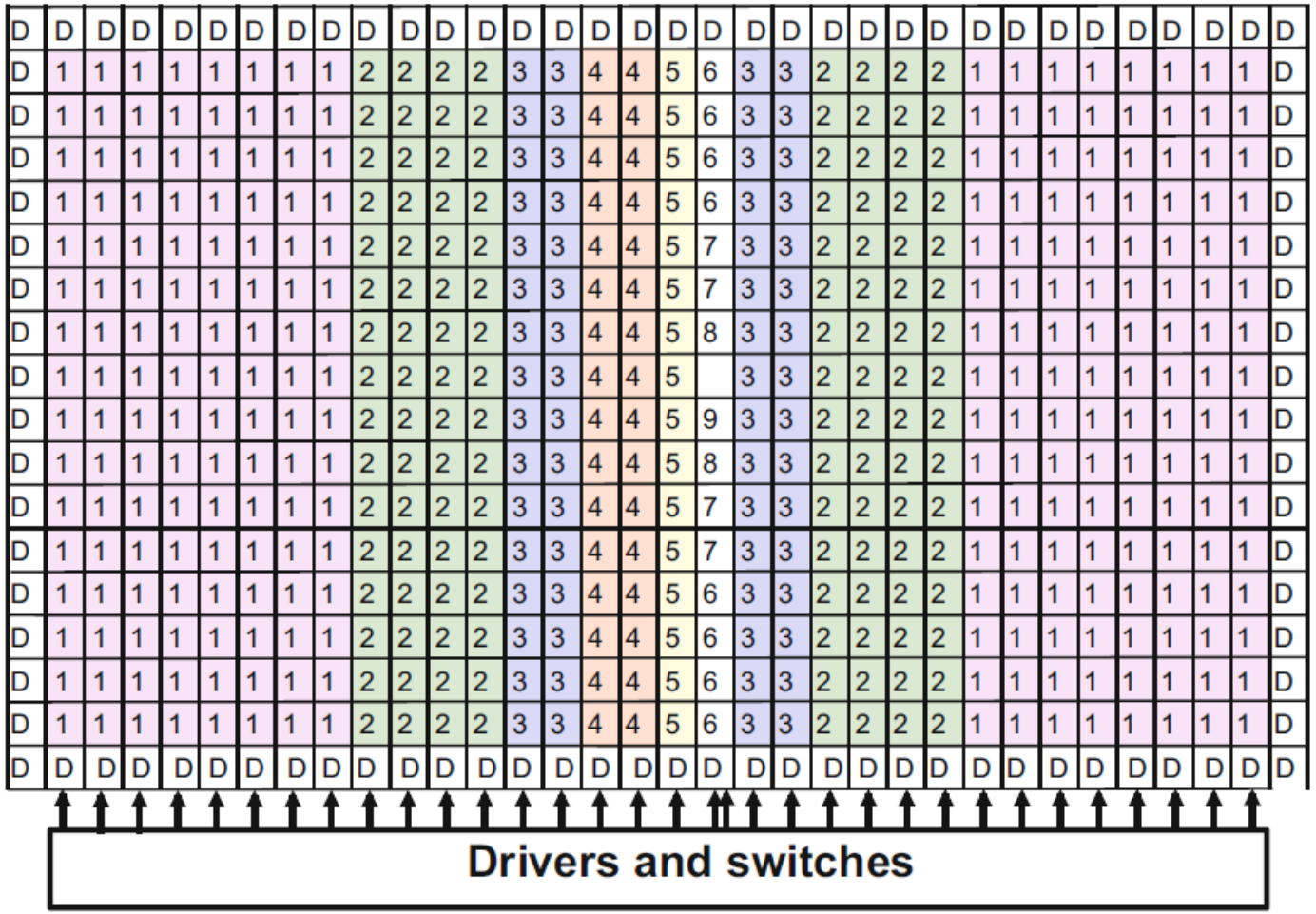
$$V_o = \frac{mC_u}{C_p + nC_u} \cdot V_R = \frac{C_u \cdot \sum_{j=0}^{N-1} 2^j b_j}{C_p + 2^N C_u} \cdot V_R$$

- Cp → gain error (nonlinearity if Cp is nonlinear, e.g., Cin of OTA or CMP)



Capacitor Array

- Capacitors can have very good matching properties
  - Main limitation is the exponential growth of the cap array area



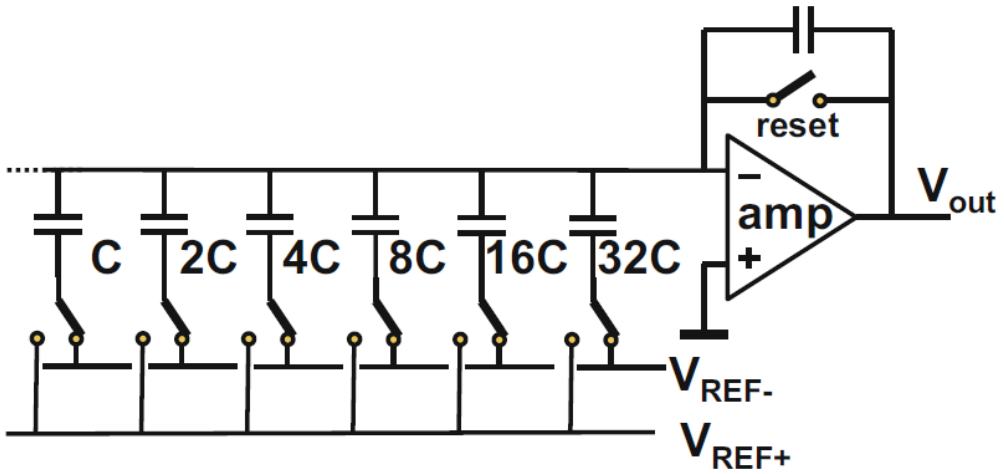
[M. Pelgrom, 2017]

Capacitor Array

- Unit capacitors can be few (or sub) femtofarad(s)
  - H. Omran *et al.*, "Matching Properties of Femtofarad and Sub-Femtofarad MOM Capacitors," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 6, pp. 763-772, June 2016.
  - H. Omran *et al.*, "Direct Mismatch Characterization of Femtofarad Capacitors," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 2, pp. 151-155, Feb. 2016.
  - P. J. A. Harpe *et al.*, "A 26 uW 8 bit 10 MS/s Asynchronous SAR ADC for Low Energy Radios," in *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1585-1595, July 2011.

Capacitor Array

- Unit capacitors can be few (or sub) femtofarad(s)
- Alternatives to using very small unit capacitors:
  1. Using capacitors in series (parasitic sensitive)
  2. Using intermediate bottom plate voltages generated by a resistor string DAC (extra power consumption)



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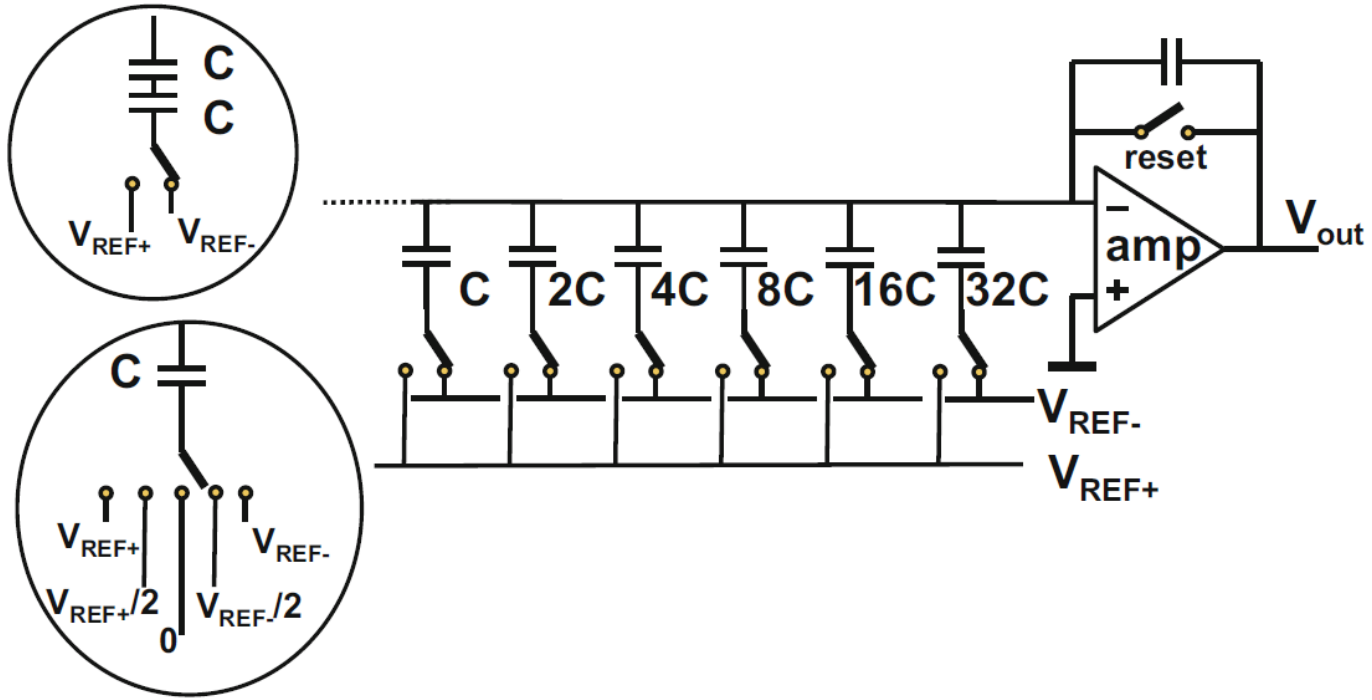
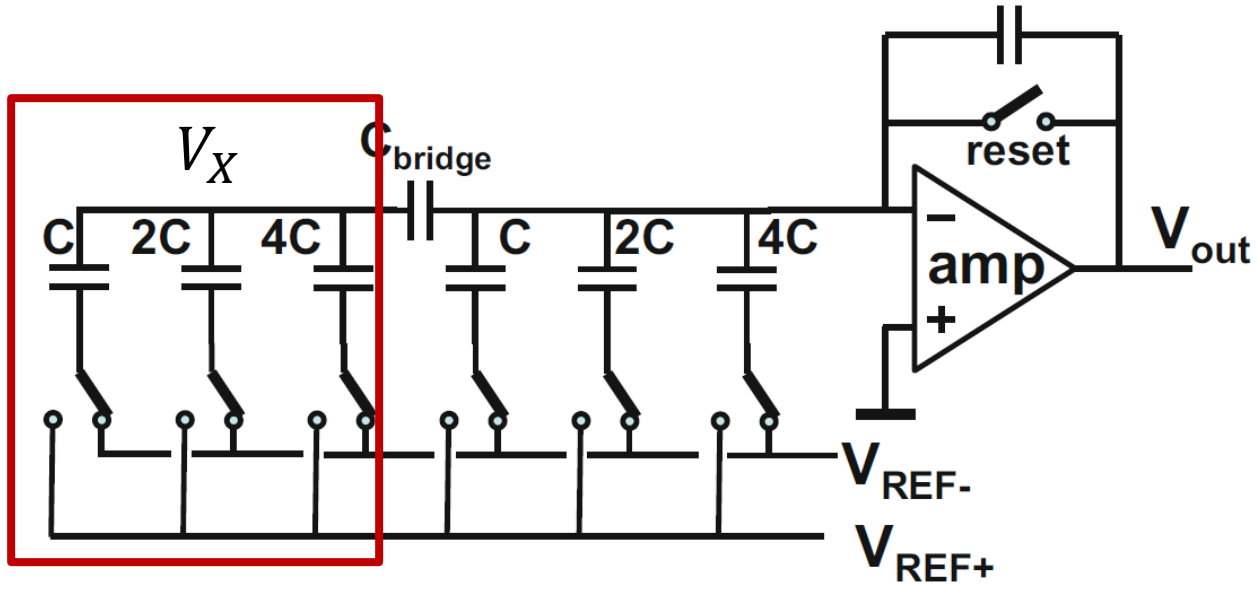


[M. Pelgrom, 2017]

Capacitor Array

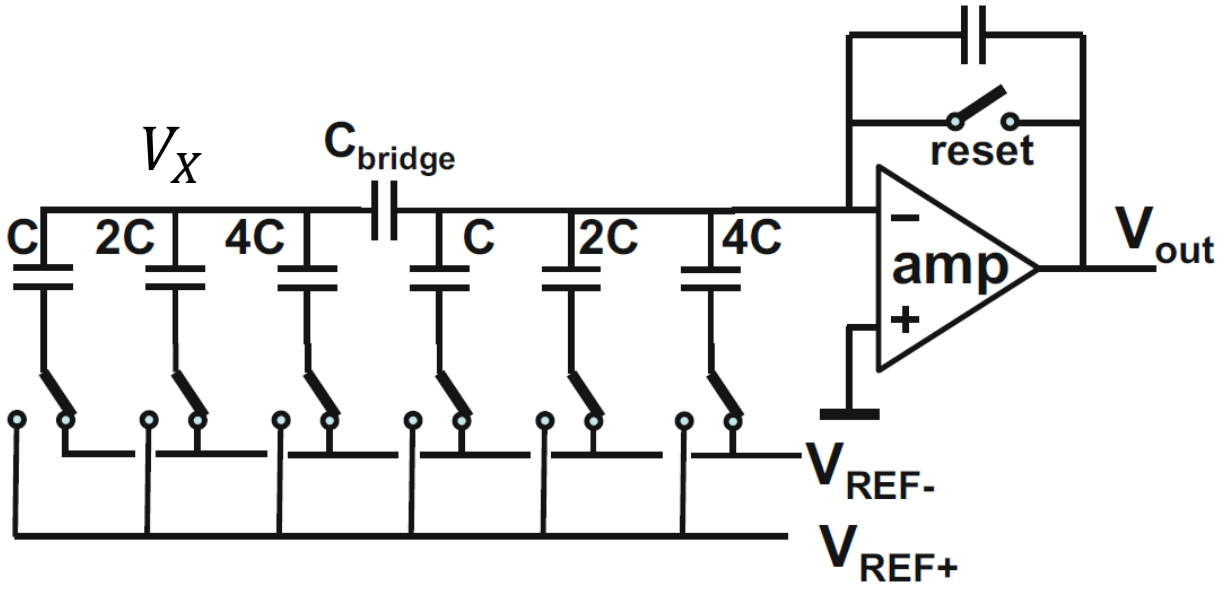
- Alternatives to using very small unit capacitors:
  3. Using bridging capacitor (parasitic sensitive)
     - The array to the left of $C_{bridge} = C$ replaces the string DAC
     - The voltage on the left side plate of C_{bridge} is set by a capacitive divider



[M. Pelgrom, 2017]

Bridge Capacitor Example

- Let $V_{REF+} = 1V$ and $V_{REF-} = 0$
  - XXX001 → $V_X = \frac{C}{C_b+7C} = \frac{1}{8}$
  - XXX111 → $V_X = \frac{7C}{C_b+7C} = \frac{7}{8}$



[M. Pelgrom, 2017]

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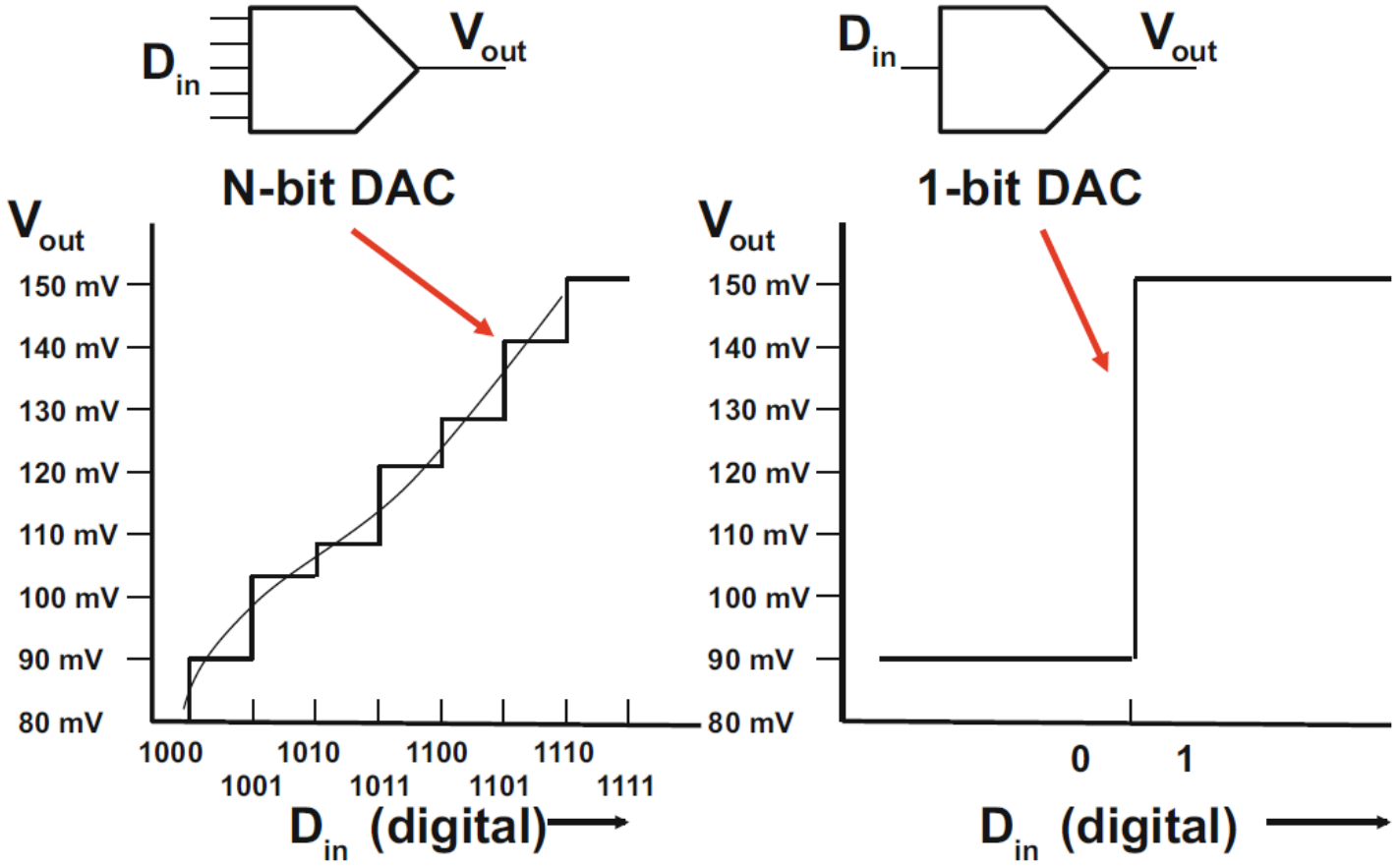
[M. Pelgrom, 2017]

Single-Bit DAC

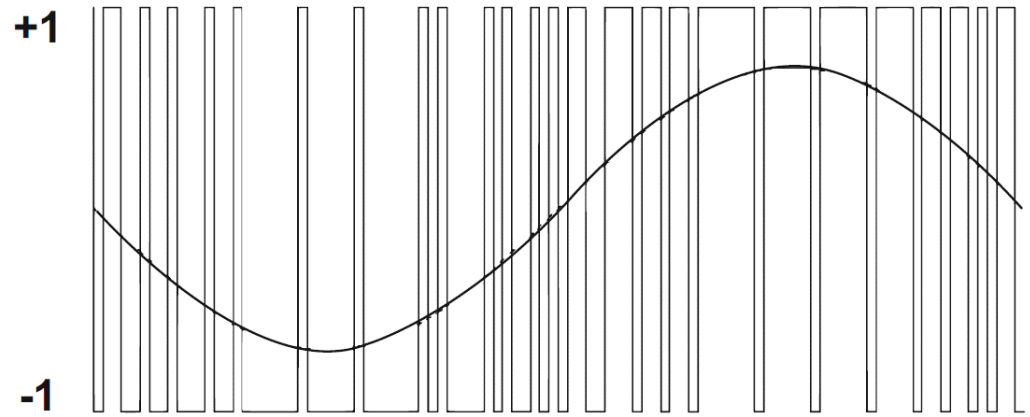
- One-bit DAC has two levels only ➔ It cannot have linearity errors!
  - No matched components are required!

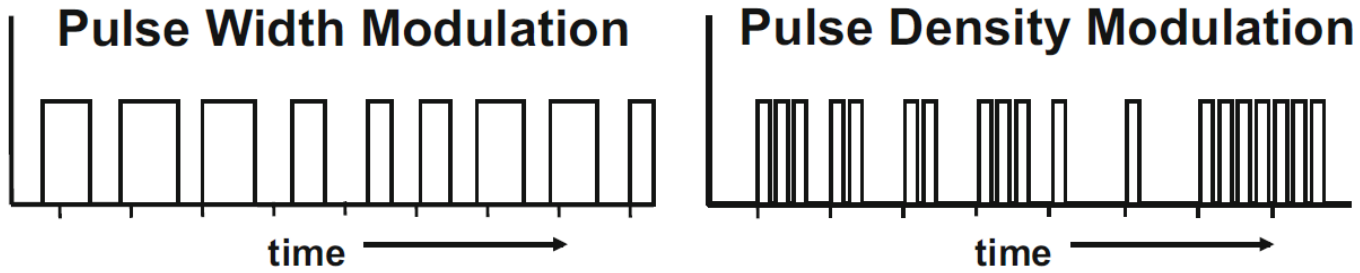


[M. Pelgrom, 2017]

Single-Bit DAC

- Use large oversampling ratio (OSR): $f_s \gg f_{Nyquist}$
- Pulse width modulation (PWM) or pulse density modulation (PDM)
- PDM avoids distortion due asymmetries in falling and rising edges
- The signal is reconstructed by a LPF





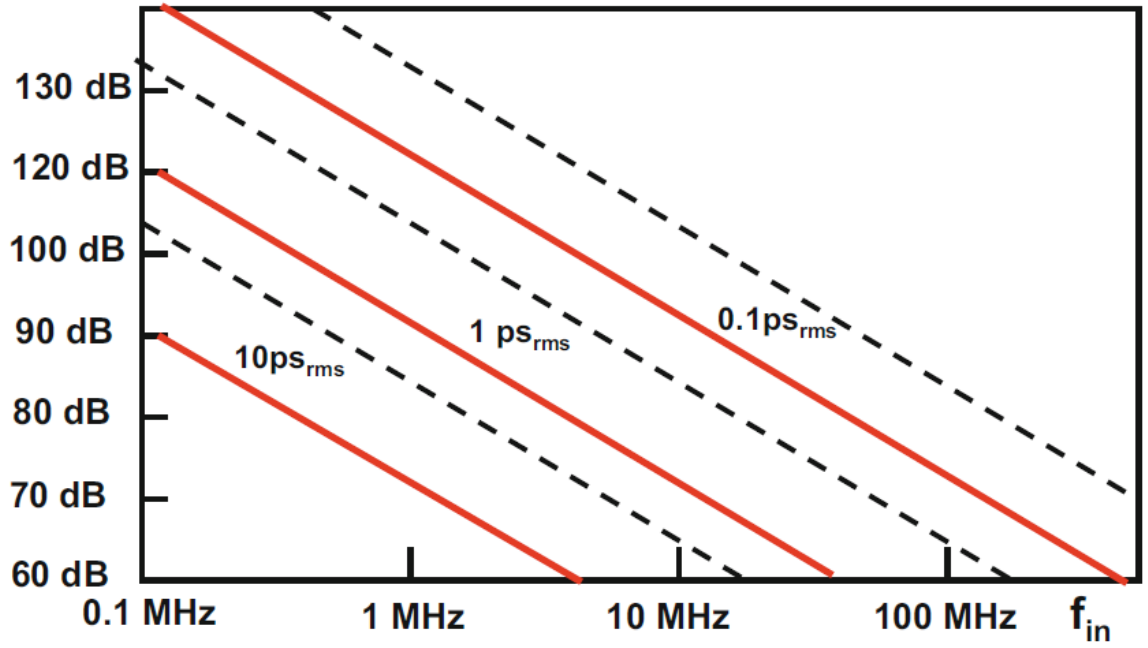
[M. Pelgrom, 2017]

Jitter-Limited SNR

- Assume single-bit DAC output from –A to A with activity factor = α

$$SNR = \frac{A^2/2}{\left(2A \times \sigma_{jit} \times \frac{1}{T_s} \times \alpha\right)^2} = \frac{1}{\left(2\sqrt{2}\alpha f_s \sigma_{jit}\right)^2} = \frac{1}{\left(4\sqrt{2}\alpha f_{sig} \sigma_{jit} \times OSR\right)^2}$$

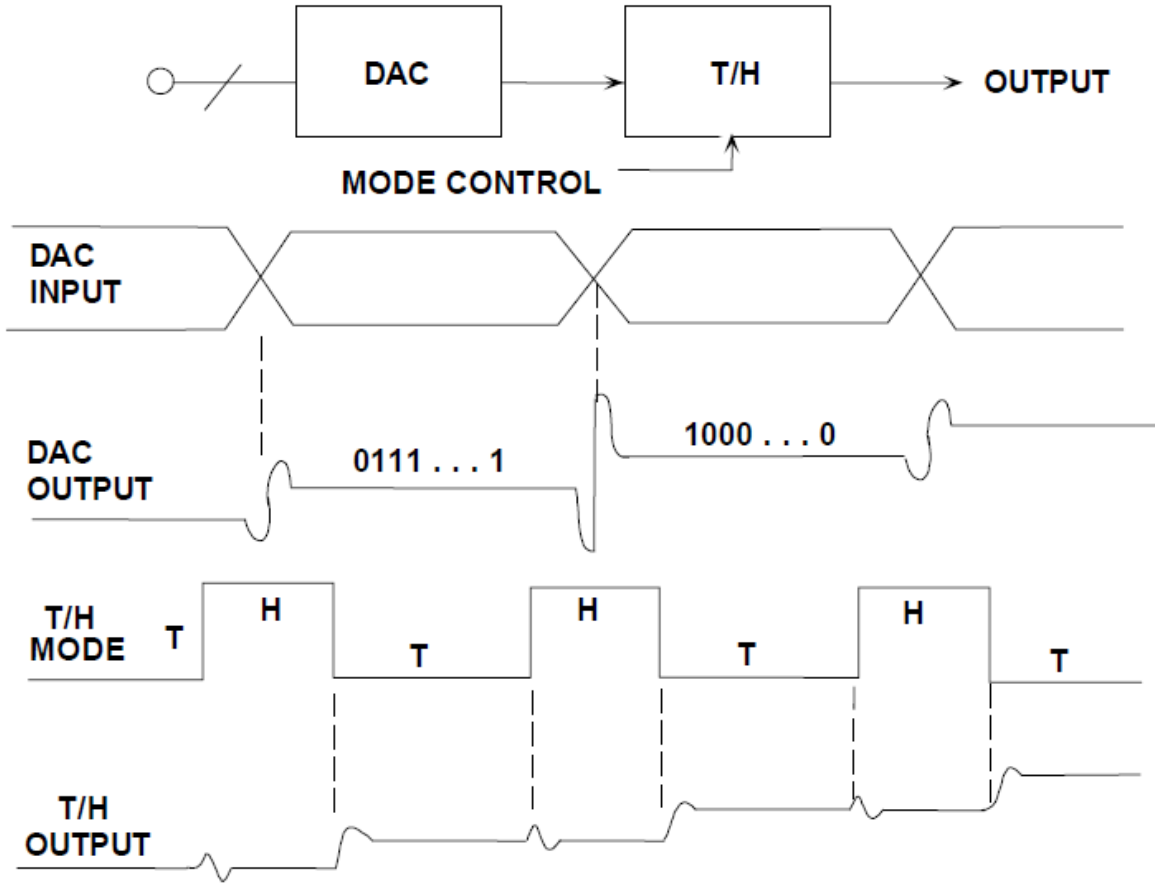
- Solid: single-bit DAC with OSR = 5 and dotted: sampled DAC
  - Single-bit DAC suffers much more from jitter (σ_{jit} is multiplied by pk-to-pk swing)



[M. Pelgrom, 2017]

Deglitching using a Track & Hold

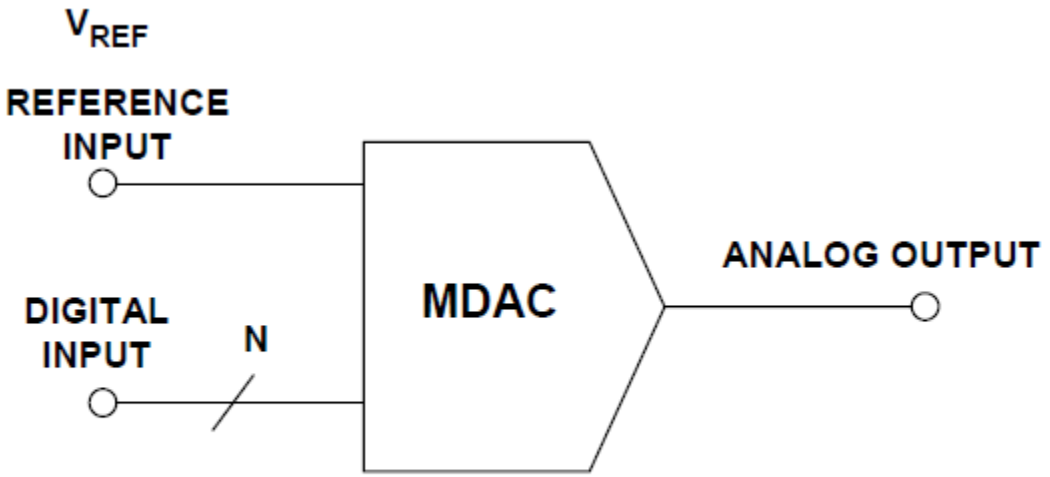
- DAC switching glitches are isolated from the output
- T/H transients are code independent and occurs at the clock frequency (can be filtered out)



[W. Kester, ADI, 2005]

Multiplying DAC

- DAC output is the produce of V_{REF} and a digital code
- If V_{REF} can be a varying signal ➔ multiplying DAC (MDAC)
- Four-quadrant multiplying DAC: A bipolar DAC with a bipolar V_{REF}



ANALOG OUPTUT = V_{REF} × DIGITAL INPUT × CONSTANT

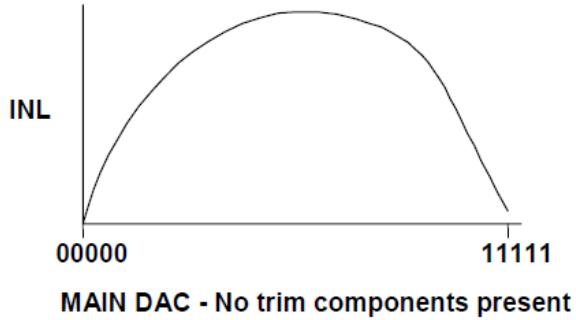
[W. Kester, ADI, 2005]

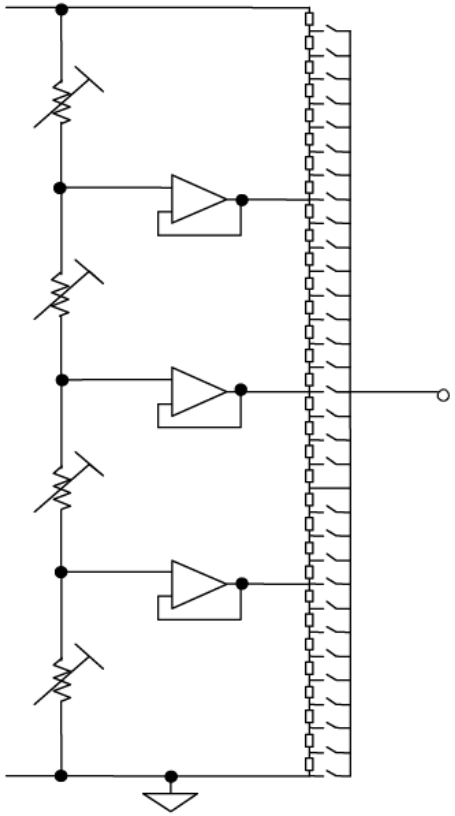
Improving DAC Accuracy

- Good design and layout can largely eliminate systematic errors
  - But random errors will limit DAC resolution to ~ 12-bit
- Methods to further improve the accuracy
  - Trimming
  - Calibration
  - Dynamic element matching (DEM)
  - …

Trimming

- A 2nd resistor string is connected in parallel with the main string
  - The resistors are made physically large enough to laser trim
  - Connected by buffer amplifiers to the ¼, ½, and ¾ points
  - INL is reduced by a factor of four

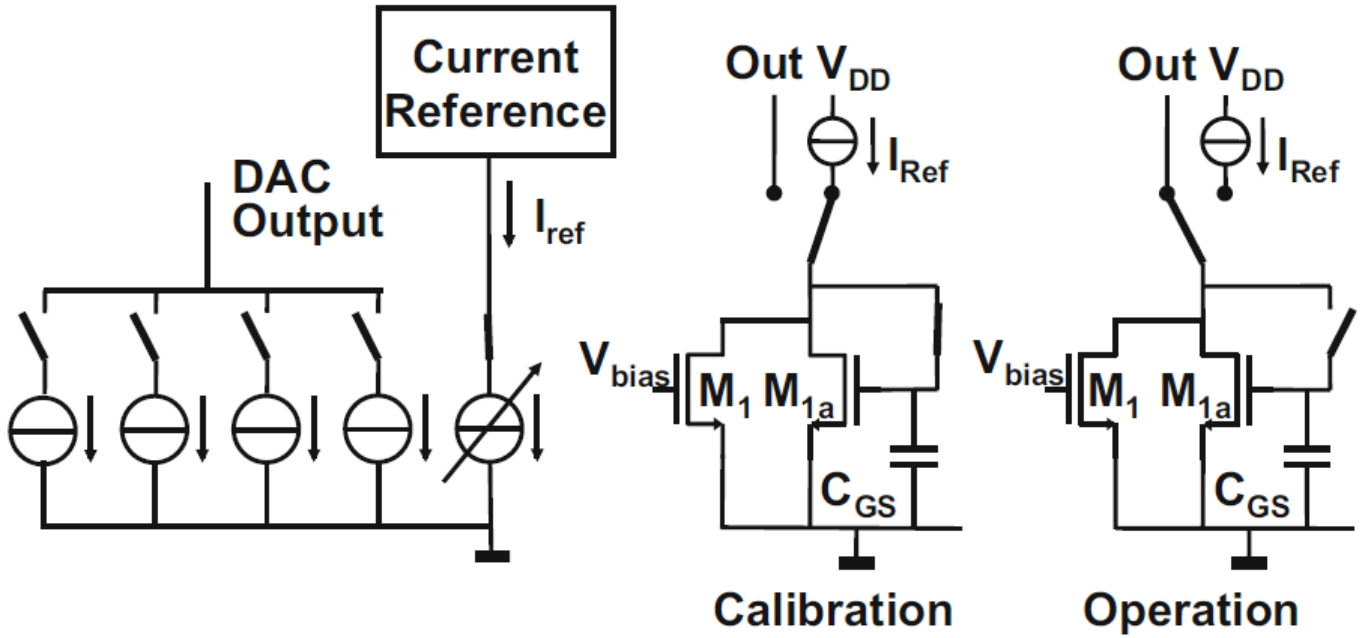




[W. Kester, ADI, 2005]

Current Calibration

- M1 supplies the majority of current as a traditional current source
- M1a is used to calibrate and to mitigate the inherent mismatch
- The calibration mechanism rotates through the array tuning all current sources
- The main problem in this arrangement is the sampling of noise in the calibration cycle

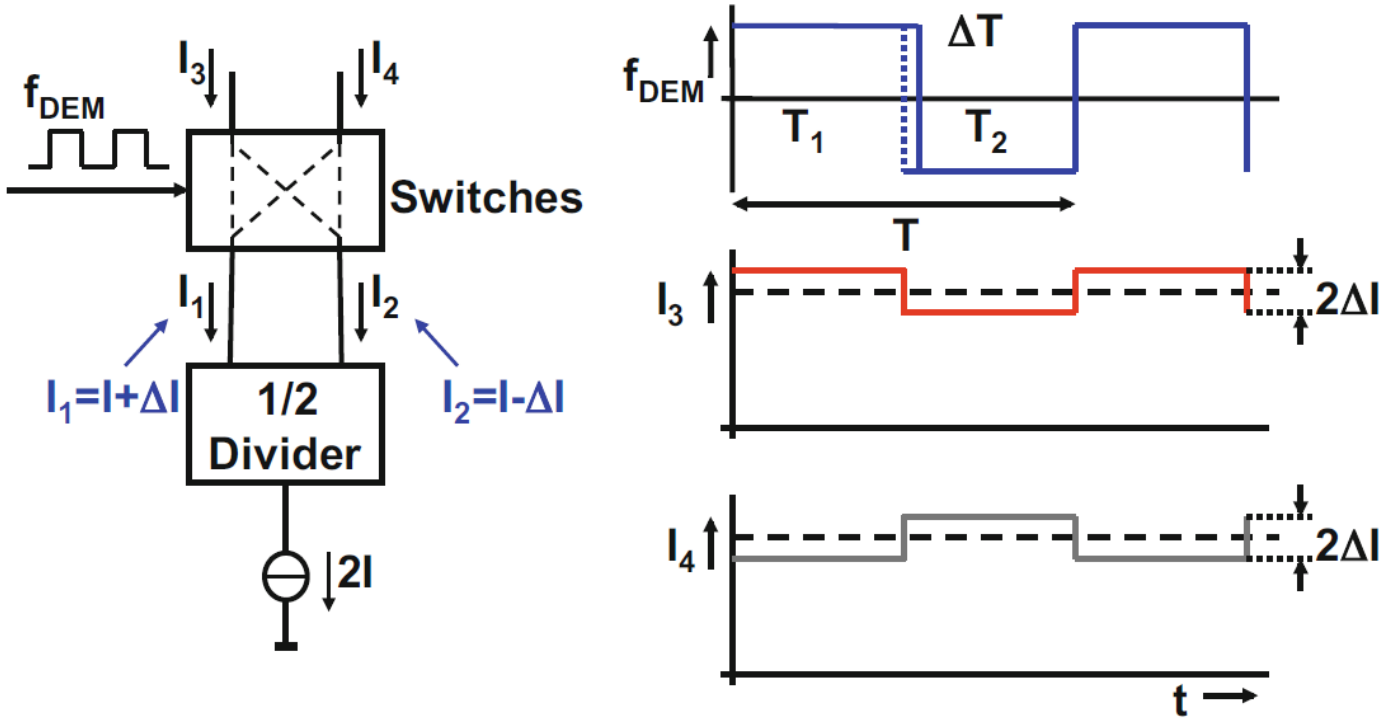


[M. Pelgrom, 2017]

Dynamic Element Matching (DEM)

- Unit currents are swapped ➔ Average error tends to zero

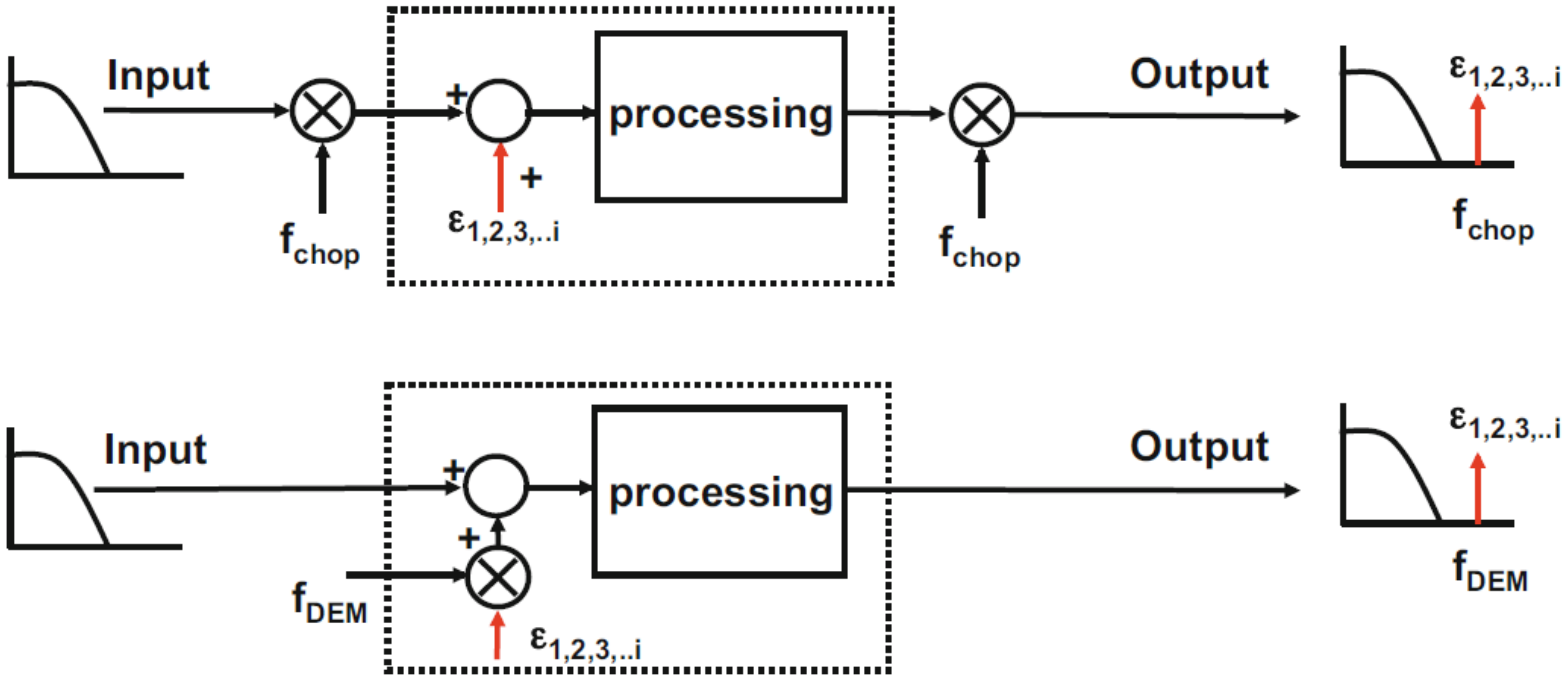
$$\frac{I_3 - I_4}{I_3 + I_4} = \frac{I_1 - I_2}{I_1 + I_2} \times \frac{t_1 - t_2}{t_1 + t_2}$$



[M. Pelgrom, 2017]

Chopping vs DEM

- A DEM with a fixed swapping frequency generates an error spectrum with tones at the multiples of the swapping frequency
- Some designs use a pseudorandom swapping sequence to spread out the error energy over the spectrum (mismatch scrambling)
- Mismatch shaping can be also applied



[M. Pelgrom, 2017]

References

- M. Pelgrom, Analog-to-Digital Conversion, Springer, 3rd ed., 2017.
- W. Kester, The Data Conversion Handbook, ADI, Newnes, 2005.
- B. Boser and H. Khorramabadi, EECS 247 (previously EECS 240), Berkeley.
- B. Murmann, EE 315, Stanford.
- Y. Chiu, EECT 7327, UTD.

Thank you!