Analog Integrated Circuits
Lec 21: SR and PSR

① Linear Settling.

1 For a LTI (Linear time invariant) systems (linear systems)

Scaling the input will scales the output

∴ Settling time $\neq f(V_{in})$

2 Time Constant τ of the system does not depends on input level

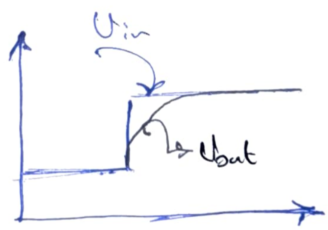
∴ we need to settle to a higher voltage in the same time

⟶ need larger slope ⟶ need larger current

∴ Linear settling: scaling the input scales the output slope and output current

3 $V_{out} = V_{step}(1 - e^{-\frac{t}{\tau}})$

$$\frac{dV_{out}}{dt} = V_{step}\left(\frac{1}{\tau} e^{-\frac{t}{\tau}}\right)$$



$$\therefore \frac{dV_{out}}{dt} \propto V_{step}$$

$$\therefore I_{out} = C_L \frac{dV_{out}}{dt} \longrightarrow I_{out} \propto V_{step}$$

4 If I_{out} reaches the max value

∴ Settling changes from linear settling to non-linear settling ☹

(2) The non-Linear settling.

1. non-linear settling: Output slope and Current NOT α input
   ∴ Output is linear ramp → finite Constant slope
2. SR (Slew rate): The max possible slope of the op-amp output
3. Linear ramp → Constant charging a Cap

$$I_{out} = C_L \frac{dV_{out}}{dt} \rightarrow SR = \left(\frac{dV_{out}}{dt}\right)_{max} = \frac{I_{out\,max}}{C_L}$$

4. Slope independent of the input level
   ∴ non-Linear behaviour → non-Linear system

(3) Example.

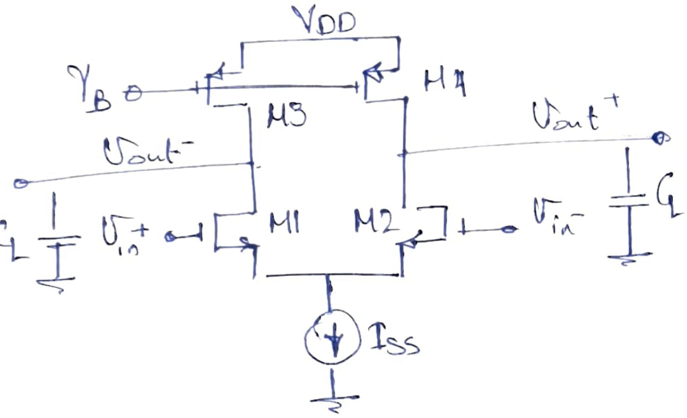
1. Small input setep: Linear Settling
   1. output Voltage has exponetial settling behavior
   2. when the output settles → $\Delta V_{id} = V_{in} - V_{out} \simeq 0$

   $\therefore I_{out} = g_m \Delta V_{id}$

2. Large input step: Slewing
   1. M2 off → Iss is fully steered to M1 → M3 → M4 → then to C_L
   2. Non-Linear settling: Output slope and charging Current α input
      ∴ Linear ramp → Constant Current (Iss) charging a Capacitor
   3. As Vout approaches V_{in} the Circuit resumes linear settling (exp)
   4. $SR = \frac{I_{ss}}{C_L}$ → efficiency ≈ 100%

(4) SR of FD-OTA

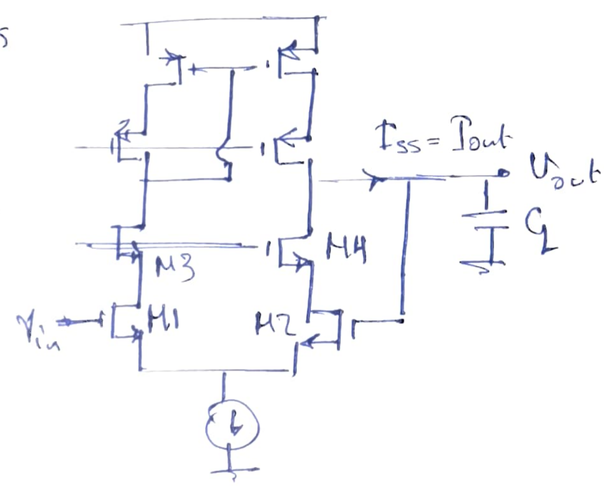
1. @ V_{out^-} : $SR = \frac{I_{ss}}{2C_L}$
2. @ V_{out^+} : $SR = \frac{I_{ss}}{2C_L}$
3. @ $V_{out,dd} = V_{out}^+ - V_{out}^-$; $SR = \frac{I_{ss}}{C_L}$



Symetrical slewing → Necessary to maintain Constant CM Level

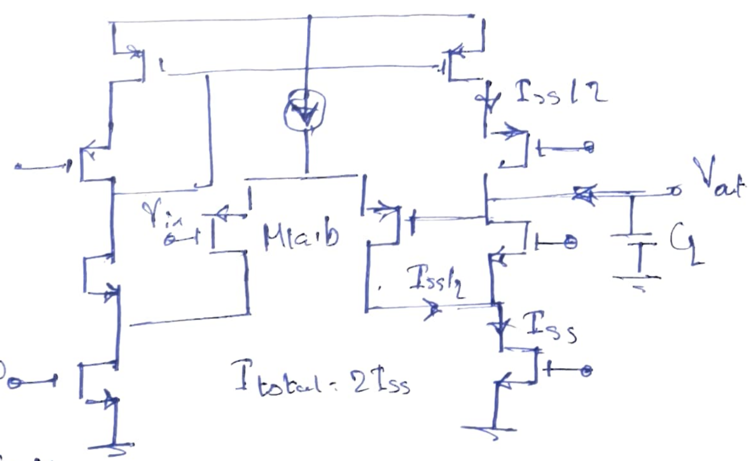
(5) SR of Telescopic Cascode

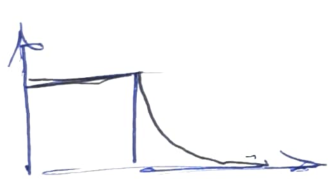
1. applying large V_{in} → M_1 $I_D = I_{ss}$
   ∴ M2 and M4 turned off
2. I_{ss} mirrored to the output C_L
   ∴ $I_{out\,max} = I_{ss}$
3. $SR = \frac{I_{ss}}{C_L}$ → efficiency = 100%



(6) Folded Cascode OTA SR

1. usually set $I_{ss} = 2I_{B1@}$
   ∴ $I_{D@,CG} = I_{D@CS}$
2. at equilibrium
   $I_{B2} = I_{B1@} + \frac{I_{ss}}{2}$
3. at slewing, $I_{B1} = I_{B2} - I_{ss} = 0$
4. $SR = \frac{I_{ss}}{C_L}$ → efficiency = 50%

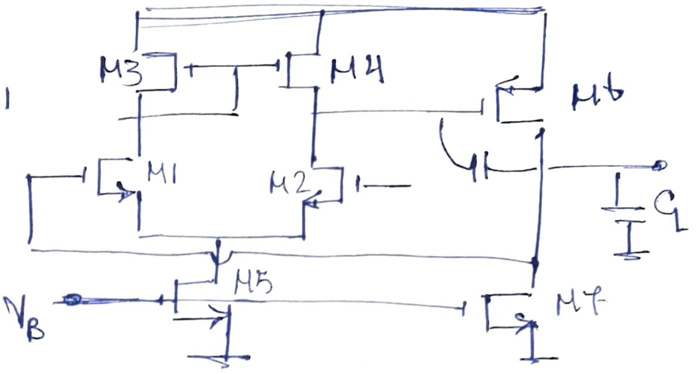




(7) Two Stage miller OTA SR

1 I_{B2} much Larger than I_{B1}

→ SR usually Limited by I_{B1}



2 internal Selwing Limits Output Slewing

3 Positive Slewing

$$\frac{I_{D6} - I_{B1} - I_{B2}}{C_L} > \frac{I_{B1}}{C_1 + C_c}$$

$$SR_+ \approx \frac{I_{B1}}{C_1 + C_L}$$

4 Negative Slewing

$$\frac{I_{B2} - I_{B1}}{C_L} > \frac{I_{B1}}{C_1 + C_c}$$

$$SR_- = \frac{I_{B1}}{C_1 + C_c}$$

5 Must be designed such that $SR_+ = SR_-$

∴ Both Limited by I_{B1}

6 Otherwise the Slewing is asymmetric

* Causes shift in CM output
* Slow transients if CMFB network is Slow

(8) Power Supply rejection

1 Supply Lines Carry noise from regulators, digital Loads, etc.

2 We don't Want Vout to be affected by VDD noise

$$PSR = \frac{1}{V_{out}/V_{DD}}$$

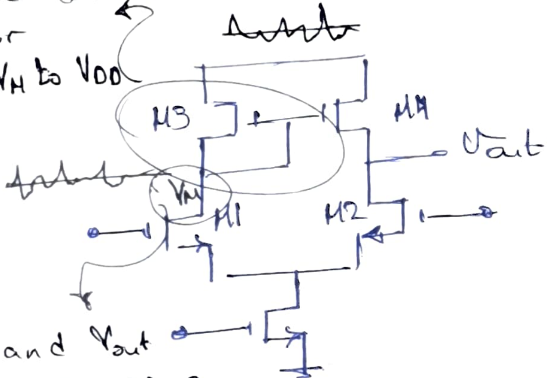
$$PSRR = \frac{V_{out}/V_{in}}{V_{out}/V_{DD}} = A_{vd} \cdot PSR$$

Both PSR and PSRR usually reported in dB

(9) PSRR Example 5T OTA

$$PSR = \frac{1}{V_{out}/V_{DD}} = 1$$

The diode connected transistor clamps V_H to VDD



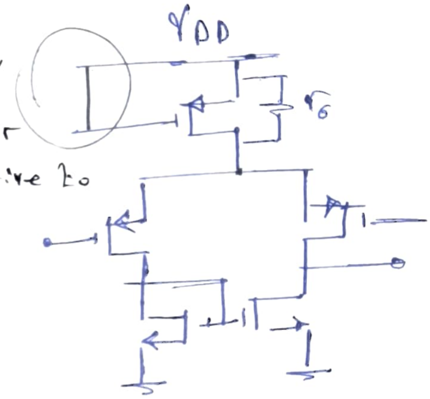
V_H and V_{out} experience approx the same change as VDD

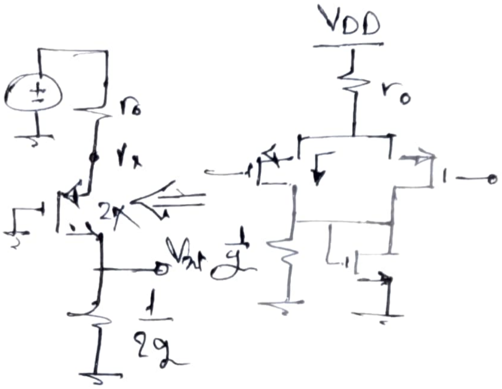
$$PSRR = A_{vd} \cdot PSR$$

$$= \frac{g_{m1,2}(r_{o2} \parallel r_{o4})}{1}$$

(10) PSRR of 5T-OT with PMOS input pair

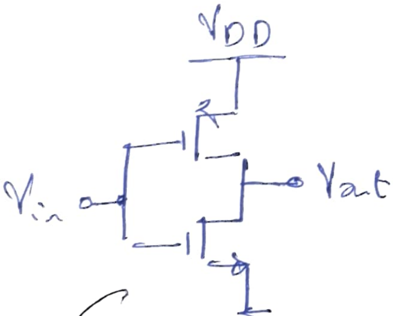
PMOS Current mirror is biased relative to VDD





$$PSRR = \frac{A_{vd}}{V_{out}/V_{dd}} \approx CMRR \approx (g_m r_o)^2$$

(11) PSRR of inverter



$$\frac{V_{out}}{V_{dd}} = g_m\left(\frac{r_o}{2}\right) \text{ very high}$$

$$\frac{V_{out}}{V_{in}} = g_m r_o$$

$\therefore$ PSRR $= 2$ ☹