Analog Integrated System Design.

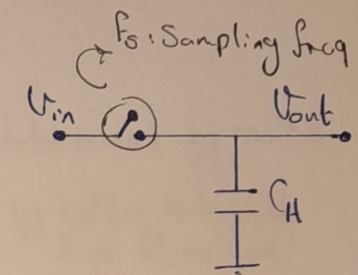
lec 7: Basics of Sample and Hold Circuits.

① Sampling.

1 Converts a Continous time Signal to a discrete time Signal this results a Sequance of numbers (Samples)

2 Sampling instants are defined by clk sig f_s which Controls an electronic Switch.

3 the Sampled Signal is stored as a Voltage on a Capacitor.



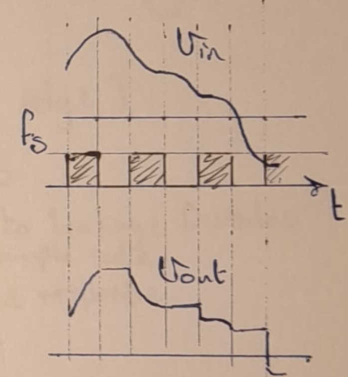
② Track and Hold

1 what We implement Practically is a T/H not a S/H

→ switch closed (ON): Track

→ Switch open (off): Hold.

2 although We refere to this Circuit as a S/H if we Want to implement a real S/H We Should Place two T/H Circuits in Series.



③ Tracking Band width.

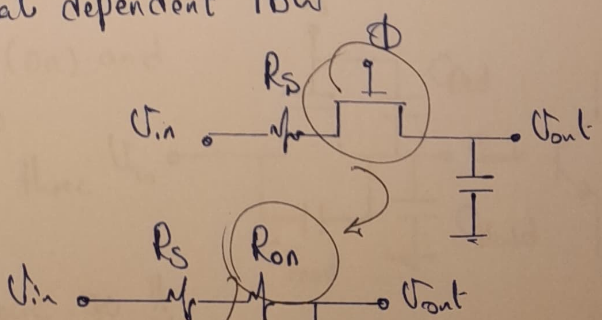
1 Mos techonology is naturally Suitable for implementing T/H

2 the Low pass network determines the tracking BW wich determines how Promptly Vout follow V_{in}

3 Single dependent on Ron → Signal dependent TBW

→ distortion ☹

not a Concern if TBW is Sufficiently Large (TBW >> f_{in})



$$R_{on}^{-1} = \mu C_{ox} \frac{W}{L} (V_{DD} - V_{TH} \pm V_{in})$$

④ T/H Speed _ Accuracy trade off

1 Short L → Large W → Large V_{ov} and Small V_{in} → reduce R_{on} → more Speed

2 But Large W and V_{ov} → Large Q_{ch} → Increase T/H error

∴ Less Accuracy ☹

$$\# \quad R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{DD} - V_{TH} - V_i)} = \frac{L^2}{\mu C_{ox} W L (V_{DD} - V_{TH} - V_i)}$$

$$= \frac{L^2}{\mu Q_{ch}}$$

$$\# \quad \tau = \frac{1}{TBW} = (R_s + R_{on})\, C_s$$

If We Want Large TBW We need Lower
- C_s : determined by noise
- R_s : by buffer but With High Power Cons.
- R_{on} : large W, Short L, Less accuracy.

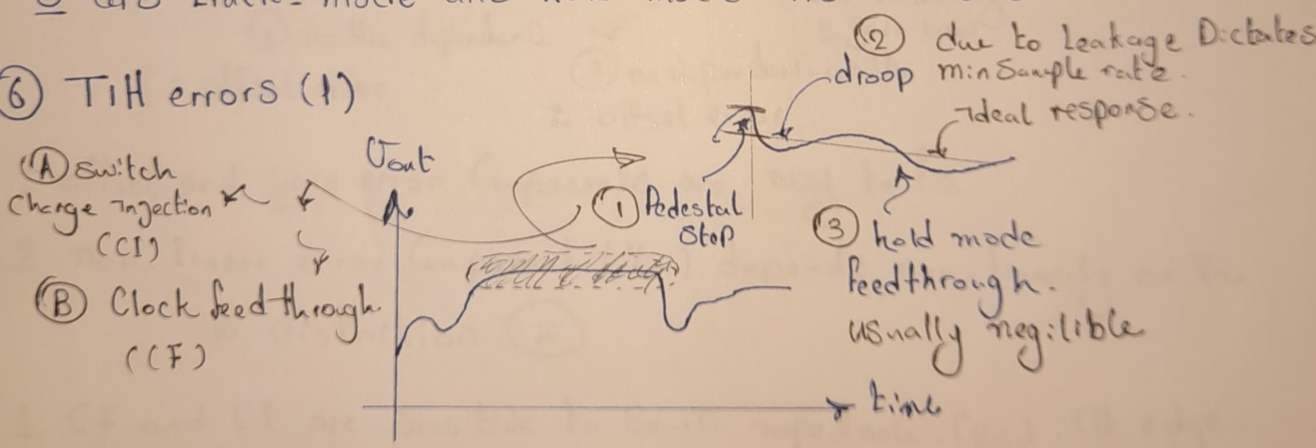
⑤ Ideal T/H

1 Sufficient TBW → negligible tracking error.

2 Well defined Sampling Instant (asserted by clk edge)

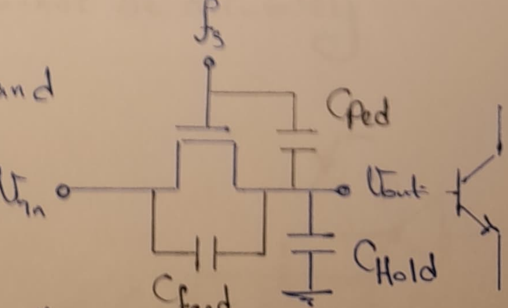
3 Zero track-mode and Hold mode offset errors

⑥ T/H errors (1)



1 Pedestal Step

A When f_s is (1) the Switch as (on) and Carry a Charge (Q_{ch}) and When f_s is (0) the Switch is (off) and there will be no Charge on it.

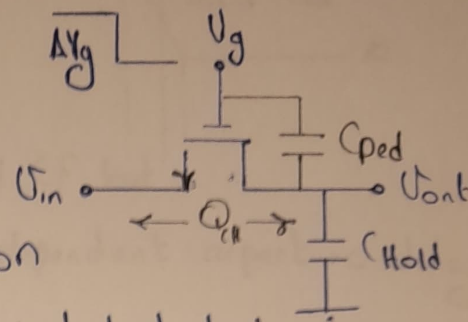


but Where the Charge go !!

It may go to C_{Hold} and make (ΔV) @ the Output $= \frac{Q_i}{C_{Hold}}$

B When fs goes from (1) to (0) the switch's Capacitances are Coupled to the output.

(7) T/H Pedestal Step.



Clock Feed through.

$$-\Delta V_{out_{CF}} = \frac{C_{ped}}{C_{ped}+C_{Hold}}\Delta V_g$$

$$= \frac{C_{ped}}{C_{Hold}}\Delta V_g$$

$$= \frac{W C_{olap} V_{DD}}{C_{Hold}}$$

Charge injection

- assume Q_{CH} is distributed equally in the two direction of switch

∴ $\frac{Q_{CH}}{2}$ goes to C_{Hold} : $\Delta V_{out_{CI}} = \frac{Q_{CH}/2}{C_{Hold}}$

$$= \frac{WL C_{ox}(V_{DD}-V_{in}-V_{TH})/2}{C_{Hold}}$$

$$V_{Ped} = \frac{W C_{olap} V_{DD} + WL C_{ox}(V_{DD} - V_{in} - V_{TH})/2}{C_{Hold}}$$

(1) no V_{in} dependance ∴ offset error

(2) no dependance on V_{in} ∴ offset error

(3) depend on V_{in} but Linearly ∴ gain error

(4) depend on V_{in} ∴ non-linearly

1 offset and gain error Components are easy to fix.

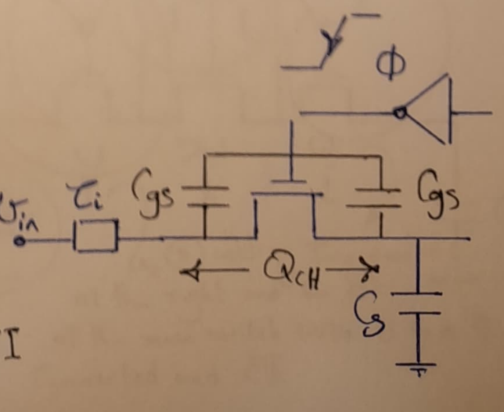
2 non-Linear error Component (V_T) depends non-linearly on V_{in} ∴ distortion ☹

3 CF and CI are Sensitive to Source impedance, C_{Hold}, Clk edge.

4 CF Can be Simulated by Spice, But CI Cannot be accurately Simulated with Lamped model.

(8) Pedestal step edge rate dependance

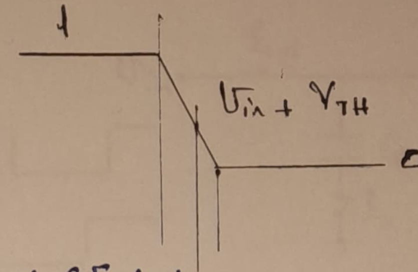
1 Fast turn off.



1 $\Delta V = -\frac{C_{gs}}{C_{gs}+C_s} V_{DD} \rightarrow CF$

2 $\Delta V = \frac{C_{ox} WL (V_{DD} - V_{TH} - V_i)}{2(C_{gs}+C_s)} \rightarrow CI$

2 Slow turn off



1 $\Delta V = \frac{C_{gs}}{C_{gs} + C_s}(V_{in} + V_{TH}) \rightarrow CF$

2 $\Delta V = 0 \rightarrow CI$

Although slow turn off is good for CI and CF but it's more sensitive to jitter and signal dependent aperture delay

⑨ T/H Speed Accuracy Trade off

- Technology scaling improves track and hold performance where.

1 Pedestal error: $\Delta V_{CI} = \frac{Q_{CH}}{2C_s}$

2 $TBW = \frac{1}{R_{on} C_s} = \frac{\mu Q_{CH}}{L^2 C_s}$

$\therefore \frac{\Delta V}{TBW} = \frac{\text{Error}}{\text{Speed}} = \frac{L^2}{2\mu}$ → as technology scalling reduce L $\therefore \frac{\Delta V}{TBW}$ enhanced.

We want it small.

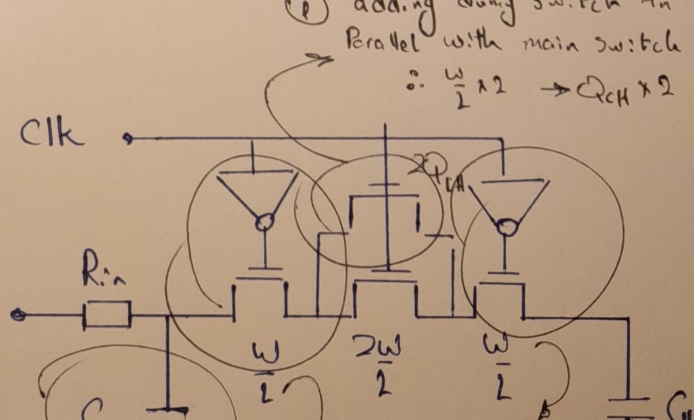
How to reduce S/H non-linearity !!

⑩ Dummy switches.

- adding dummy switches mitigates switch CI error by.

- when main switch turn on → off the dummies then turn off → on ∴ they need Q_{CH} which the main switch does not need it ∴ We ensure no Q_{CH} reaches C_s

- the CI dependance on Rin, CH and Clk make it difficult



① adding dummy switch in parallel with main switch $\therefore \frac{W}{2} \times 2 \rightarrow Q_{CH} \times 2$

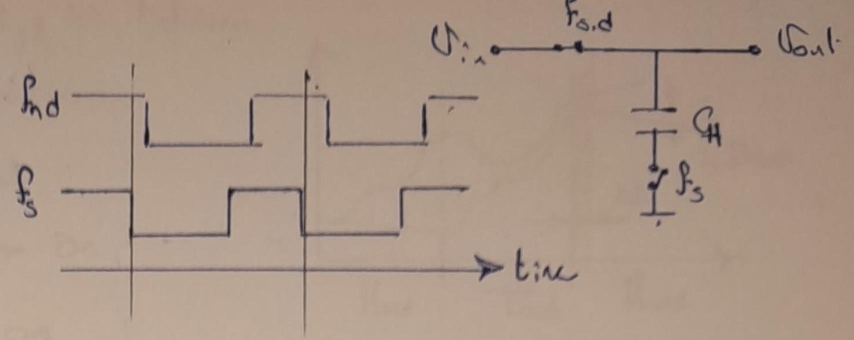
② adding two dummies at the right and the left of the main switch with S and D connected and $\overline{Clk}$

③ Cin ensures that the charge sees equal impedance at both sides ∴ split equally.

(11) Bottom plate Sampling.

- add another Switch at the bottom plate

  → the new Switch Charge injection is independent of V_{in}



→ No non-linear error → no distortion

→ Necessary for more than 8-bit resolution

- When the main switch turns from on → off the bottom plate switch will be already turned off

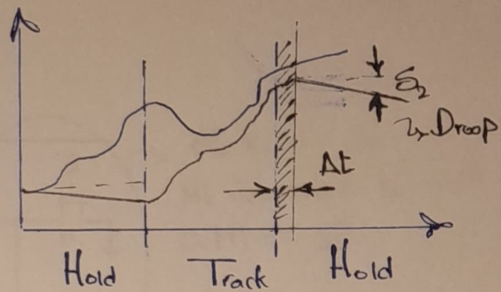
∴ no pass for Q_{CH} to the C_{Hold}

- note the Charge of bottom plate switch not depend on V_{in}

  ∴ not non-linear

(12) T/H errors (2)

1 Aperture delay: is the delay Δt between hold command and hold action.



$\because V_{GS} = \Phi - V_{Input}$

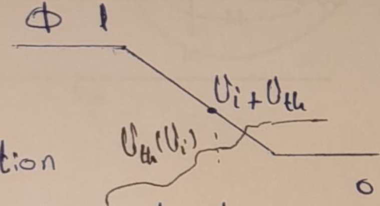
$\therefore \Phi - V_{in} > V_{TH} \rightarrow$ On

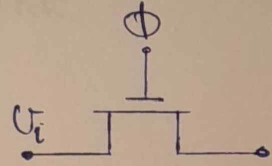
$\therefore \Phi > V_{TH} + V_{in} \rightarrow$ on

$\because$ device switch depends on V_i

$\therefore \Delta t = f(V_{in})$

$\therefore$ non-uniform sampling $\rightarrow$ distortion





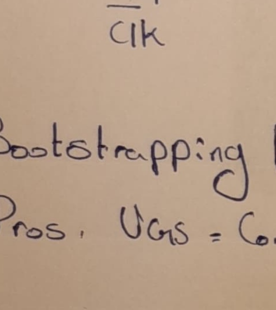
$\rightarrow$ Sharp clk edge and small V_{in} mitigate the delay variation

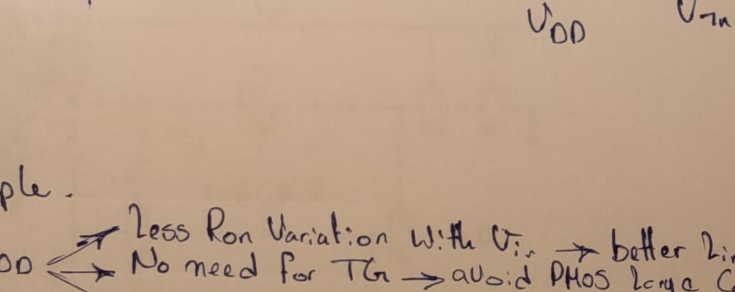
2 Aperture jitter is the random variation in Δt. It causes sample moment to shift position

(13) Transimission Gate (TG)

1 R_{on} (TBW) depends on V_{in} $\rightarrow$ can be reduced by using TG which may be indispensable for low voltage operation.

but delay mismatch between clk and $\overline{clk}$ cause distortion





(13) Bootstrapping Principle.

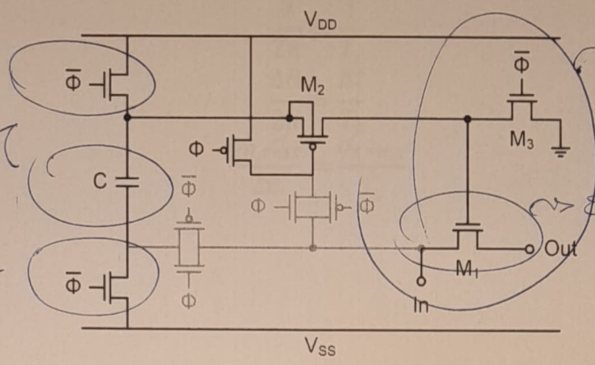
1 Pros. $V_{GS} = \text{Const} = V_{DD}$
- $\rightarrow$ Less R_{on} variation with V_{in} $\rightarrow$ better linearity
- $\rightarrow$ No need for TG $\rightarrow$ avoid PMOS large cap
- $\rightarrow$ use smaller NMOS switch $\rightarrow$ less clk loading.

2 Concept: instead of inserting Φ directly on switch we use charged cap with V_{DD} and connect it between S and G of the switch. $V_{GS} = V_{DD} = \text{Const} \neq f(V_{in})$

Page 7

Bootstrapping Example (1)

(1) ❑ Hold Mode: $\Phi = 0$
- C is precharged



ON

1 Charged with VDD

ON

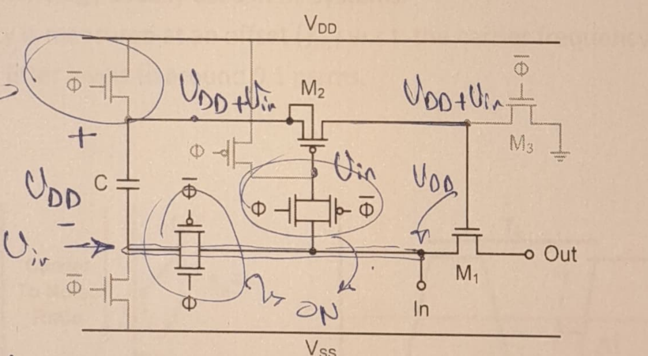
2 M3 is on So. M1 Connected to GND ∴ M1 is off

Sampling Switch

Bootstrapping Example (2)

❑ Track mode: $\Phi = 1$

(2)
- VGS = constant = VDD



VDD+Vin VDD+Vin

+ VDD −

Vin Vin VDD

ON

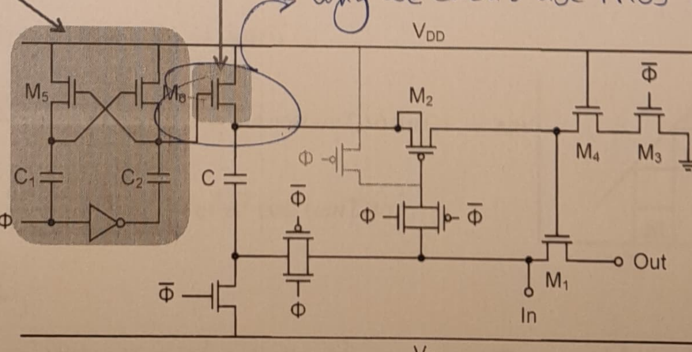
Assuming this device pass Strongly

Cons of Bootstrapping
1 Complex, Area, Power
2 Device reliability
3 Residual errors due to body effect

Bootstrapping Example (3)

❑ Charge pump to drive the NMOS switch with $V_G > V_{DD}$

Why we didn't use PMOS ??



Page 8

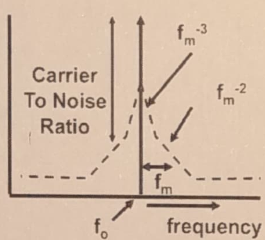
Jitter vs Phase Noise (1)

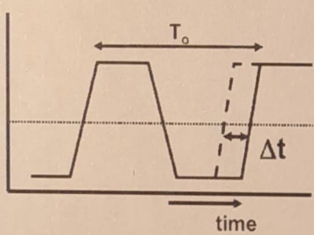
- Variations in time (jitter) is equivalent to variations in phase (phase noise)

$$V_S = V_o \sin(\omega_s t) = V_o \sin(\theta)$$
$$\theta = \omega_s t = 2\pi f_s t$$
$$\frac{\theta}{2\pi} = \frac{t}{T_s}$$
$$\frac{\Delta\theta}{2\pi} = \frac{\Delta t}{T_s}$$
$$\frac{\sigma_{\theta,rms}}{2\pi} = \frac{\sigma_{t,rms}}{T_s}$$

Jitter vs Phase Noise (2)

- Jitter in time domain is equivalent to Phase Noise in frequency domain.
- Jitter terminology usually used in sampled systems.
- Phase noise terminology usually used in RF systems.
  - Noise density is measured at an offset (f_m) w.r.t. the carrier frequency.
- BPF can reduce jitter levels to around 0.1 psrms.





Jitter Limited SNR (1)

- Timing variations means amplitude variations
- Jitter limits the max attainable SNR

$$A(nT_s + \Delta t(t)) = \hat{A}\sin(\omega \times (nT_s + \Delta t(t)))$$

$$\Delta A(nT_s) = \frac{d\hat{A}\sin(\omega t)}{dt} \times \Delta t(nT_s) = \omega \hat{A}\cos(\omega n T_s)\Delta t(nT_s)$$

$$\sigma_A^2(nT_s) = \left(\frac{dA(nT_s)}{dt}\right)^2 \sigma_t^2 = \omega^2 \hat{A}^2 \cos^2(\omega n T_s)\sigma_t^2$$

$$\sigma_A^2 = \frac{\omega^2 \hat{A}^2 \sigma_t^2}{2}$$

$$\mathrm{SNR} = \frac{P_{\mathrm{signal}}}{P_{\mathrm{jitter}}} = \frac{\hat{A}^2/2}{\sigma_A^2} = \left(\frac{1}{\omega\sigma_t}\right)^2 = \left(\frac{1}{2\pi f \sigma_t}\right)^2 \rightarrow \mathrm{SNR} = 20\log\left(\frac{1}{\omega\sigma_t}\right) = 20\log\left(\frac{1}{2\pi f \sigma_t}\right)$$