# Analog Integrated Circuits
## lec13: gm over ID Design methodology.

① The problem.

1 Since Berkeley Spice Simulator in 1970s → there's no major change in analog design flow!

2 Nano-meter transistor models are very Complex

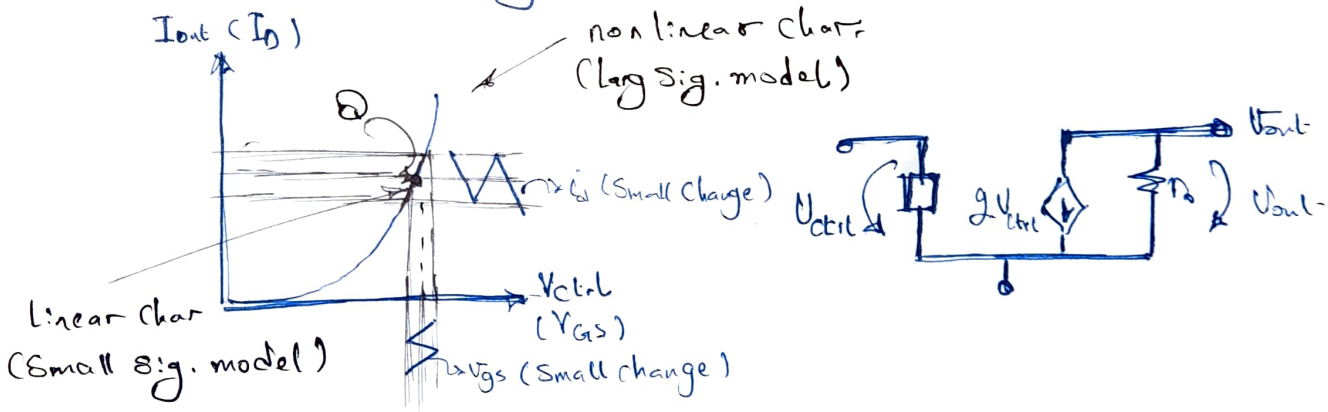
3 No Systematic analog design process

② Why is Transistor Different

1 The transistor is a three terminal device where the voltage between two terminals Controls the current flowing into the third terminal.

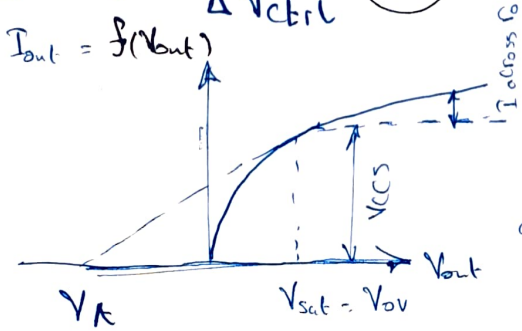
2 The transistor Works as VCCS

③ Transistor modeling




1 If there's Small Change in Vctrl it results a Small Change in Iout → this area assumed to be linear

∴ Slope $= \frac{\Delta I_{out}}{\Delta V_{ctrl}} = g_m$ → The transConductance of Transistor




2 as the VCCS of Transistor is not ideal → there will result an output resistance $r_o = \frac{V_{out}}{I_{out}}$

3 $r_o = \frac{1}{g_{ds}} = \left(\frac{\Delta I_{out}}{\Delta V_{out}}\right)^{-1} \simeq \frac{V_A}{I_Q}$

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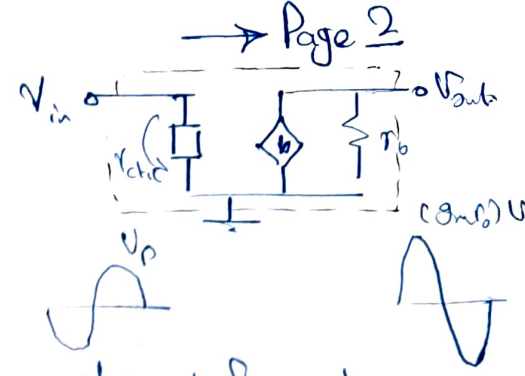
4 $V_{out} = -g_m V_{ctrl} \times r_o = -g_m V_{in} \times r_o$

$$|A_{v0}| = \frac{V_{out}}{V_{in}} = g_m r_o = \left|\frac{g_m}{I_Q}\right| V_A$$

Intrinsic



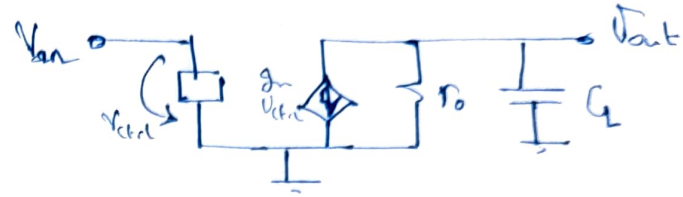

Intrinsic gain is the max gain can be achived from transistor

④ $g_m$ Controls the Speed.

$$\therefore A_v = \frac{V_{out}}{V_{in}} = g_m r_o$$

$$\because \tau = r_o C_L$$

$$\therefore BW = \frac{\omega_p}{2\pi} = \frac{1}{2\pi\tau} = \frac{1}{2\pi r_o C_L}$$




2 $GBW = |A_{v0}| . BW = f_u$ (for a single Pole Systems) $= \frac{g_m}{2\pi C_L}$

$\therefore$ $g_m$ Controls the speed of Amplifier

Speed ↑, $g_m$ ↑

⑤ $g_m$ Controls the Noise

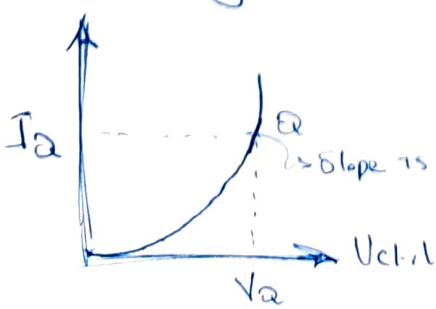
- We can show that for both MOSFET thermal noise and BJT shot noise

$$V_{n,in}^2(f) \propto \frac{1}{g_m}$$

$\therefore$ $g_m$ Controls the noise

Noise ↓, $g_m$ ↑

⑥ We must Pay $I_Q$ to Buy $g_m$




1 $\therefore$ Higher Slope → Higher $g_m$

$\therefore$ Higher $I_Q$ → Higher Power Cons.

2 $\therefore$ $g_m$ ↑, Speed ↑, Noise ↓, Power ↑ ☹

3 TE = Transistor efficiency = $\frac{\text{What you want}}{\text{what you pay}} = \frac{g_m}{I_Q}$ ☺ ☺

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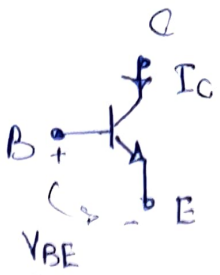
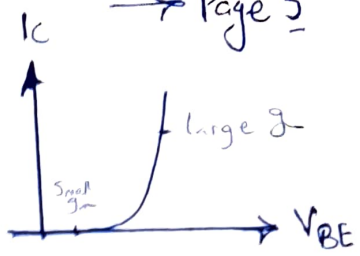
## ⑦ BJT story.

1. $I_C = I_S e^{\frac{V_{BE}}{V_T}}$

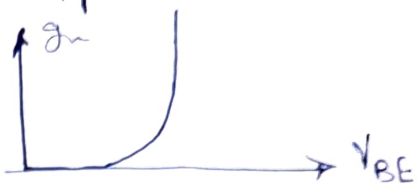
exponential characteristics




2. $\because g_m = \text{slope} = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{V_T}$ also exp

3. $\frac{g_m}{I_C} = \frac{1}{V_T} \approx \frac{1}{26\,mV} \approx 38.5\,S/A$




Constant (:o)

∴ no $\frac{g_m}{I_C}$ design methodology. ☺

4. The digital Prespective is

How much change in Vctrl ($V_{BE}$) for 10x change in $I_C$?

this spec called Subthreshold slope

$$(S) = \left(\frac{\partial \log_{10} I_C}{\partial V_{BE}}\right)^{-1} = \left(\frac{1}{2.3}\frac{g_m}{I_C}\right)^{-1} \approx 2.3\,V_T \approx 60\,\frac{mV}{dec}$$

5. BJT intrinsic gain

$$V_{out} = -g_m V_{ctrl} \times r_o = -g_m V_{in} \times r_o$$

$$|A_{vl}| = \frac{V_{out}}{V_{in}} = g_m r_o = g_m \cdot \frac{V_A}{I_C} = V_A \cdot \frac{g_m}{I_C}$$

$$\therefore |A_{vl}| = \frac{V_A}{V_T} = \text{Const}$$

## ⑧ The old school MOSFET

1. N-type channel region (inversion layer) formed @

$$V_{GS} > V_{TH} \rightarrow V_{GS} = V_{TH} + V_{ov}$$

2. The channel is Pinched off if $V_{GD} \le V_{TH} \leftrightarrow V_{DS} \ge V_{ov}$

3. The Simple long channel model is $I_D = \frac{\mu C_{ox}}{2}\frac{W}{L} V_{ov}^2 = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2$

4 There's a large division between Square-Law and actual characteristics for short channel devices.

5 Short Channel Effects

↳ Velocity Saturation → $I_D$ has linear dependance on $V_{GS}$
→ $I_D$ has no (or weak) dependance on L

↳ mobility degradation

∴ $g_m = \frac{\partial I_D}{\partial V_{GS}}$ is linear at large $V_{ov}$ = Constant @ Large $V_{ov}$

6 The Square law fails to describe Strong-inversion (SI) accurately ☹

7 The Square law fails to describe Weak-inversion (WI) Completely 😐

8 $g_m/I_D$ depends on bias point → large in WI
→ small in SI

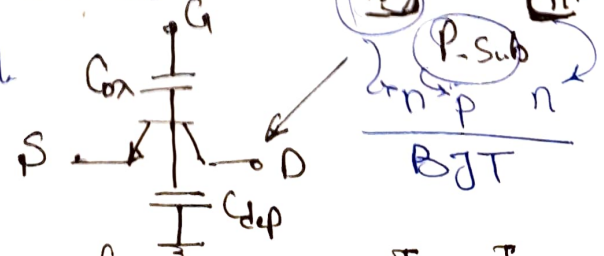
∴ Tuning MOSFET $\frac{g_m}{I_D}$ is the core of $\frac{g_m}{I_D}$ design methodology. 🙂

9 Since $\frac{g_m}{I_D}$ saturates in (WI) we expect $I_D$ characteristics is exponentially dependance on $V_{GS}$
Similar to BJT ☹

⑨ The Subthreshold Operation (Weak inversion)

1 In Weak inversion we still have the depletion region

∴ MOS Structure will be




2 MOS behave as BJT with its base coupled to the gate through capacitive divider

$V_{BE} = V_{GS}\frac{C_{ox}}{C_{ox}+C_{dep}} = \frac{V_{GS}}{n}$ → $n = \frac{C_{ox}+C_{dep}}{C_{ox}} > 1$ → $I_D = I_{off}\, e^{\frac{V_{GS}}{nV_T}}$

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3 MOS intrinsic Gain

$|A_{v1}| = g_m r_o = \frac{g_m}{I_D} \cdot V_A \quad r_o = f(L)$

↑ higher $\frac{g_m}{I_D}$ higher $|A_{v1}|$

until!!

Subthreshold region where $\frac{g_m}{I_D}$ Saturate ☹

4 Operation in WI → max Ai ☺

→ $I_D$ exp ↓ → $g_m$ exp ↓ → $f_u$ exp ↓ ☹

→ to keep same $I_D$ and $g_m$ → W exp ↑ → Area exp ↑ ☹

(heat Area ↑, Parasitics ↑, $f_u$ ↓ again ☹)

## (10) Operation in MI

1 Operation in MI is becoming increasingly Popular where, we can reap WI benefits

High $\frac{g_m}{I_D}$ High $\frac{g_m}{g_{ds}}$

Some degradation in speed is ok where the short channel MOS are already fast

2 In MI no simple model exists ☹ !!

## (11) MOS Design Problem.

*MOS is a function of five param

- $V_{GS}$ → $V_{CCS}$
- $V_{DS}$ → $r_o$
- $V_{SB}$ → $V_{TH}$
- L → Speed
- W → $I_D$ given all Voltage const

1 $V_{SB}$: increasing $V_{SB}$ increase $V_{TH}$

usually $V_{SB}$ is not a designer DOF

it's imposed by circuit topology.

2 $V_{DS}$ → Ideally $V_{DS}$ should not affect $I_D$

∴ MOS is a VCCS for $V_{DS} > V_{Dsat}$

- But practically increasing $V_{DS}$ increases $I_D$ → CLM, DIBL
- $V_{DS}$ effect modeled by $r_o = \frac{V_A}{I_D}$
- $V_{DS}$ ↑, $V_A$ ↑, $r_o$ ↑ as we go deeper into Sat.
- We need Large $V_{DS}$ (much larger than) $V_{DSat}$ to notice the difference of $V_A$ ($r_o$)

- $V_{DSat}$ and $V^*$

For the Square law

$$\frac{g_m}{I_D} = \frac{2}{V_{ov}} \rightarrow V_{ov} = \frac{2}{g_m/I_D}$$

We define new Param inspired by Vov

$$V^* = \frac{2}{g_m/I_D}$$ Computed from Simulation

So → it's valid in all region

- $V^*$ is always larger than $V_{Dsat}$ ☺ So it can be used as an estimate for saturation
- It's gurantee biasing a littel deeper into Sat

$V_{DS}$ is set to $V^* + V_{DSat\_margin}$

3 $V_{GS}$ is the primary Voltage Controlling the device behaviour

- So $V_{GS}$ is the primary Voltage Controling $I_D$ (VCCS)
- In analog ICs, we usually Set the bias Current rather than Setting the bias Voltage ($V_{GS}$) → Current mirror biasing
  ∴ replace $V_{GS}$ by $I_D$ in the DOFs list

4 Length (L)

- shorter L allows smaller area and higher speed
- but analog designers usually tend to use relatively long L

use shorter L if you want

1 Smaller Area → Smaller Cap

2 High Speed (high $f_T = \frac{g_m}{2\pi C_{gg}}$)

use longer L if you want

1 High gain (high $V_A$)

* Must have large $V_{OST}$ margin

2 less random mismatch

3 low flicker noise

5 Width (W)

- Choosing W is one of the most difficult tasks
- the Choice of W is affected by
  - How much $\frac{g_m}{I_D}$ do you want
  - How much L do you use
  - How much $I_D$ do you force
- the Search range of W is very large.
- The meaningful Search range depends on $\frac{g_m}{I_D}$, L, and $I_D$

(12) The $g_m/I_D$ design methodology.

1 What we care most about is the (TE) on $\frac{g_m}{I_D}$ where $g_m$ captures the relation between the basic function $I_D$ of the transistor ($g_m$) and the most valuable resource (Power Consumption $I_D$)

Replace W by $\frac{g_m}{I_D}$ in the DoFs

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# Think gm/ID!

| Use small gm/ID if you want | Use large gm/ID if you want |
|---|---|
| ➢ Strong-inversion (SI) biasing<br>➢ Small gm (for a given ID)<br>▪ Devices whose gm do NOT contribute to gain (Ex: active loads)<br>➢ Small area<br>➢ Small capacitance<br>➢ High speed<br>➢ Large $V_A$ (large ro)<br>▪ The gate has better control on channel (VDS effect is less) | ➢ Moderate inversion (MI) or weak-inversion (WI) biasing<br>➢ Large gm (for a given ID)<br>▪ Devices whose gm do contribute to gain (Ex: input stage and cascode devices)<br>➢ High efficiency<br>▪ Low power consumption (low ID) for a given speed or noise spec (gm spec)<br>➢ Less random mismatch<br>▪ Large gm/ID implies larger W (larger area) (beware of exceptions due to non-uniform doping profile)<br>➢ Low flicker noise<br>▪ Large gm/ID implies larger W (larger area)<br>➢ Large input range and/or output swing<br>▪ Large gm/ID implies small V* |

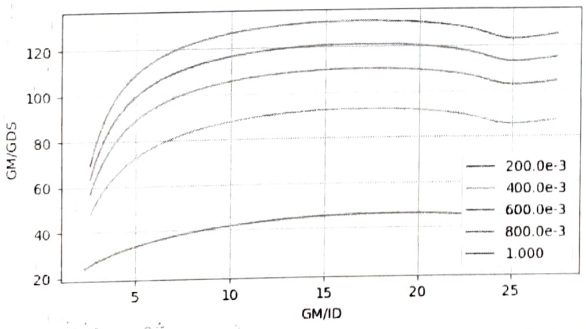


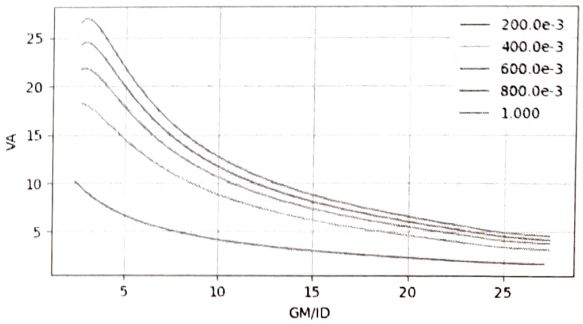
# gm/ID and Gain

$$g_m r_o = \frac{g_m}{I_D} \cdot V_A$$

- For high intrinsic gain go for high gm/ID
- But beware that $V_A$ (and consequently $r_o$) decreases as you go in WI
  - The gate has less control in WI
  - The effect of VDS on ID increases

($g_m \cdot r_o$) Saturate



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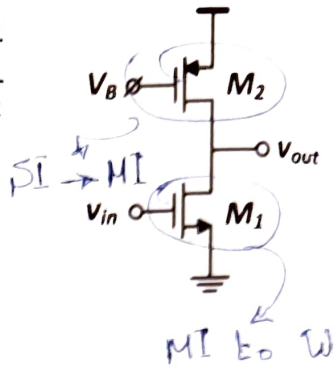
# gm/ID and Gain

$$|A_v| = g_{m1}(r_{o1}||r_{o2}) = \frac{g_{m1}}{g_{ds1}+g_{ds2}} = \frac{(g_m/I_D)_1}{\frac{1}{V_{A1}}+\frac{1}{V_{A2}}}$$




SI → MI

- From gain perspective
  - A large gm/ID may be good for M1
  - But a small gm/ID is better for M2 (higher $V_{A2}$)

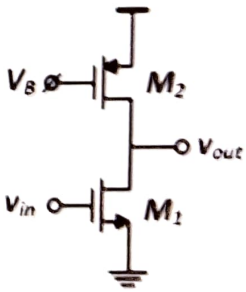
MI to WI

- Generally, from gain perspective
  - Use large gm/ID for transistors whose $g_m$ contribute to the gain
    - Ex: input stage and cascode devices
  - Use small gm/ID for transistors whose $g_m$ do not contribute to gain
    - Ex: active loads



# gm/ID and Thermal Noise

$$v_{n,in}^2(f) \approx \frac{4kT\gamma}{g_{m1}}\left(1+\frac{g_{m2}}{g_{m1}}\right)$$




- From noise perspective
  - A large gm/ID is good for M1
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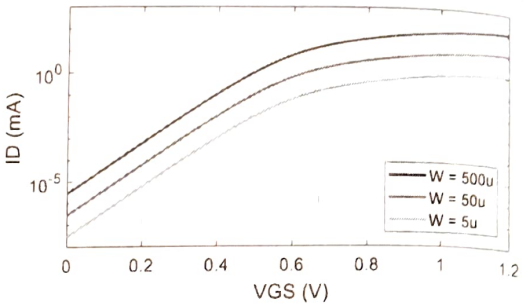
- Generally, from noise perspective
  - Use large gm/ID for transistors whose $g_m$ contribute to gain
    - Ex: input stage and cascode devices
  - Use small gm/Id for transistors whose $g_m$ do not contribute to gain
    - Ex: active loads

# From gm/ID to W

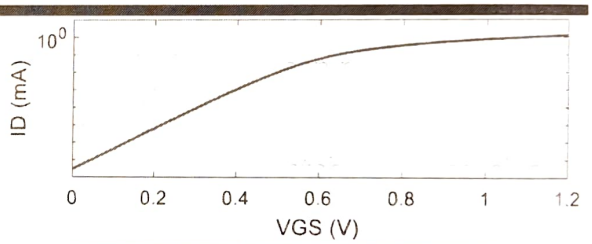
- The problem is that you cannot plugin gm/ID in the simulator
  - Side note: you can directly plugin gm/ID in the Analog Designer's Toolbox (ADT) ☺
- The good news is that ID is always proportional to W: $I_D \propto W$
  - This holds for both long and short channel devices
  - This holds for all operating regions (WI, MI, SI)
  - Simply, the wider the street (the channel) the more cars (electrons) can pass
- The exception is narrow-width devices
  - But they are seldom used in analog as they will have excessive mismatch and excessive flicker noise

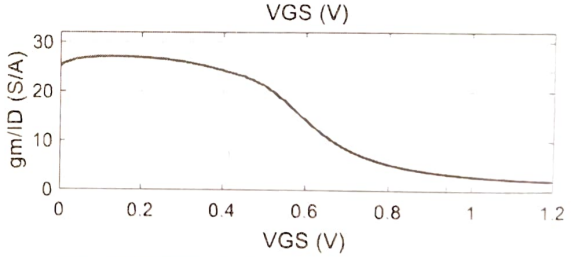


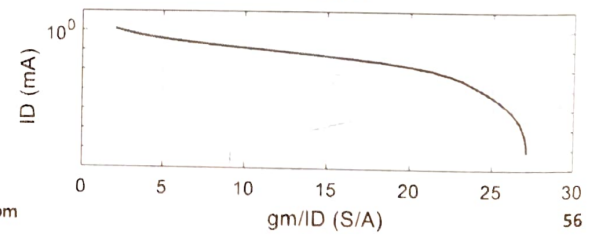



# From gm/ID to W

- Assume a reference device with Width = W
- For a given L, there is one-to-one correspondence between VGS and ID
- And there is one-to-one correspondence between gm/ID and VGS
  - Points to the left of the max gm/ID are discarded
- Thus, there is one-to-one correspondence between gm/ID and ID
- Similarly, we can plot any other parameter vs gm/ID



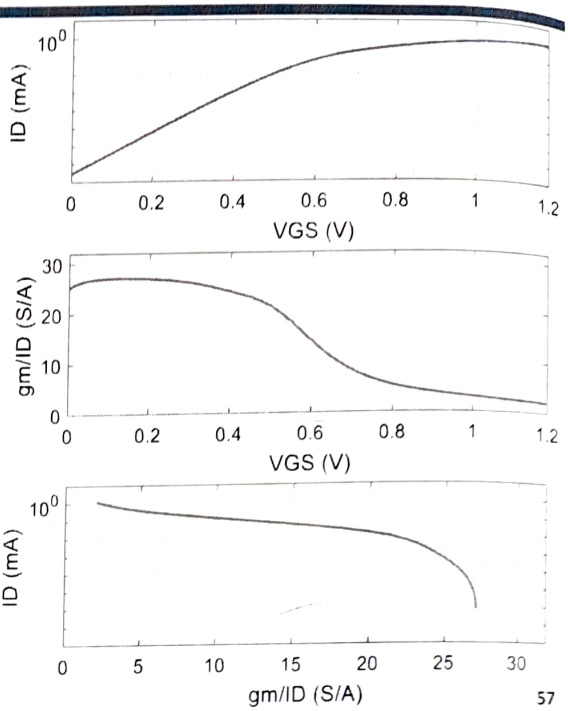
# From gm/ID to W

$$I_D \propto W$$

- Apply cross multiplication

| Ref Device | ID (from chart or look-up table) | W (reference device width) |
|---|---|---|
| Design Problem | IDx (defined in problem DOFs) | Wx = ? |

$$W_x = W \times \frac{I_{Dx}}{I_D}$$






# Recapping MOSFET DOFs

| Original | The Old-School | The gm/ID Methodology |
|---|---|---|
| W | Vov (square law) | gm/ID (use charts or LUTs to get W) |
| L | L (get a rough estimate for $V_A = 1/\lambda$) | L (use charts or LUTs) |
| VGS | ID (current mirror biasing) | ID (current mirror biasing) |
| VDS | VDS = Vov + VDsat_margin (get a rough estimate for VDsat_margin) | VDS = VDsat + VDsat_margin (taken into account by using charts or LUTs) |
| VSB | Forced by topology (use simple model or ignore) | Forced by topology (taken into account by using charts or LUTs) |