Analog Integrated Systems Design

Switched Capacitor Circuits

Assignment No. 5

Lab Objective

1) To be able to model a fully differential amplifier.

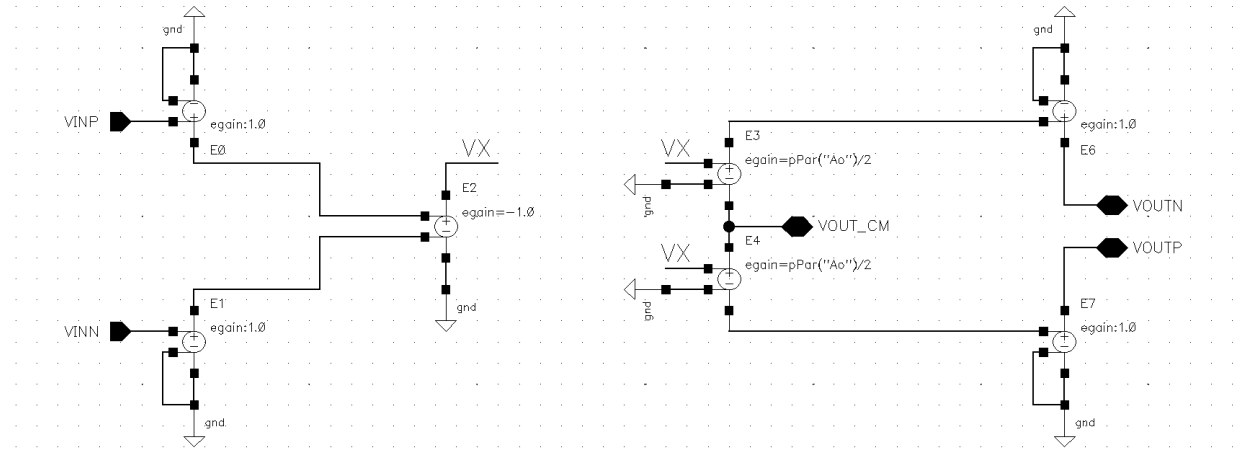
2) To be familiar with the operation of a fully differential switched cap amplifier.

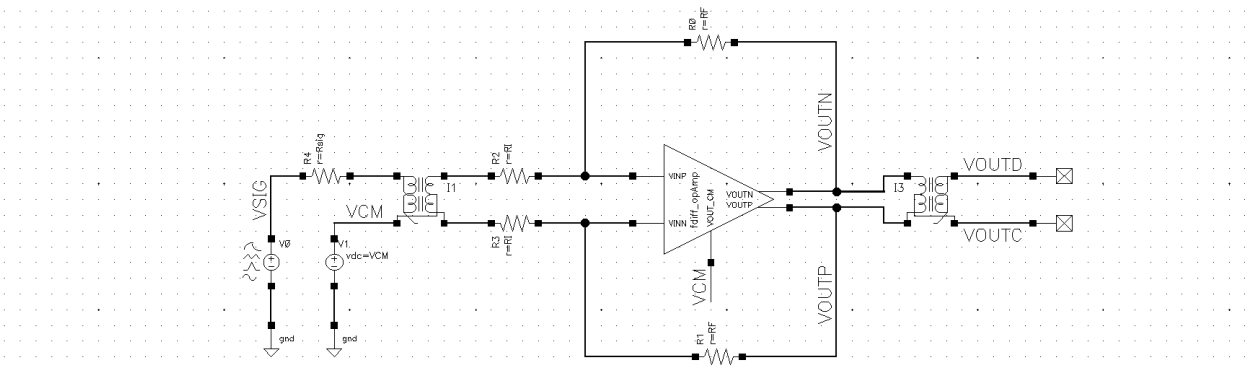
3) To be familiar wit the operation of a fully differential switched cap integrator.

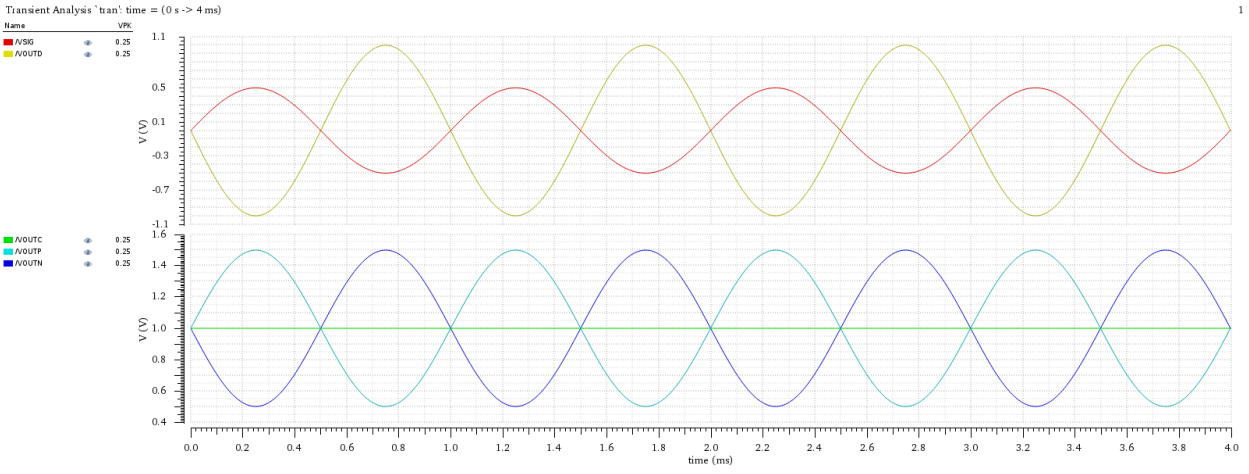
4) To be familiar with Periodic Steady State (PSS) and Periodic AC (PAC) analyses.

Part 01 - Fully Differential Op-amp Behavioral Model

1. Create the schematic shown below to model a fully differential op-amp with finite gain, finite input range, and finite output range. Use vcvs from analogLib.
2. Create a new symbol
3. Create a simple testbench to verify your fully differential op-amp. An example testbench is shown below.
4. Run transient analysis



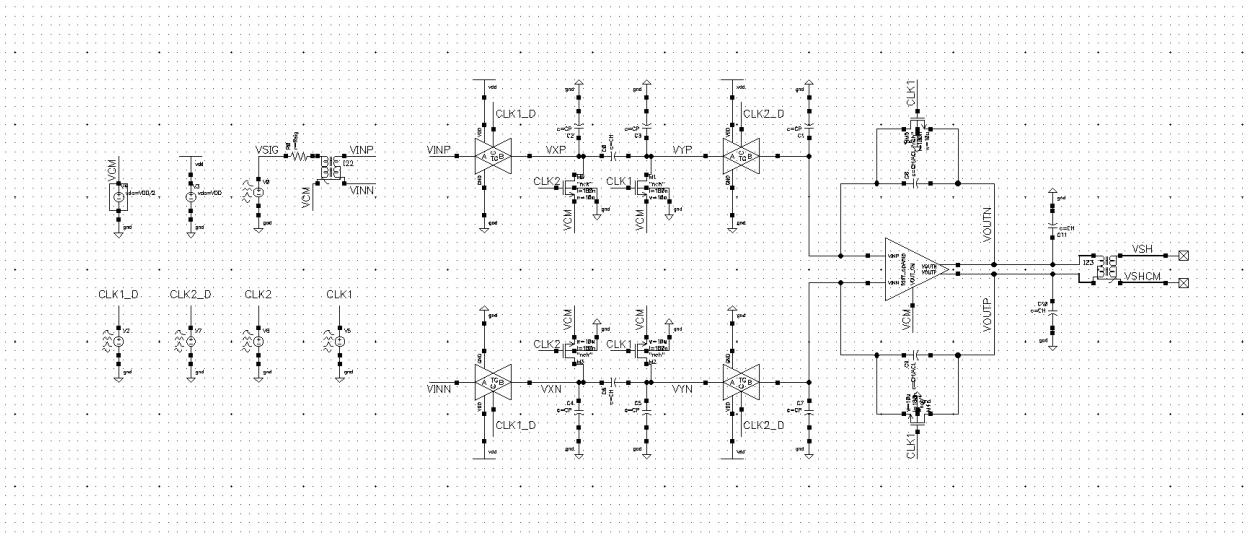


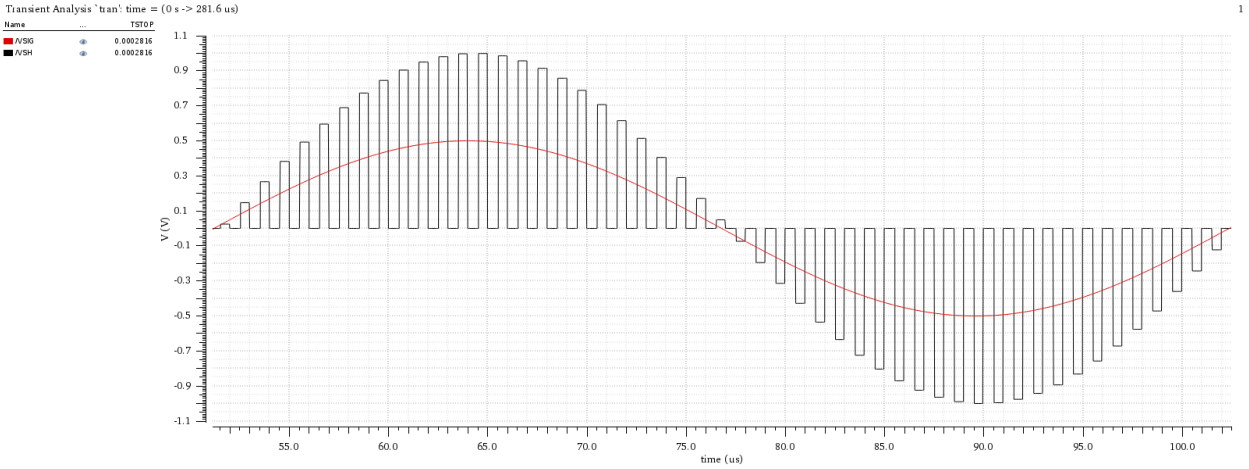


Part 02 - Fully Differential Switched Capacitor Amplifier

1. Create a testbench for a fully differential switched cap amplifier as shown below. This is an example of a sample and hold amplifier (it samples the signal and multiplies it by 2).
2. Set signals as following
3. Run transient analysis

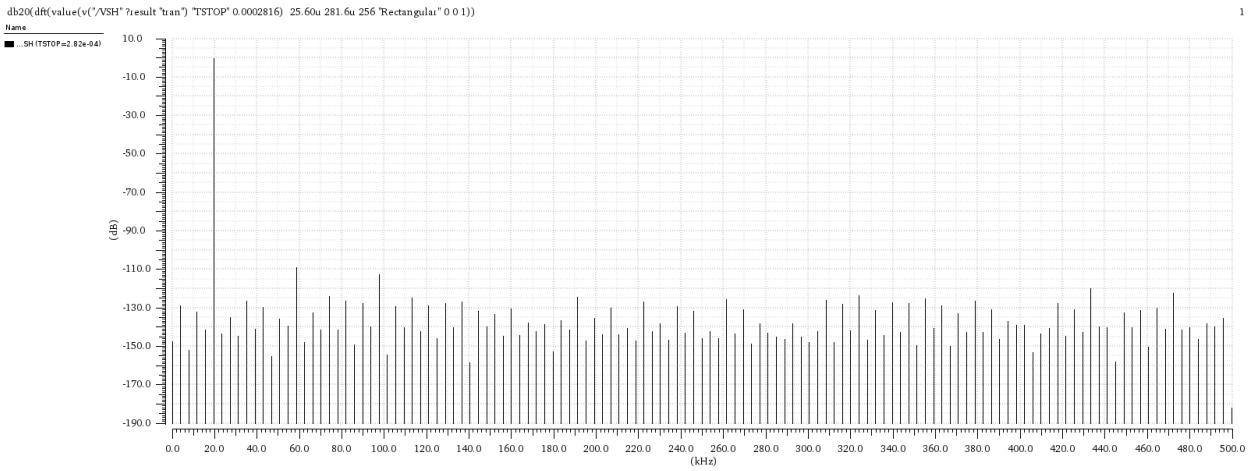
	CLK1	CLK1_D	CLK2	CLK2_D
Type	PULSE	PULSE	PULSE	PULSE
Initial Value	0	0	0	0
Pulse Value	VDD	VDD	VDD	VDD
Period	TS	TS	TS	TS
Pulse Width	TON	TON	TON	TON
Delay	0	0.1*TON	0.5*TS	0.5*TS+0.1*TON
Rise/Fall Time	TRF	TRF	TRF	TRF





4. Use the Spectrum Assistant to plot FFT for the differential output. Report the following results.

ENOB	17.246 bits
SINAD	105.585 dB
SNR	110.357 dB
SFDR	108.739 dB
THD (in dB)	-107.26 dB
Signal power	-0.0008 dB
DC power	-147.57 dB

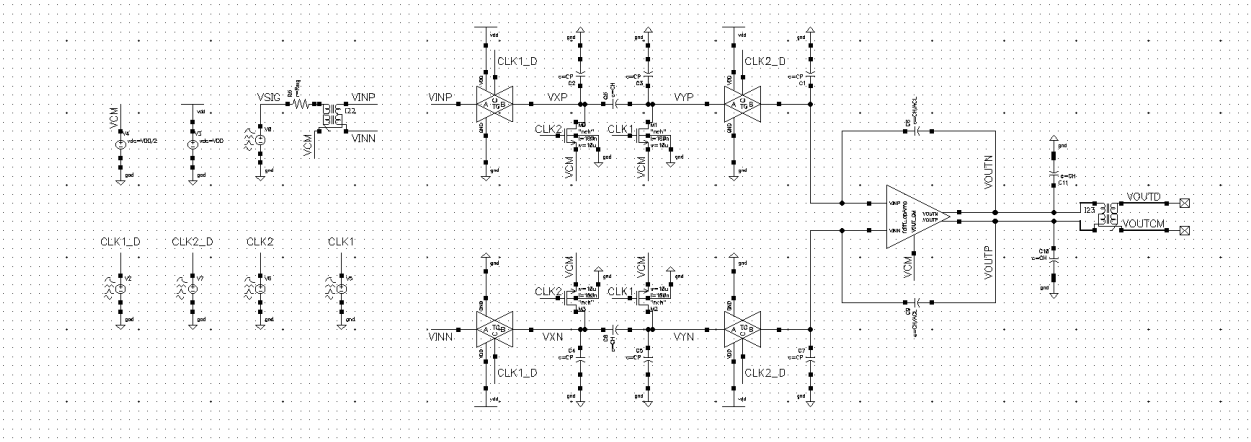


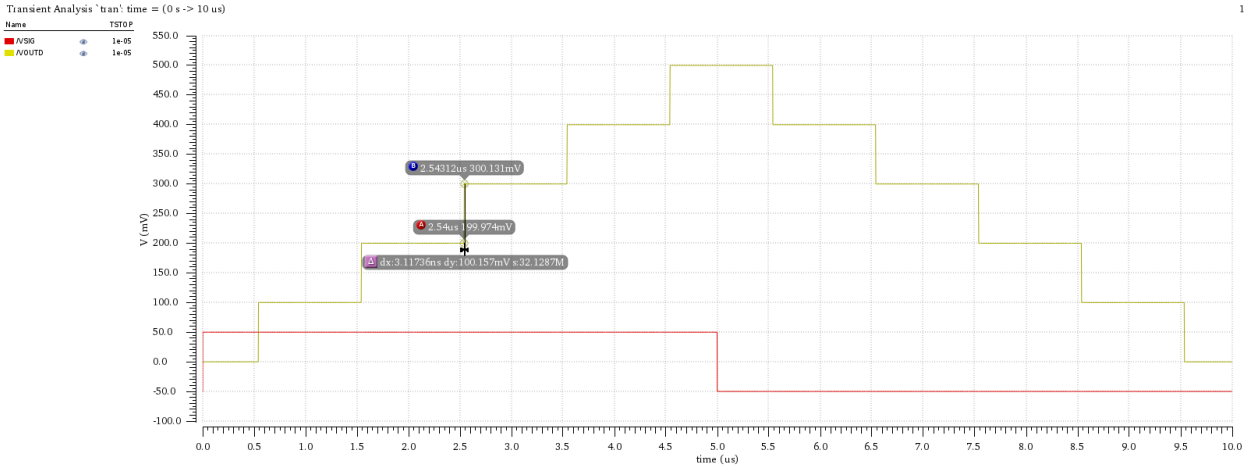
Part 03 - Fully Differential Switched Capacitor Integrator

1. Copy the previous cell to a new cell. Remove the reset switch that was used across the feedback capacitors. The circuit now acts as a switched capacitor integrator. The modified circuit schematic is shown below.
2. Modify the input signal to a be a pulse source with the properties shown below.

Type	Pulse	Period	2* NP*TS
Initial (one) value	VPK	Pulse width	NP*TS
Pulse (zero) value	-VPK	Rise/fall time	TRF

3. Run transient analysis for VAR("TSTOP"). Plot VSIG and VOUTD.
   a. What is the relation between input and output waveforms?
      Vout (n) = Vout(n - 1) + Vin(n - 1) * A_{CL}
   b. What is the value of each voltage step in the output waveform? Why?
      100 mV, Vout (n) = Vout(n - 1) * A_{CL} = 2 * 50 mV = 100 mV

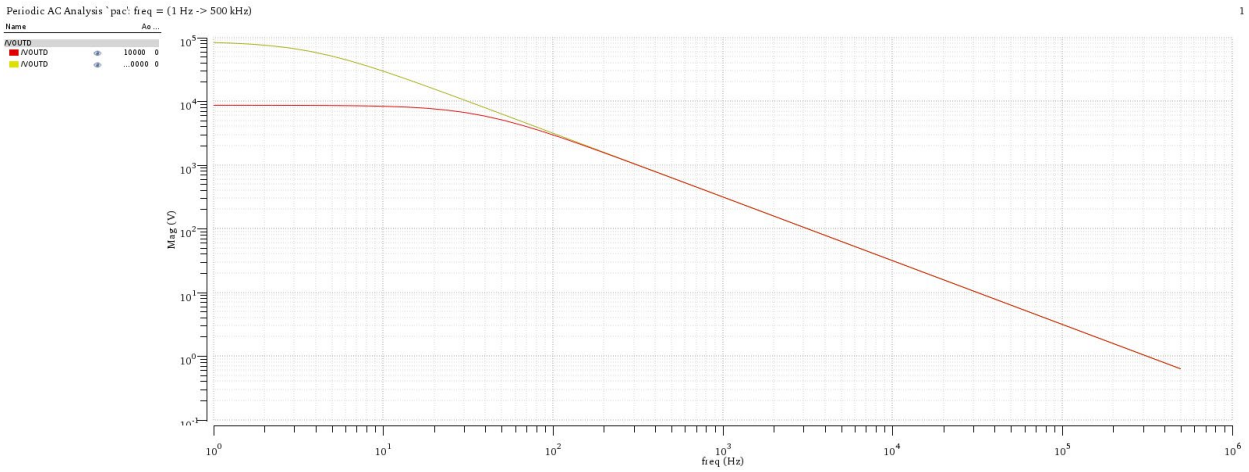




Part 04 - Periodic Steady State (PSS) and Periodic AC (PAC) Analyses

In this part we would like to plot the frequency response of the switched capacitor integrator. Note that a switched cap circuit is a linear circuits (doubling the input doubles the output), but it is time variant (not an LTI system). Since the behavior of the circuit changes with time according to the clock signal, it is not possible to use normal ac analysis. The circuit doesn't have an operating point (dc steady state), but the clock signal which changes the circuit state is periodic (periodic steady state). A specialized type of analysis name periodic steady state (PSS) is used to analyze such type of circuits. PSS can be followed by other types of analysis such as PAC (periodic equivalent of ac analysis) and pnoise (periodic equivalent of noise analysis)

1. Run the simulation. Use the Direct Plot Form to plot the integrator ac response (VOUTD vs frequency). Use log-scale for both x and y axes.
   a. What is the type of the frequency response (LPF, HPF, BPF)? Why?
      LPF, because $H(z) = \frac{C_1}{C_2}\frac{1}{z-1}$ which equivalent to LPF
   b. Does the gain of the transfer function saturate? At what value? Why?
      Yes, at the Ao value, Saturation occurs because the OpAmp not ideal enough as Ao not equal ∞



[2] Note that the continuous time equivalent output is $v_{out}(t) = \frac{A_{CL}}{T_S}\int v_{in}(t)dt$. Convert to s-domain and take the magnitude: $|v_{out}(f)| = \left|\frac{A_{CL}}{T_S \cdot 2\pi f}\right|$.