Analog Integrated Circuits.

Lec22: Veriability and mismatch.

① Introduction to PVT Variations.

1. Variations → Manufacturing Variations. : Process Variations.
   → Environmental Variations: Voltage and temperature Vars
2. PVT → Voltage, → Temperature, → Process
3. Veriability is a random process moduled using a stastical distribution.
4. Statistical distribution Can be
   - → Uniform distribution
   - → Normal (Gaussian) distribution.

② Process Variations.

1. Variations happens due to tolerance and noise in the machines during the manufacturing.
2. Examples.

A) Threshold Voltage.

- V_{TH} Value depend on dopant Consentration at the channel "gate" region
- We Can not Controls the dopant Consentration Presise so: due to random dopant fluctuation "RDF" there will be Variations in the V_{TH} Value.

B) Channel Length.

- Variations in Channel Length L depends on.
  1. Lithography Limitations.
  2. Varying etch rates.
  3. Line edge roughness.

3. Binning: means Faster Parts are rated for higher frequency and Sold for more money.

③ Normal "Gaussian" distribution.

1. 68, 95, 99.7 rule.
2. 3 Sigma range is usually acceptable.
3. Components replicated millions of times (e.g., memory cells) are designed to tolerated 5:7 Sigma Variations.

④ Voltage Variations.

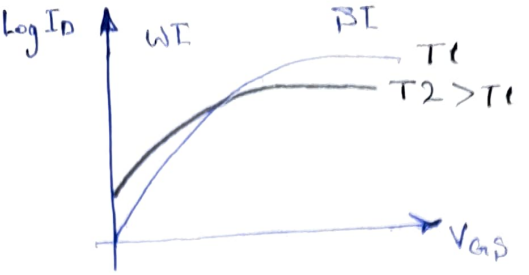
1. Supply Voltage may vary around its nominal value
   - Regulated tolerances.
   - IR drops
   - $L * \frac{di}{dt}$ noise
2. Voltage Varies in both space "across chip" and "time"
3. Typically tolerance to 1. Variation.
4. Usually assume Uniform distribution for Voltage Variations

$$V_{DD} = V_{DD_{nom}} \pm \Delta V_{DD}$$

⑤ Temperature Variations.

1. Ambient ranges.
   - → Commercial: 0:70°C
   - → Industrial: -40:85°C
   - → Military: -55:125°C
2. Junction temperature may significantly exceed the ambient
   ↳ Commercial parts commonly verified at 125 Junction temp.
3. temperature Varies in both space: across chip and time
   - ↳ Circuits in a 1mm diameter see nearly the same temperature
   - ↳ Temperature Varies in time on scale of milliseconds.

4. Drain Current in WI (SI) increases (decreases) with temp.

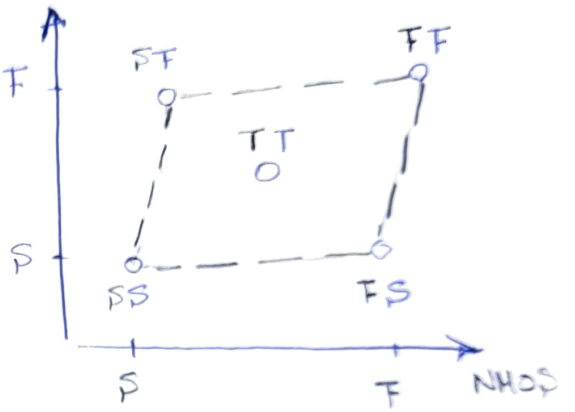


⑥ Design Corners.

1. MOS → Slow (S)
   → Typical/nominal (T)
   → Fast (F)

2. Voltage → 0.9 V_{DD} (S)
   → V_{DD} (T)
   → 1.1 V_{DD} (F)

3. Temperature → 125°C (S)
   → 70°C (T)
   → 0°C (F)



4. For old technologies we had Small number of Corners.
5. For DSM technologies we have Large number "May be thousand" of Corners.
   ↳ need to experiance so that you can identify the important Corners.

⑦ Monte-Carlo Simulations.

1. the Worst-Case Corners can be Too Pessimistic for Practical design
   ↳ Lead to using unnecessary excessive design margins
   ↳ results in performance degradation
2. Monte-Carlo generates the statistical dis of the Variations
   ↳ Repeated Simulations with Parameters randomly Varied each time

↳ the design margins can be adjusted depending on the required yield

3. yield (Y) is the fraction of manufactured chips that are opertional or that works according to the specification
   - ↳ Can tolerate one-sigma: Y = 68%.
   - ↳ Can tolerate two-sigma: Y = 95%.

(8) Process Variation Classification

1. Lot-to-Lot: a group of wafers can be vary from other groups.
2. (L2L extremes) Process Corners are Very Pessimistic
3. Wafer to Wafer (W2W) → from the same Lot
4. Die-to-die (D2D) → Inter-die
5. Within-die → Intra-die "mismatch"
6. Within-die Variations (WID) are what really matters for most of analog designs.
7. mismatch → modeled using Pelgrom's model
   → Simulated using monte-Carlo Simulation

(9) Pelgrom's mismatch model

1. the standard deviation of random Within die (WID) Variations is inversely proportional to square root of the transistor area (WL)
2. this makes sens intuitively because Variations tend to average out over a larger area.

$$\sigma_{V_{TH}} = \frac{A_{V_{TH}}}{\sqrt{WL}} \quad , \quad \frac{\sigma_{\Delta\beta}}{\beta} = \frac{A_\beta}{\sqrt{WL}} \xrightarrow{\beta = \mu C_{ox} \frac{W}{L}}$$

- $A_{V_{TH}}$ and A_β are Constants (Pelgrom's Coeff) ↳ determined by foundry by experimental measurements.
- $A_{V_{TH}} \sim 2-5\ mV.\mu m$
- $A_\beta \sim 1-2\ \%.\mu m$

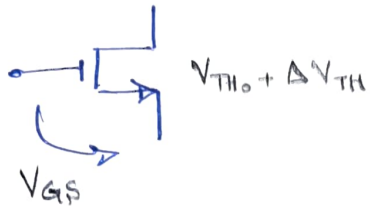
(10) Mismatch in Amplifiers: offset Voltage

1. Mismatch Circuit model.

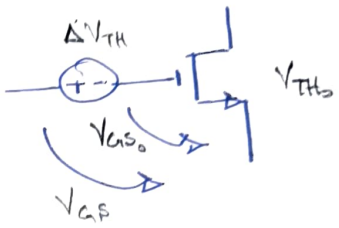
* The most important effects in MOS device is V_{TH} mismatch
  - V_{TH} is a function of doping levels in the channel.
  - These Levels Vary randomly from one device to another
* Variation in V_{TH} can be modeled by a dc source at the gate
  - ΔV_{TH} is a random Variable with

$$\sigma_{V_{TH}} = \frac{A_{V_{TH}}}{\sqrt{WL}}$$

$$V_{OV} = V_{GS} - V_{TH_0} - \Delta V_{TH}$$

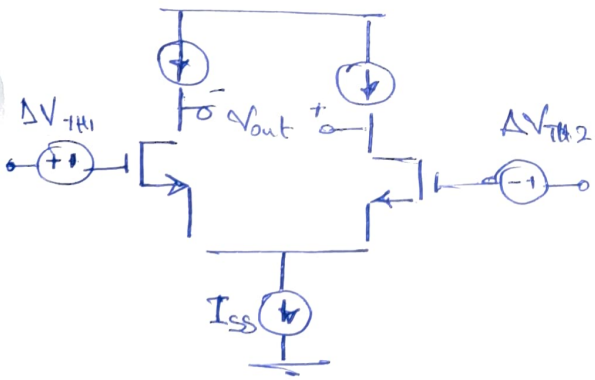


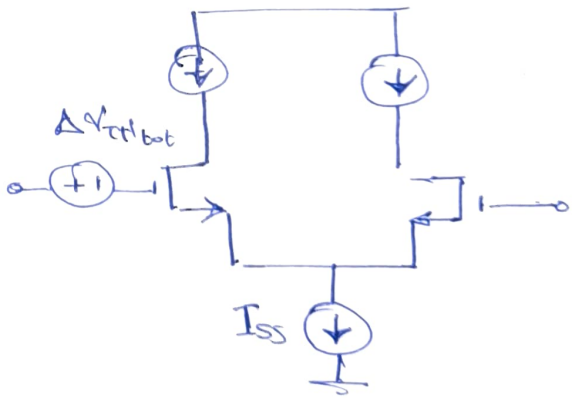
$$V_{OV} = V_{GS_0} - V_{TH_0}$$
$$= V_{GS} - V_{TH_0} - \Delta V_{TH}$$



2. Mismatch in diff_pair

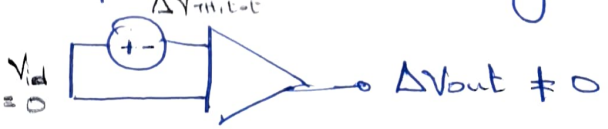
* ΔV_{TH} is a random Variable with $\sigma_{V_{TH}} = \frac{A_{V_{TH}}}{\sqrt{WL}}$
* $\sigma(V_{TH,tot}) = \sqrt{\sigma^2_{V_{TH1}} + \sigma^2_{V_{TH2}}} = \sqrt{2}\,\sigma_{V_{TH}} = V_{OS}$





(11) Offset Voltage

1. With $V_{id} = 0$ and Perfect symetry: $\Delta V_{out} = 0$
   - But in Presence of mismatch: $\Delta V_{out} \neq 0$ as it will be amplified and usually will hit the supply rails



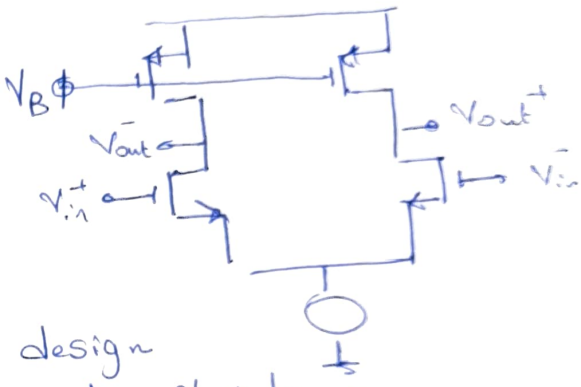
2. the input-referred offset Voltage V_{OS}
   ↳ the input Level that forces the output Voltage to go back to Zero.

3. V_{OS} is random Variable : $\sigma(V_{OS}) = \sigma(\Delta V_{tot})$

4. Quiz
   Assume PMOS V_{TH} mismatch is σ_P and NMOS σ_N
   What is the rms input reffered offset Voltage.
   Hint → the mismatch is usually a small perturbation
   so we can analyze it using small sig modal (as noise)

$$\sigma_{OF} = \sqrt{\sigma_N^2 + \sigma_N^2 + 2\sigma_P^2 \frac{g_{mp}^2 R_{out}^2}{g_{mN}^2 R_{out}^2}}$$

$$= \sqrt{2\sigma_N^2 + 2\sigma_P^2 \frac{g_{mp}^2}{g_{mN}^2}}$$



(12) Systematic offset

1. Systematic offset is due to design or Layout issues rather than random Variations.
   ↳ it can be nulled by proper design and Layout

2. One Common example is miller OTA
to Cancel offset we must size M6 such that

$V_{GS6} = V_{GS3,4}$

$V_{out1Q} = V_{in2Q}$