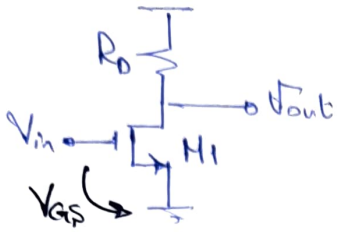
# Analog Integrated Circuits.
# Lec20: Common-mode feedback.

## ① Well defined Vs. ill defined output level.

- To understand what's the meaning of well and ill output level, Lets take examples.

### 1.1

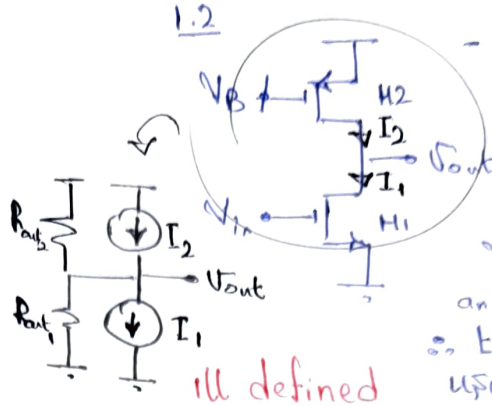



$V_{out} = V_{DD} - I_D R_D$

; $I_D = f(V_{GS})$

∴ Well defined output level.

### 1.2




ill defined

- each transistor $M_1, M_2$ works as VCCS that generates $I_1 = f(V_{GS1})$ and $I_2 = f(V_B)$
- Now, we have voltage source = $V_{DD}$ and current source = $I_1, I_2$
∴ to calculate $V_{out}$ use super position.
  1. activate $V_{DD} \rightarrow V'_{out}$
  2. activate $I \rightarrow V''_{out}$
  3. $V_{out} = V'_{out} + V''_{out}$

- $V'_{out} = V_{DD}\left(R_{out1} \,//\, (R_{out1} + R_{out2})\right)$
- $V''_{out}$: as $I_1, I_2$ are defined by to different voltages $V_{GS1}, V_B$
∴ they can not be exactly the same
∴ there's $\Delta I = I_2 - I_1$ @ $V_{out}$
∴ $V''_{out} = \Delta I R_{out}$ ; $R_{out} = R_{out1} \,//\, R_{out2}$

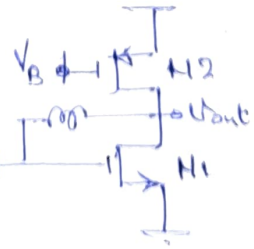
# Still where is the problem?

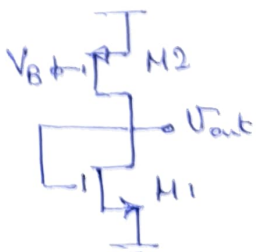
Problem is the HI.N @ the output ; Small ΔI generates Large ΔV

ΔI → +Ve: $V_{DS2}$ ↓ → M2-triode
ΔI → -Ve: $V_{DS1}$ ↓ → M1-triode

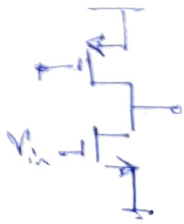
- Practically to use the previous amplifier "1.2" you'll need to make one of the current sources defined by the other one.
- the Cap and inductor can be used but it will take large area and the inductor will generate other problem so we can use other tricks here as
  - negative feedback
  - switches
  - Resistances with different ac and DC values.

@ DC

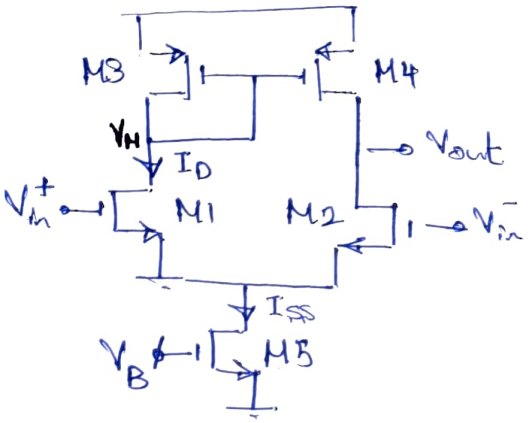



@ AC



## 1.3 SE-5T OTA



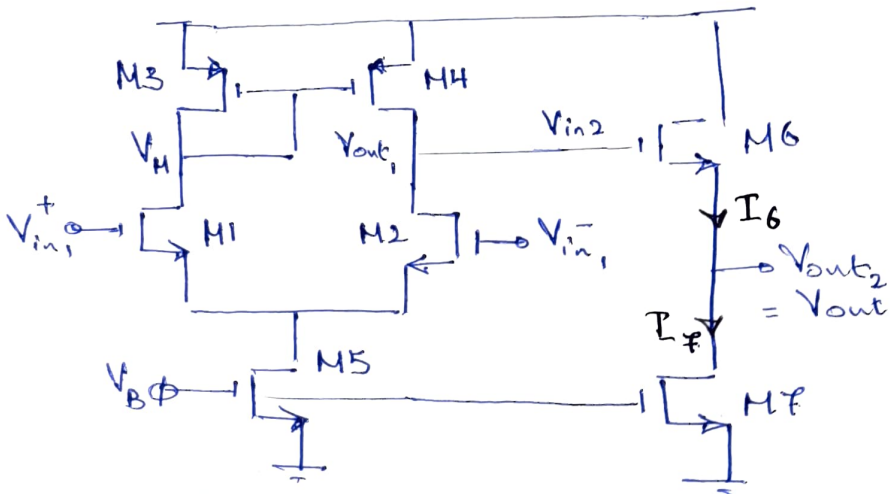

$V_{out} = V_M = V_{DD} - V_{GS3}$

$\because V_{GS3} = f(I_D) = f(I_{SS})$

$= f(V_B)$

$\therefore$ Well defined output

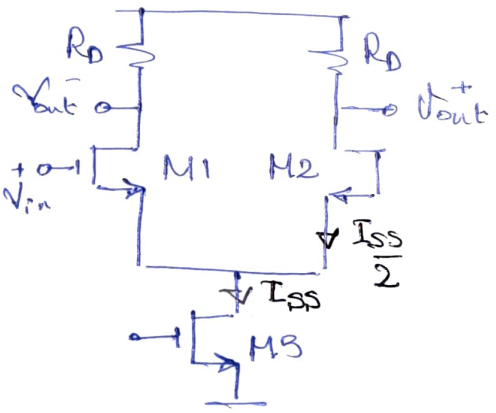
## 1.4 SE-two Stage.




$\because M_f\_I_D = f(V_B)$ , $M6\_I_D = f(V_{out_1})$

$\therefore$ ill defined output Level.

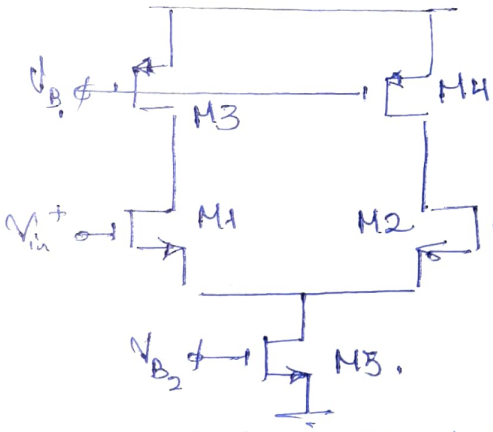
## 1.5 FD-Resistive Load




$V_{out} = f(V_B)$

$\therefore$ Well defined output Level.

## 1.7 FD-5T OTA



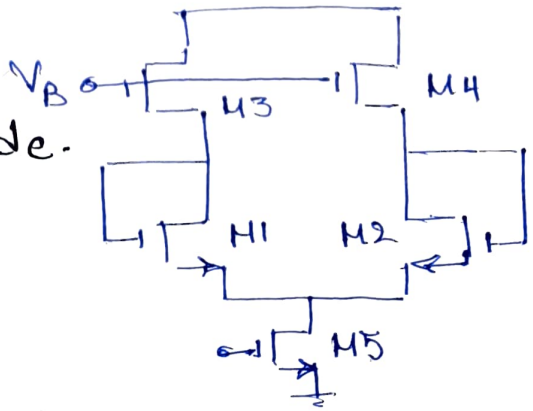

$\because I_{D_{3,4}} = f(V_{B_1})$ and $I_{D_{1,2}} = \frac{I_{SS}}{2} = f(V_{B_2})$

$\therefore$ ill defined output Level.

- mismatch will always create a finite error between $I_{D_{3,4}}$ and $\frac{I_{SS}}{2}$

- if
  - $I_{D_{3,4}} > \frac{I_{SS}}{2}$ : $I_{D_{3,4}}$ fall to $\frac{I_{SS}}{2}$ : M3 and M4 enters triode.
  - $I_{D_{3,4}} < \frac{I_{SS}}{2}$ : $\frac{I_{SS}}{2}$ falls to $I_{D_{3,4}}$ : M1, M2, M5 enter triode.

- even if we make feedback to this types of circuits we will ensure M1, M2 always in saturation, But still M5 in triode.



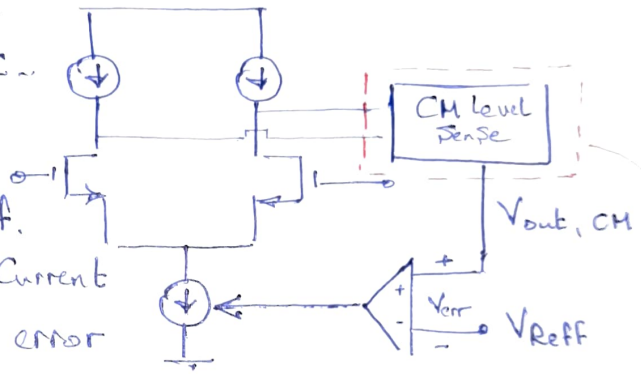

- So we need a CMFB !!

- Even this problem is in all FD networks with H.I.N @ the output. Why we use it?

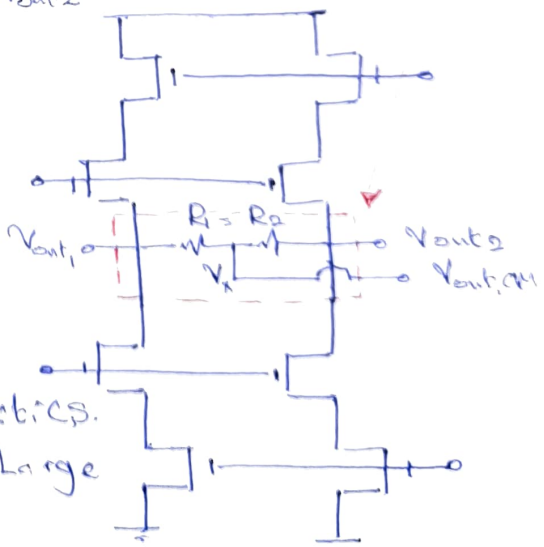
* Fully differential Vs. diff input SE output.
  - Larger output swing ~ 2x
  - No mirror poles. → higher speed
  - Better CMRR and PSRR.
  - Better SNR.
  - Better Linearity → lower distortion → 2nd order canc.
  - Easy to analyze. → half circuit principle.

## ② Common mode feedback Loop.

2.1 CMFB is a Negative Feedback system that..
1. Sense CM level
2. Compare it to a ref.
3. adjust the bias current to minimize the error



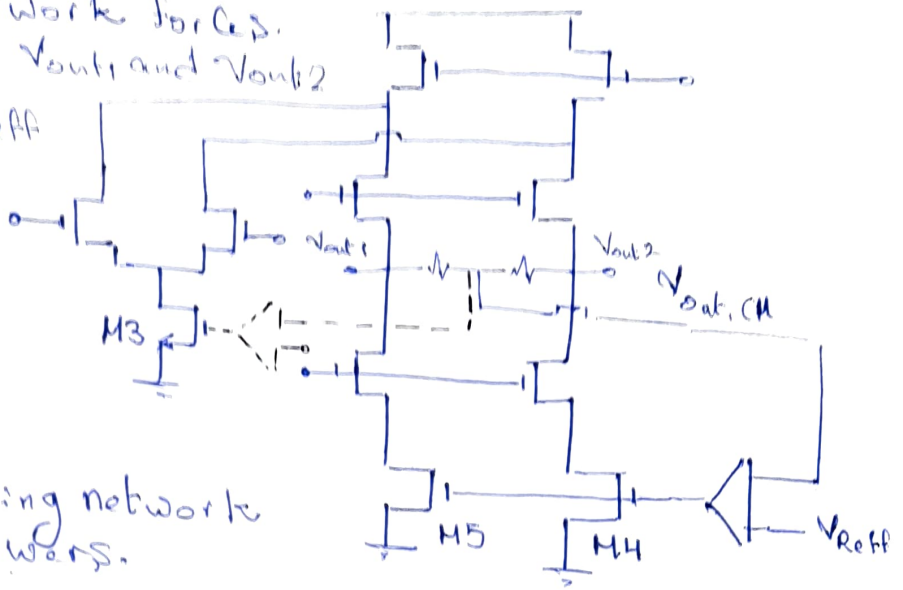

2.2 CM Level Sensing network: Resistive Sensing.
1. Vx is the avg. between Vout1, Vout2
   → Vout, CM
2. Pros: Linear Sensing.
3. Cons:
   → Small R will degrade the gain.
   → Large R will occupies Large area and has Large Parasitics.




4. Why we not use trans. as a Large resistance with small area and small parasitic?
   because this resistance is non-Linear
5. Non-Linear Sensing → CM Sensing fails.

» Example.

The feedback network forces the CM level of $V_{out,1}$ and $V_{out,2}$ to approach $V_{Reff}$ either by adjust M4, M5 or by adjust M3.




## 2.3 CM Level Sensing network : Source followers.

- To use resistive sensing without degrades the gain we can use a CD-stage. « buffer »

2- The CD stage introduce DC shift → Should be considered in the comparison step

$V_{Reff} \rightarrow V_{Reff} - V_{GS,7,8}$

- this means $V_{Reff}$ should enters to exact buffer

4- disadvantages.

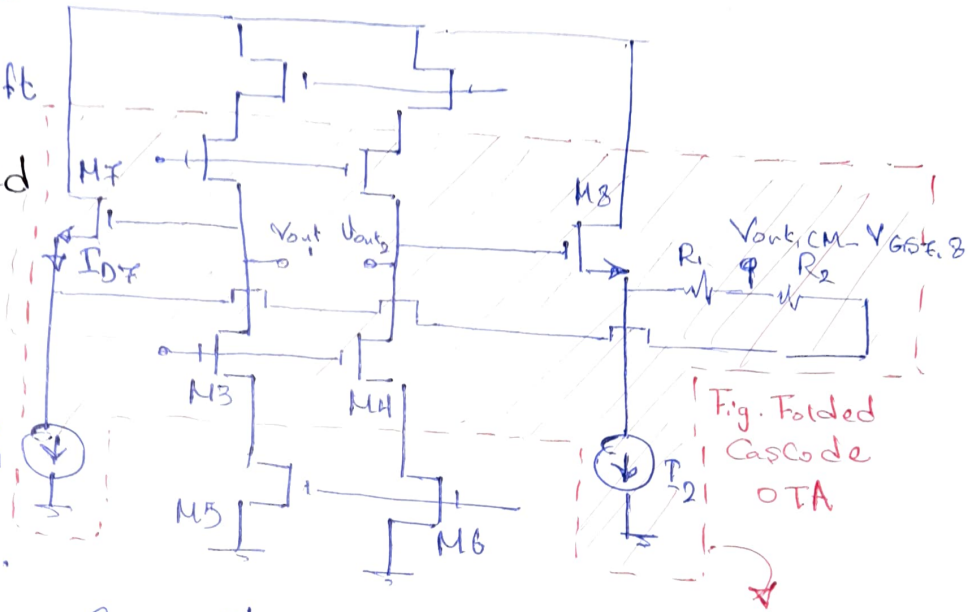



Fig. Folded Cascode OTA

→ 1. extra Power Consumption

→ 2. If $V_{out2} \uparrow$, $V_{out1} \Downarrow$

- $I_1$ must sink both

$$I_x \simeq \frac{(V_{out2} - V_{out1})}{R_1 + R_2}$$ Pk to Pk diff output

and If

∴ if $[R_1 + R_2]$ or $I_1$ are not sufficiently Large,

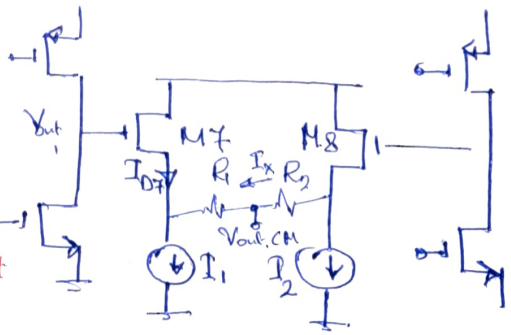
∴ $I_{D7}$ drops to zero → non-Linearity added

# To ensure it will not happen.

→ Small $I_x$ → Large $R_1, R_2$ → more area, more Capacitance

or

→ Large $I_{1,2}$ → More Power Cons.



↳ 3. $I_1$, $I_2$ need $V_{Compliance}$

∴ Limited $V_{out,min}$ → Limited swing.

→ Without CMFB

$V_{outmin} = V_{ov3,4} + V_{ov5,6}$

Limited by $M_{3,4}$ and $M_{5,6}$

→ With CMFB

$V_{outmin} = V_{TH} + V_{ov7,8} + V_{I1,2}$

Limited with sensing circuit M8, F and $I_{1,2}$

## (3) Continous time CMFB network - Summary

3.1 Resistive Sensing → Low Voltage gain

3.2 Source followers → Limited linear range and high Power

3.3 other techniques exist but also suffer from Limited Linear range.

3.4 Designing Continous-time CMFB Circuits that are both Linear and operate with Low-Power supply Voltage is not an easy task.

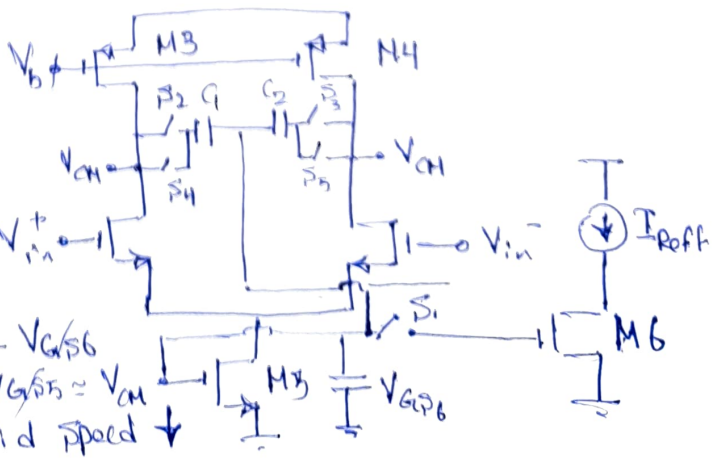
## (4) Discrete-time CMFB

4.1 another Popular CMFB technique is discrete time switched-Capacitor CMFB

1. Suitable for discrete-time switched Caps Circuits.
2. uses switches and Capacitors.
3. the Circuit must be refreshed periodically

4.2 Switched Capacitors CMFB

- Reset Phase $S_1$, $S_4$ and $S_5$ Close
  ↳ Capacitor charged
  ; $V_C = V_{CM} - V_{GS6}$
- Amplification phase $S_2$ and $S_3$ Close
- $V_{out,CM} = V_C + V_{GS5} = V_{CM} - V_{GS6} + V_{GS5} \simeq V_{CM}$
- Note $C_1 = C_2$ = Small Value to avoid speed ↓



## (5) CMFB Loop Practical aspects.

### 5.1 aspects.

1. CMFB Loop must be Carefully analyzed.
   - ↳ Draw SS model using (SS half Circuit principle) or (Combine both side in parallel)
   - ↳ Find LG, Gx, PM, etc.

2. We don't need high DC LG for CMFB Loop Why?
   - ↳ We not need highly Precise CM Level.

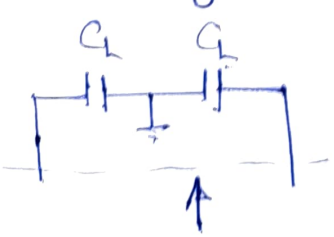
3. Ideally CMFB Loop Bw Sould be Close to diff Loop Bw
   - ↳ Recover quickly from CM disturbance (e.g. Supply and Coupling noise)
   - ↳ But this means high Power Consumption.

4. Practically Set CMFB bandwidth to 30% of diff Loop Bw
   - ∴ for $10\tau_{diff}$ we need $3\tau_{CM}$
   - ∴ 95% of CM disturbance is removed

### 5.2 CMFB Loop Capacitive Loading.

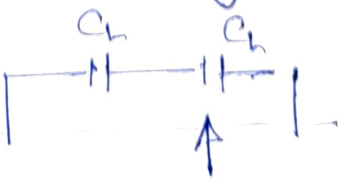
1. Single stage OTAs are Compensated by large $C_L$
2. the same $C_L$ Can be used to Compensate the CMFB Loop

# 3. Cautions: the differential and CM Capacitive Loading are not necessarily the same!



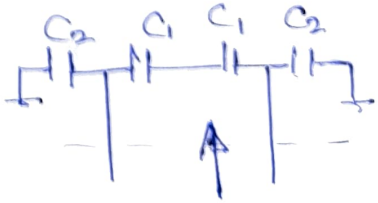

$\gamma_{CM} = 2sC_L$

$\gamma_{diff} = sC_L/2$




$\gamma_{CM} = 0$

$\gamma_{diff} = \frac{sC_L}{2}$

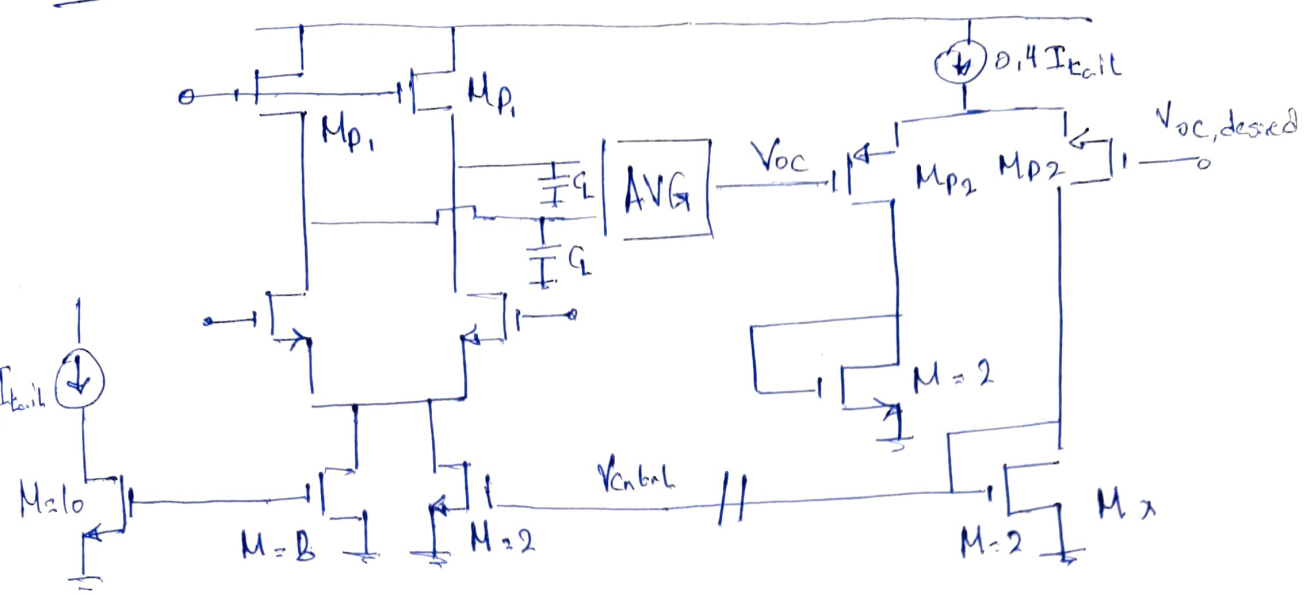



$\gamma_{CM} = 2sC_2$

$\gamma_{diff} = \frac{s(C_1+C_2)}{2}$

# (7) CMFB Loop Examples.

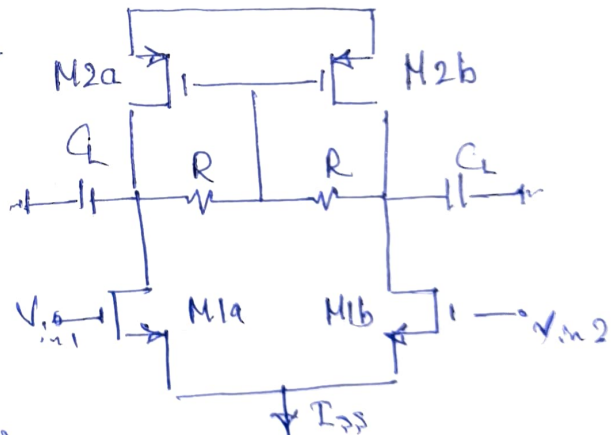
## 7.1




$$LG_{0,CM} = \frac{1}{2} * g_{mx} * r_{op_1} * \frac{g_{mp2}}{g_{mx}} * \frac{1}{2}$$

$$\omega_{u,CM} \simeq LG_{0,CM} * \frac{1}{r_{op_1} C_L}$$

## 7.2




1. Error amp replaced by a wire
2. $V_{CM}$ pinned to $V_{DD} - V_{SG2}$
3. max pk to pk diff swing $\simeq 4 V_T$
4. $LG_{0,CM} \simeq g_{m2} r_{O2}$
5. $LG_{0,diff} = g_{m1} (r_{O1} \| r_{O2} \| R)$
6. $\omega_{u,CM} = LG_{0,CM} \times \frac{1}{r_{O2} C_L} = \frac{g_{m2}}{C_L}$ , $\omega_{P_2,CM} = \frac{1}{R C_{gg2}}$
7. $\omega_{u,diff} = \frac{g_{m1}}{C_L}$ , $\omega_{P_2,diff} = \frac{g_{m2}}{C_{gg2}}$