5T OTA Design Example

1. If VA slightly decreases with gm/ID, the chart of gm*ro vs gm/ID will be _____.

A	Curves with slightly decreasing slopes convex upwards	C	All answers are wrong
B	Straight lines	D	Curves with slightly increasing slopes convex downwards

2. If the long channel model (square-law) is valid, then VGS vs gm/ID chart should be _____.

A	All answers are wrong	C	Multiple curves with shortest L at top
B	Multiple curves with longest L at top	D	A single curve independent of L

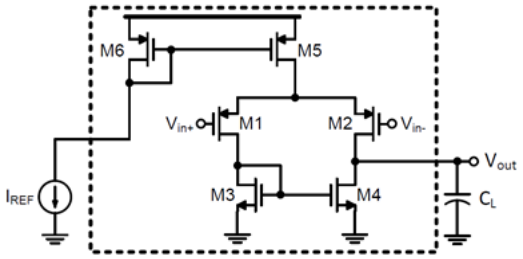
$$I_D = \frac{uC_{ox}}{2} \times \frac{W}{L} V_{ov}^2 \rightarrow g_m = uC_{ox} \times \frac{W}{L} V_{ov} \rightarrow \frac{g_m}{I_D} = \frac{2}{V_{ov}} = \frac{2}{V_{GS} - V_{TH}} \neq f(L) \rightarrow \text{single curve}$$

3. If VDD = 2V and the required CMIR of an OTA is 0.2 V to 1.8 V, then the input stage should be _____.

A	NMOS and PMOS (both of them together)	C	PMOS
B	NMOS	D	NMOS and PMOS (anyone of them will work)

4. For a 5T OTA, if you want to use larger gm/ID for the current mirror load while keeping the amplifier DC gain almost unchanged, this means you should use ____.
Hint: Neglect VA variation with gm/ID.

A	Smaller W	B	Larger W	C	Larger L	D	Smaller L



5. For the shown 5T OTA, increasing L will increase the DC voltage gain and improve the matching at the expense of _____.

A	Lower phase margin	B	Larger area	C	All are correct	D	Larger device caps

Increasing L → Increase Area → Increase device capacitances → Increase C_{mirr} → Reduce the PM

6. For the shown 5T OTA, the gm/ID of _____ is a design parameter that affects the output swing.

A	$M_{3,4}$	B	All are correct	C	M_5	D	$M_{1,2}$

7. For the shown 5T OTA, if CL is much larger than device capacitors, the main design parameter affecting the relation between power consumption and the GBW is _____.

A	L of the input pair	B	gm/ID of the input pair	C	L of the load	D	gm/ID of the load

$$GBW = \frac{g_{m1,2}}{2\pi C_L} \rightarrow \text{for a given } I_D \text{ the GBW achived depends on the } g_m \text{choosed for the input pair}$$

8. For the shown 5T OTA, using ____ will cause more CMRR degradation at high frequency.

A	Larger L for M1,2	B	All answers are correct	C	Larger gm/ID for M1,2	D	Larger gm/ID for M5

$$CMRR = g_{m1,2}[r_{o2} \parallel r_{o4}] \times 2g_{m3,4}R_{ss}$$

$C_{sb1,2}$ will increase as $M_{1,2}$ area increase by larger L or larger $\frac{g_m}{I_D}$ (W) reducing

Larger $\frac{g_m}{I_D}$ (W) for M_5 → larger area for M_5 → larger C_{gd5} and C_{db5}

All these capacitance are parallel with R_{ss} reducing the effective R_{ss}

9. For the shown 5T OTA, assume the input pair is biased at a given gm/ID. Achieving higher ____ necessitates higher power consumption.

A	CMRR	B	Gain	C	BW	D	GBW

$$GBW = \frac{g_{m1,2}}{2\pi C_L} \rightarrow \text{for a given} \frac{g_m}{I_D} \text{ the higher } I_D \rightarrow \text{ the higher } g_m \rightarrow \text{the higher GBW}$$

10. For the shown 5T OTA, if there is a strict spec on the fanout (FO = CL/Cin), i.e., a small Cin is required, then the following assumption should be used to satisfy the gain spec: _____.

A	ro2 << ro4	B	ro2 >> ro4	C	ro2 = ro4	D	All answers are wrong

Smaller C_{in} → Smaller Area of input devices → Smaller L for input device → $r_{o2} \ll r_{o4}$