

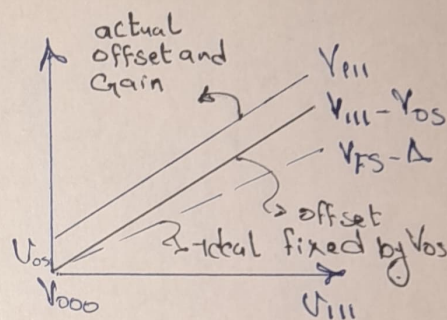
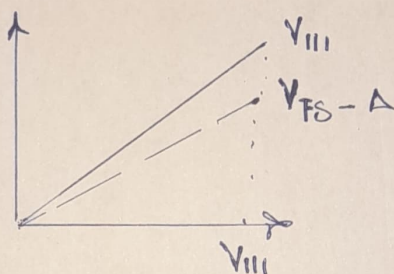
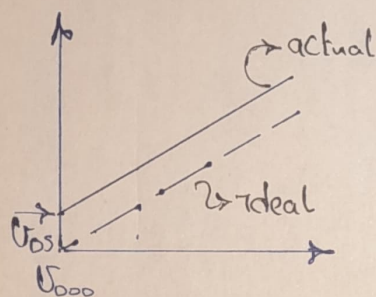
lec 6, Testing

① DAC Static Testing

- As input is wide range we have many points to test so we automate it. by Computer-based test setup
- Most equipment can be Computer Controlled.

② DAC offset and Gain error

- measure offset error first then measure gain error.



- Offset error is @ input all zeros.

$$V_{000} = V_{os}$$

$$\left(\frac{V_{III}}{V_{FS} - \Delta} - 1 \right) \times 100$$

- offset $V_{os} = V_{000}$

- Gain error % :

$$\left(\frac{V_{III} - V_{os}}{V_{FS} - \Delta} - 1 \right) \times 100$$

③ DAC Dynamic Testing.

- Dynamic characteristic of DAC measured by two input \perp Digital Sinusoidal \rightarrow DAC \rightarrow Spectrum analyzer.

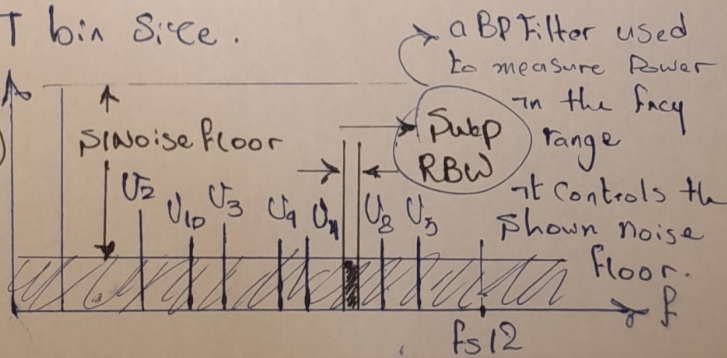
as it has a single tone, so if there are any unwanted components it will be crral.

\rightarrow Spectrum analyzer resolution band-width (RBW)

is equivalent to FFT bin size.

$$SNR = \text{SINoise floor} - 10 \log_{10} \left(\frac{f_{s/2}}{RBW} \right)$$

\rightarrow if RBW is low \rightarrow the noise floor is clear \rightarrow but slow



- $SNR = \text{Signal Floor} - 10 \log \left(\frac{FS12}{RBW} \right)$
- $THD = 20 \log \sqrt{\left(10^{\frac{-V_1}{20}} \right)^2 + \left(10^{\frac{-V_3}{20}} \right)^2 + \dots + \left(10^{\frac{-V_6}{20}} \right)^2}$ the first 5-Harmonic. note we took V_6
- $SINAD = 20 \log \sqrt{\left(10^{\frac{-SNR}{20}} \right)^2 + \left(10^{\frac{-THD}{20}} \right)^2}$

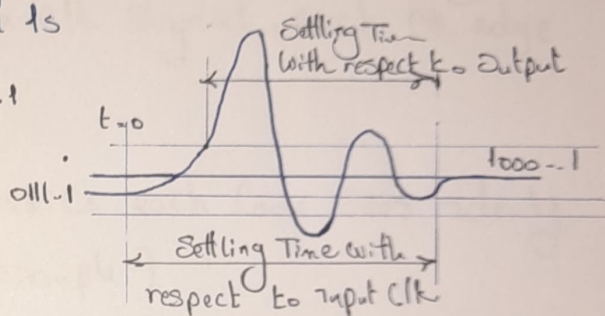
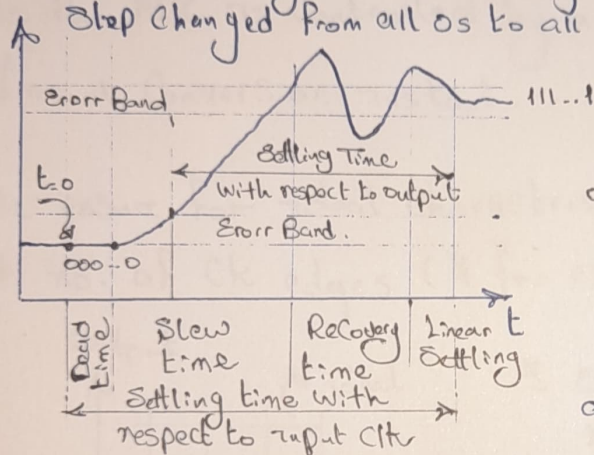
note: all in unit of dBc

The ratio of update rate to test tone freq must be non-integer. otherwise the quantization noise appears as

distortion (??)

2 Step signal \rightarrow DAC \rightarrow oscilloscope to plot both clk and output

- Full scale settling time where digital step changed from all 0s to all 1s



- In mid scale transition all bits are switched, but may not switch

Simultaneously (??)

4 ADC Static Testing

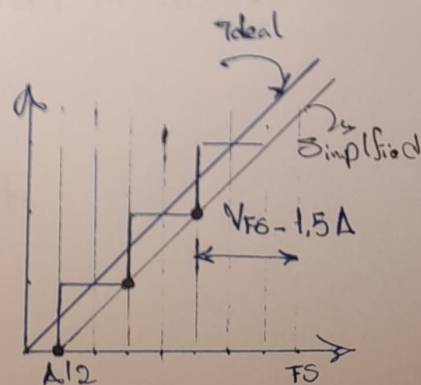
1 The ideal characteristics of ADC is the line which connects the Code Centers.

2 measuring Code Centers is very difficult, so we define the characteristics using Code Transition

3 first point in the CCS @ $V_{LSB}/2$

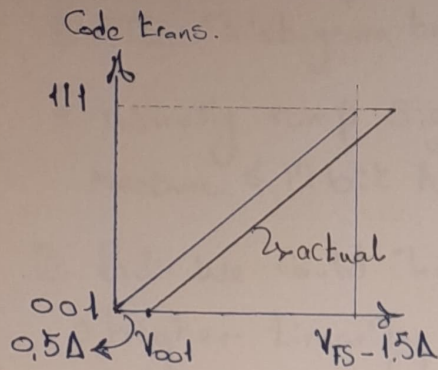
4 Last point in the CCS @ $V_{FS} - 1.5 V_{LSB}$

note: Static Testing can be done by a very slow signal not only DC



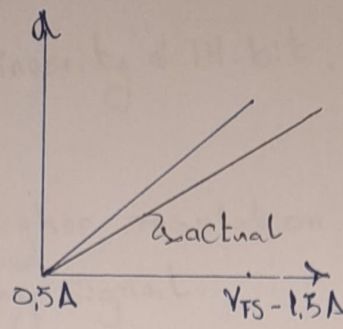
⑤ ADC offset and Gain errors.

Page ③



$$\text{Offset error} = V_{001} - 0.5Δ$$

$$\text{Gain error} = 0$$



$$\text{Offset error} = 0$$

$$\text{Gain error} = 100 \times \left(\frac{V_{111} - 0.5Δ}{V_{FS} - 2Δ} - 1 \right)$$

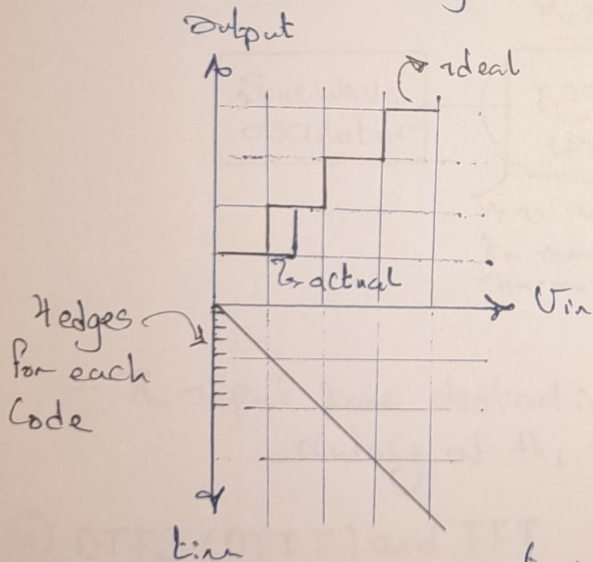
$$\text{Gain error} = \left(\frac{V_{111} - V_{001} - 1}{V_{FS} - 2Δ} \right)$$

$$\text{Offset error} = V_{001} - 0.5Δ$$

⑥ Histogram (Code density test)

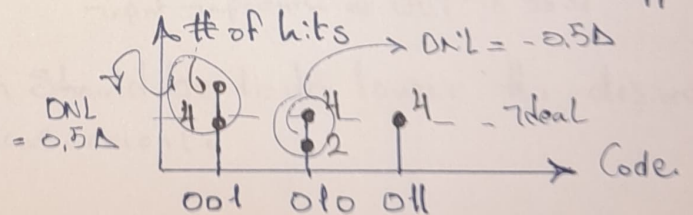
- 1 This test is done by adding ramp signal as analog input
- 2 As the ADC is controlled by a clk signal, each clk edge define a Conversion instant.

- 3 We ensure for ideal characteristics each Code sees ideally # no. of clk edges (4 for example)



- 4 So ideally each Code appears 4 times before output changes

- 5 So if we Plot a Histogram for Code vs no. of hits (appear)



- 6 We got non-idealities in actual CCS

So, we have wide Code and narrow Code.

∴ The DNL and INL Can be obtained as

$$\text{DNL} = \frac{\text{ideal no of hits} - \text{actual no. of hits}}{\text{actual no of hits}}$$

$$\text{INL} = \text{CumSum (DNL)}$$

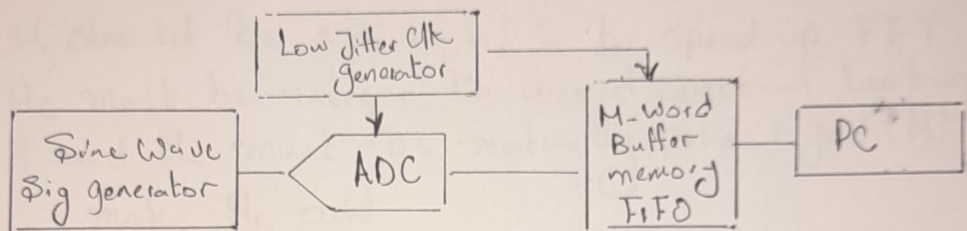
- 8 no of ideal hits & testing resolution but increase testing time

④ Sine Wave Histogram test.

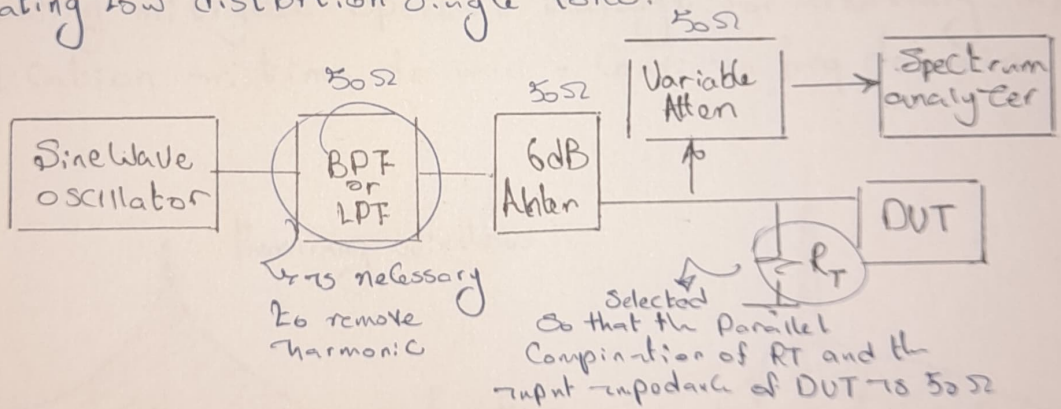
Page ④

- 1 The Histogram test depends on the linearity of testing sig.
- 2 usually ramp signal linearity ≤ 14 -bit, so it only used to measure ≤ 12 bit ADC
- 3 But we could have higher resolution ADC, so we need a higher linearity testing signal.
- 4 Sinewaves can be generated with extremely high linearity and low noise with appropriate filtering.

⑧ ADC Dynamic testing.



- Generating low distortion single tone.



- The input tone distortion should be 10dB lower than the desired accuracy of the measurements

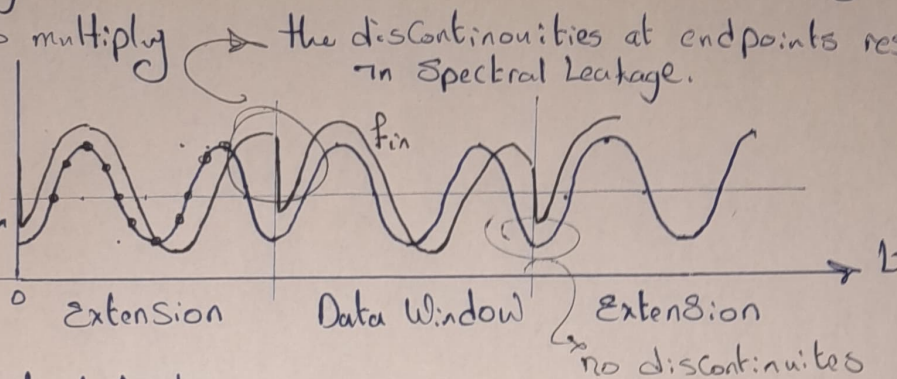
⑨ DFTS (DTFT) and FFT

- 1 The DFT operates on a finite number (N) of digitized time samples
- 2 When these samples are repeated and placed "end-to-end" they appear periodic to the transform
- 3 Practically, FFT is used to compute DFT
- 4 The FFT is simply an algorithm that reduces the mathematical computations

5 Spectral Leakage.

Page 5

It is equivalent to multiply the input sine wave by a rect window Puls which has $\frac{\sin x}{x}$ freq resp.



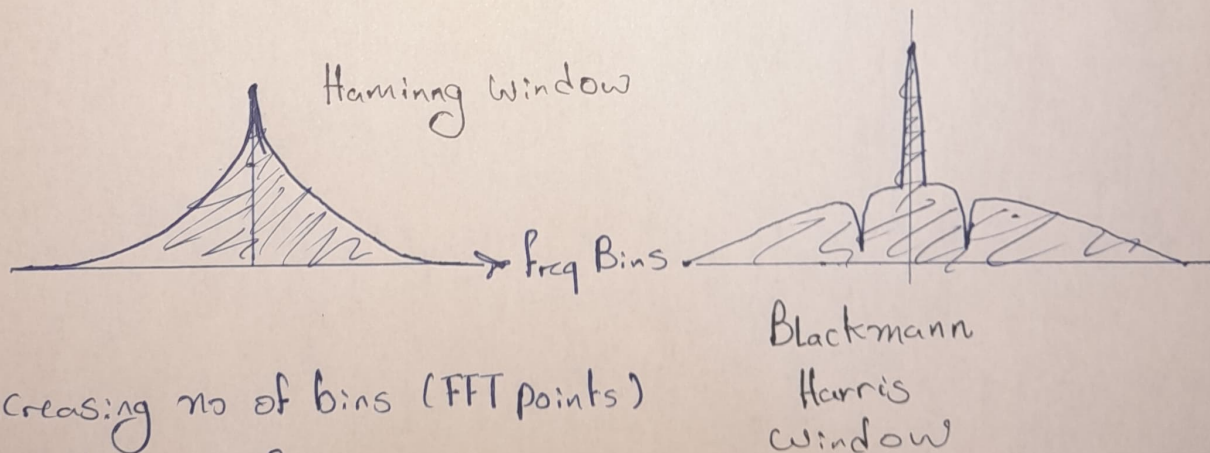
6 to prevent spectral leakage

The window we take should cover an integer no. of cycles.

$$T_{\text{measure}} = M \times T_s = M_c \times T_{\text{in}} \rightarrow \frac{f_s}{f_{\text{in}}} = \frac{M}{M_c}$$

Where: M should be a power of 2 to speed up FFT
 M_c must be integer to avoid spectral leakage.
 M and M_c must be mutually prime: $\text{gcd}(M, M_c) = 1$
make M_c odd

7 Windowing mitigate spectral leakage for arbitrary input
Multiplication in time domain = Conv. in freq domain



8 Increasing no of bins (FFT points)

reduces the noise floor

note: noise power = $M/2 \times \text{Noise floor} = \text{Const}$