01 | A junior designer in your company is designing an amplifier. The input signal can be as low as 1 mV and the supply noise can be up to 100 mV. He is confused about what PSRR spec could be reasonable for his amplifier. It is well known in your company that you are a systematic and knowledgeable designer, so he came to you asking for help. You suggested that the input-referred supply noise should be 10 times smaller than the signal, which translates to _____ dB PSRR spec.

$$v_{in} = 1\ \text{mV and}\ v_{out} = 100\ \text{mV and}\ v_{DD,in} = 0.1\ \text{mV}$$

$$\text{PSRR} = 10 * \frac{100\ \text{mV}}{1\ \text{mV}} = 1000 = 60\ \text{dB}$$

02 | A junior designer in your company is designing a two-stage Miller OTA. He designed the input pair to have gm/ID = 10. One of his colleagues suggested that, in order to boost the speed of the OTA, he should redesign the input pair to have gm/ID = 20, while keeping all other devices unchanged. It is well known in your company that you are a systematic and knowledgeable designer, so he came to you asking: what will happen to the GBW and SR?

$$\text{GBW} = \frac{g_{m1}}{2\pi C_c} \quad \text{and} \quad \text{SR} = \frac{I_{B1}}{C_c + C_1}$$

$$\text{if} \frac{g_{m1}}{I_D} \uparrow\uparrow \ @\ \text{Constant}\ I_{ss} \rightarrow\ g_m \uparrow\uparrow \rightarrow \text{GBW} \uparrow\uparrow \rightarrow W \uparrow\uparrow \rightarrow C_1 \uparrow\uparrow \rightarrow \text{SR} \downarrow\downarrow$$

03 | A junior designer in your company is designing an OTA. He doesn't have a strict CMIR spec and the gain is not high, so he decided to use a 5T OTA. But he has a tough PSRR spec. It is well known in your company that you are a systematic and knowledgeable designer, so he came to you asking for advice. You told him that he should use a _____ input stage.

PMOS

04 | A junior designer in your company is designing a folded cascode OTA. One of his colleagues suggested that, in order to boost the speed of the OTA, he should put more than half the current in the CS branch instead of splitting the current equally. It is well known in your company that you are a systematic and knowledgeable designer, so he came to you asking: what will happen to the GBW and SR?

$$\text{GBW} = \frac{g_{m1}}{2\pi C_c}$$

$$\text{if}\ I_{CS} \uparrow\uparrow\ @\ \text{Constant} \frac{g_m}{I_D} \rightarrow\ g_{m1} \uparrow\uparrow \rightarrow \text{GBW} \uparrow\uparrow \rightarrow I_{CG} \downarrow\downarrow \rightarrow \text{SR} \downarrow\downarrow\ \text{SR} \downarrow\downarrow\ \text{as SR is limited by smaller current}$$

05 | A junior designer in your company is designing a two-stage Miller OTA. He selected Cc = CL and designed the circuit for a critical damped response. One of his colleagues suggested that, in order to boost the speed of the OTA, he should select Cc = 0.5*CL, while keeping all other devices unchanged. It is well known in your company that you are a systematic and knowledgeable designer, so he came to you asking: is anything wrong going to happen in the circuit? (Select all correct answers)

- ■ The PM will decrease
- □ The power consumption will increase
- ■ The rms noise will increase
- □ The gain will decrease

06 | A junior designer in your company is designing a two-stage Miller OTA. He selected Cc = CL. One of his colleagues suggested that, in order to boost the speed of the OTA, he should select Cc = 0.5*CL, while keeping all other devices unchanged. It is well known in your company that you are a systematic and knowledgeable designer, so he came to you asking: what will happen to the GBW and SR?

$$GBW = \frac{g_{m1}}{2\pi C_c} \quad \text{and} \quad SR = \frac{I_{B1}}{C_c + C_1}$$

$$\text{if } C_c \downarrow\downarrow \rightarrow GBW \uparrow\uparrow \rightarrow SR \uparrow\uparrow$$

07 | A junior designer in your company is designing a two-stage Miller OTA that has a specific closed loop gain, a specific closed loop bandwidth, and a critical damped response. He selected gm/ID = 16 for the input pair. Now he wants to double the SR without spending more power. It is well known in your company that you are a systematic and knowledgeable designer, so he came to you asking: what change shall I do in my circuit? (Select all correct answers)

- ■ Use gm/ID = 8 for the input pair and halve Cc
- □ Halve Cc
- □ Use gm/ID = 8 for the input pair
- □ Use degeneration in the first stage with Rs = 1/gm1 and halve Cc

08 | A junior designer in your company is designing a two-stage Miller OTA in a BiCMOS technology. He has a tough SR spec. It is well known in your company that you are a systematic and knowledgeable designer, so he came to you asking: shall I use BJT or MOSFET for my input pair? You recommended using MOSFET, and you gave him an example that for the same UGF, if he used gm/ID = 10, then MOSFET SR will be _____ times higher than BJT SR. Hint: Assume Vth = 26 mV.

$$\frac{g_m}{I_C} = \frac{1}{V_T} = 38.5\frac{S}{A} \rightarrow \text{for the same UGF} = \frac{g_m}{2\pi C_c} \rightarrow C_c \text{ for BJT} = 3.85\ C_c \text{ for MOSFET}$$

$$SR = \frac{I_{B1}}{C_c} \rightarrow \text{SR of MOS} = 3.85 \text{ SR of BJT}$$

09 | The distortion caused by the finite SR of an OTA is _____ distortion.

$$\text{non} - \text{linear}$$

10 | A junior designer in your company is designing a folded cascode OTA. One of his colleagues suggested that, in order to boost the speed of the OTA, he should put more than half the current in the CG branch instead of splitting the current equally. It is well known in your company that you are a systematic and knowledgeable designer, so he came to you asking: what will happen to the GBW and SR?

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

$$\text{if } I_{CG} \uparrow\uparrow \rightarrow I_{CS} \downarrow\downarrow \text{ @ Constant} \frac{g_m}{I_D} \rightarrow g_{m1} \downarrow\downarrow \rightarrow GBW \downarrow\downarrow \rightarrow SR \downarrow\downarrow \text{ as SR is limited by smaller current}$$