Analog Integrated Systems Design.

lec8: Basics of Switched Capacitor Circuits.

① Switched Cap Circuits.

1 The most popular approach for realizing analog Sig processing in CMOS ICs.

2 Analog Signals are Sampled and stored on Capacitors.

→ 1 → Charge is transfered from one Cap to another.

→ 2 → discrete time analog Sig → need z-transform.

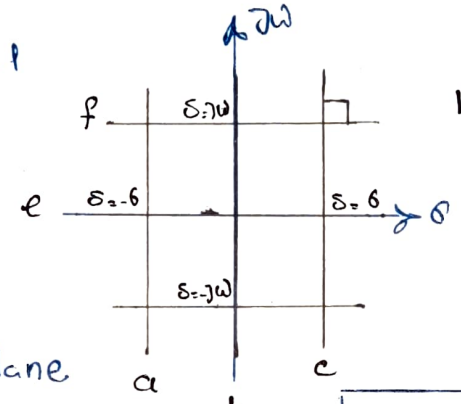
→ 3 → require AAF and Smoothing filter when Combined with Continous time Circuits.

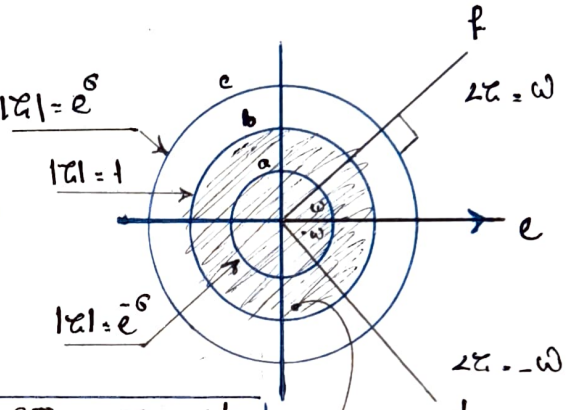
② S-plane Vs z-plane

1 - Assume $f_s = 1$ → normalized.

$|z| = e^{\sigma}$

$\angle z = \omega$





2 RHP in S-plane maps to outside unit Circle in z-domain

$z = e^{sT_s} = e^{(\sigma + j\omega)/f_s}$

LHP ∴ Stable

3 Why z-transform?

that because Sampled Systems are periodic in freq domain with 2π distance (Period) normalized representation.

∴ 2π is Complete Circule So, we do not need to plot again for each Period.

③ Switched Cap Circuits buliding blocks.

1 OP-Amps (OTA)

- DC gain ≈ 40 to 80 dB
- GBW ≈ > 10 f_s
- PM > 60°
- SR, noise, offset.

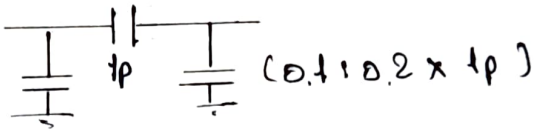
2 Capacitors.

- Very well matched Cap could be fabricated.
- The absolute error of variation for Cap is less than res.
- Caps dependance on V and T is much better than res.
- Unit Caps ranged from sub fF to few pF

- Types of Caps
  - Poly insulator Poly → not used beyond 0.18 u
  - Metal insulator Metal → Vertical field
  - Metal oxide Metal → Lateral and Vertical field
  - MOSCaps. → High density but highly non-linear

- Caps Specs
  - Linear → Low Voltage Coeff
    - P.P, MiM, MoM are good up to 16 bits
    - MOSCaps are highly non-linear but it's ok for less 8 bits
  - Small parasitics

For P.P and MiM → bottom plate Cap
Could be 20% of the desired Cap

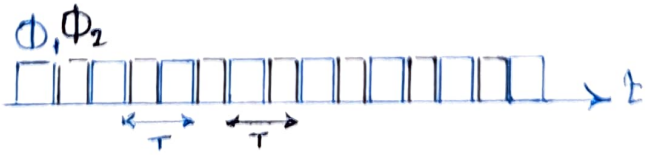


3 Switches

- Switches imperfection
  - Input dependent resistance → use TG or BS
  - Channel Charge injection → use bottom plate Samp
  - Clk feedthrough → use diff architecture
  - Non-linear junction Cap → use Parasitics insensitive structure

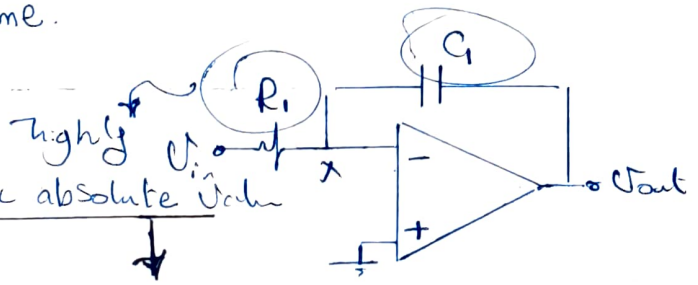
4 Non-overlaping clks.

- Running @ same freq but they are not simultaneously high.
- Non-overlapping time determined by inverter delays or RC network
  - → Sensitive to PVT variation.
  - → High Speed designs use delay Locked Loops



(4) Why not CT Continous time.

1- Ex: CT integrator



S-domain

$$\frac{V_{out}}{V_{in}} = -\frac{\frac{1}{C_1 S}}{R_1} = -\frac{1}{R_1 C_1 S}$$

T-domain

$$\frac{V_{in}}{R_1} = -C_1 \frac{dV_{out}}{dt}$$

$$\therefore V_{out} = -\frac{1}{R_1 C_1} \int V_{in}\, dt$$

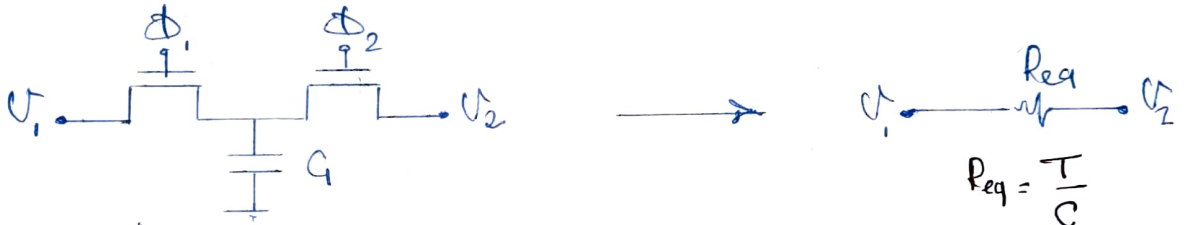
$\tau = R_1 C_1$

↳ as Absolute R and C are highly Variable → We can not build a precise CT integrator

↓

Solution to DT !! (5)

2 Switched Capacitor resistor equivalence.



$$R_{eq} = \frac{T}{C_1}$$

Φ_1 and Φ_2 are non-overlaping Clk.

assume $V_1 > V_2$

→ ① 1st half period: C_1 is charged with V_1

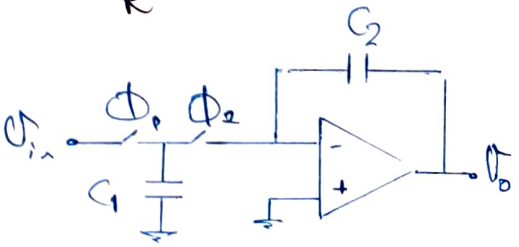
② 2nd half period: C_1 is charged with V_2

$$\therefore \Delta Q = C_1 \Delta V = C_1 (V_1 - V_2) \text{ every Clk period}$$

$$\therefore I_{avg} = \frac{\Delta Q}{T} = \frac{C_1 (V_1 - V_2)}{T} = \frac{V_1 - V_2}{R}$$

$$\therefore R = \frac{T}{C_1} = \frac{1}{f_s C_1}$$

3 DT integrator

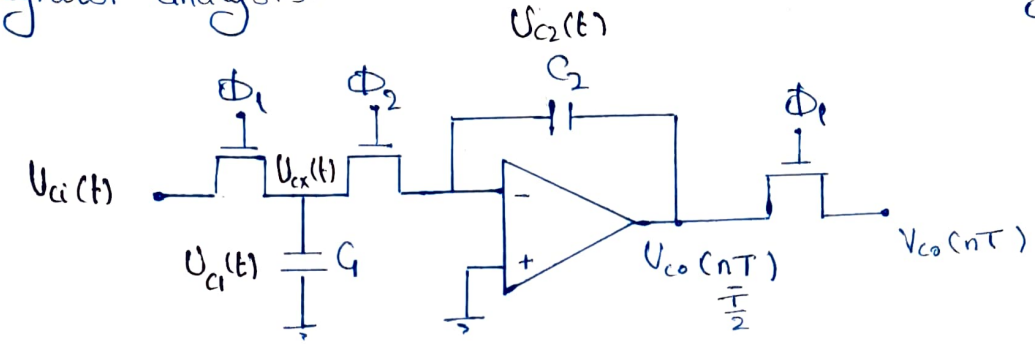


$$\tau = R_1 C_2 = \frac{C_2}{f_s C_1}$$

↳ ratio of Caps
∴ matched Caps
∴ Very precise.

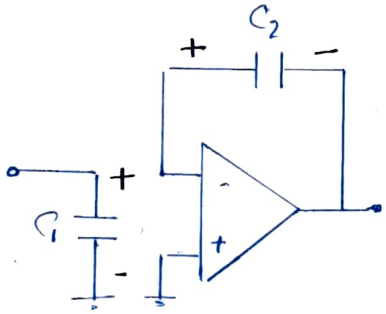
From Crystal osc and PLL
Very precise and fixable

(5) DT integrator analysis.

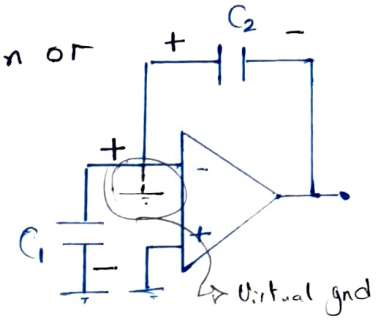


this Circuit has 2 mode

① Φ_1 (Sample)



② Φ_2 (update)



We analyze this Circuit either in Charge domain or Voltage domain

But, take Care of the Charge polarity

1 Charge domain: Total Charge in Φ_2 = total Charge in Φ_1

$$\therefore Q_{\Phi_2} = -C_2 V_{co}(nT)$$

$$\therefore Q_{\Phi_1} = -C_2 V_{co}(nT-T) + C_1 V_{ci}(nT-T)$$

$$\therefore -C_2 V_{co}(nT) = -C_2 V_{co}(nT-T) + C_1 V_{ci}(nT-T)$$

$$\therefore V_o(n) = V_o(n-1) - \frac{C_1}{C_2} V_i(n-1) \rightarrow \text{normalized by } T$$

$$\boxed{\mathcal{Z}\{x(n-m)\} = z^{-m} X(z)}$$

$$\therefore V_o(z) = z^{-1} V_o(z) - \frac{C_1}{C_2} z^{-1} V_i(z)$$

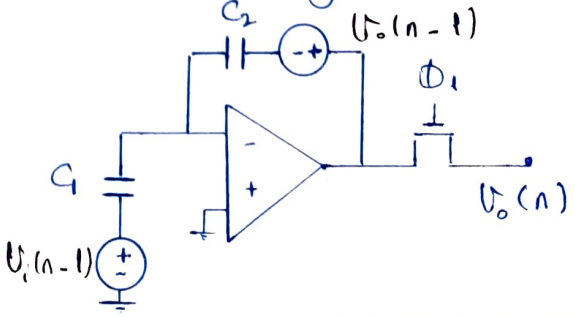
$$\therefore H(z) = \frac{V_o(z)}{V_i(z)} = -\frac{C_1}{C_2} \frac{1}{z-1}$$

2 Voltage domain

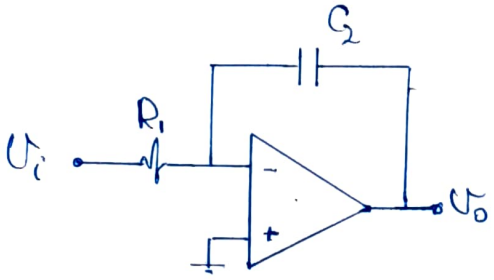
- replace every charged Cap with an uncharged Cap in Series with a Voltage Source (in Series with Same polarity)
- apply Superposition

$$V_o(n) = -\frac{C_1}{C_2} V_i(n-1) + V_o(n-1)$$

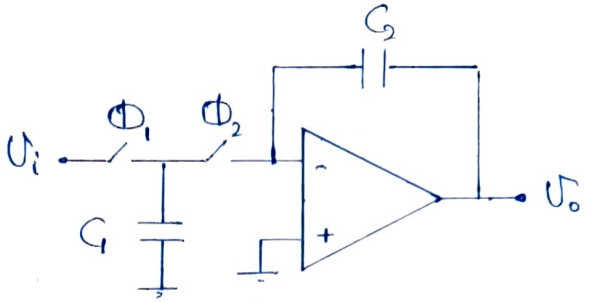
$$\therefore V_o(z) = z^{-1} V_o(z) - \frac{C_1}{C_2} z^{-1} V_i(z)$$



(6) CT Vs DT Integrator Step response.

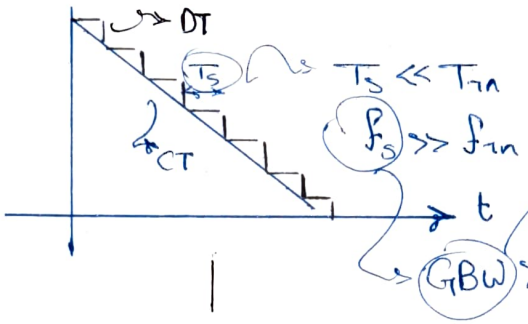


$$V_{out} = -\frac{1}{R_1 C_1}\int V_{in}\,dt$$



$$V_{out}[n] = -\frac{C_1}{C_2} V_{in}[n-1] + V_{out}[n-1]$$

(7) CT Vs DT Integrator Frequency response



$T_s \ll T_{in}$

$f_s \gg f_{in}$

→ higher GBW
∴ higher Power

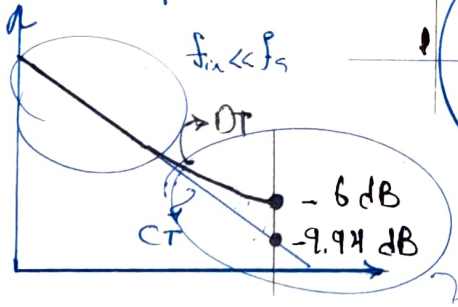
GBW >> f_s

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{\delta R_1 C_1}$$

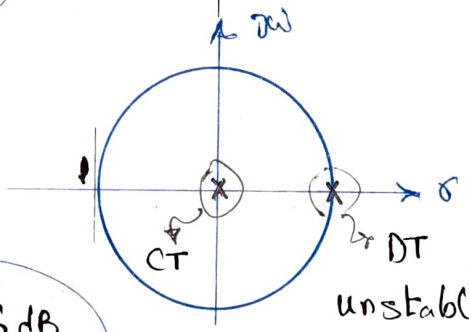
$$\frac{V_{out}(z)}{V_{in}(z)} = -\frac{C_1}{C_2}\frac{1}{z-1}$$

$z \to z_p = 1$

$\delta_p = 0$



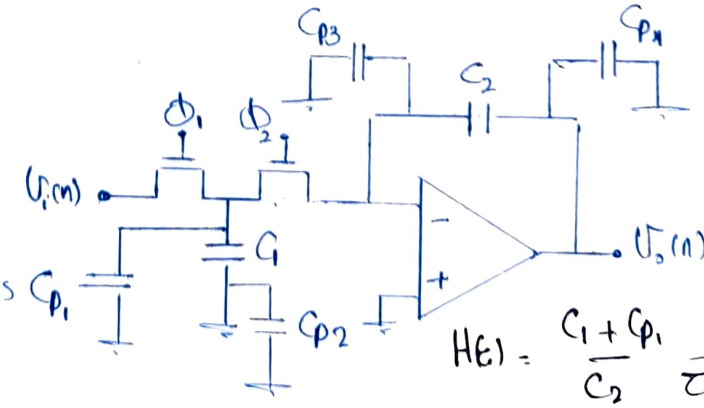
→ f_{in} increases



unstable System

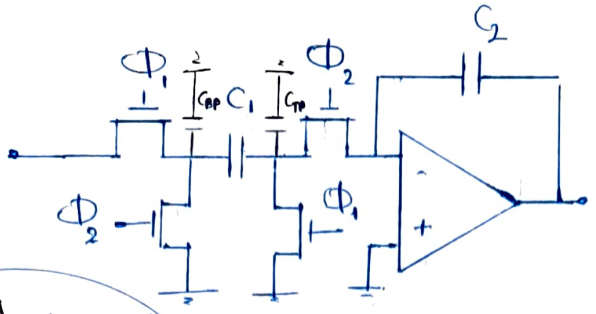
(8) Parasitic (Stray) Sensitivity.

- The Parasitic (Stray) Cps Can be problematic if they Contribute to Charge Sharing as C_{p1}
  - → Not Well Controlled
  - → Partially non-linear due to the DIS Junction Capacitance of the Switches

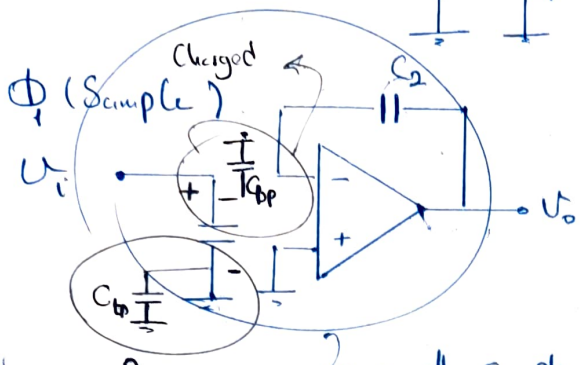


$$H(z) = \frac{C_1 + C_{p1}}{C_2}\frac{1}{z-1}$$

(a) Non-Inverting parasitic-insensitive

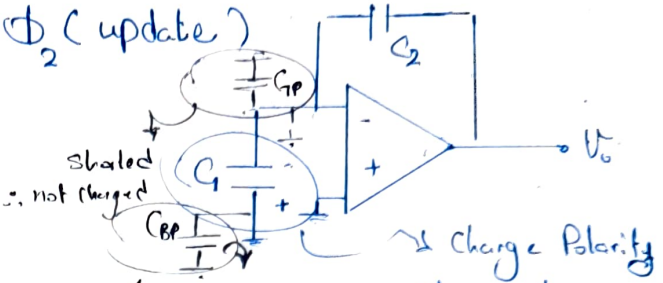


The solution idea is: Parasitic caps dump their charge to gnd or do not charge at all



↳ shorted
∴ not charged

↳ in the sample phase the C_{TP} is shorted to gnd and C_{BP} is charged

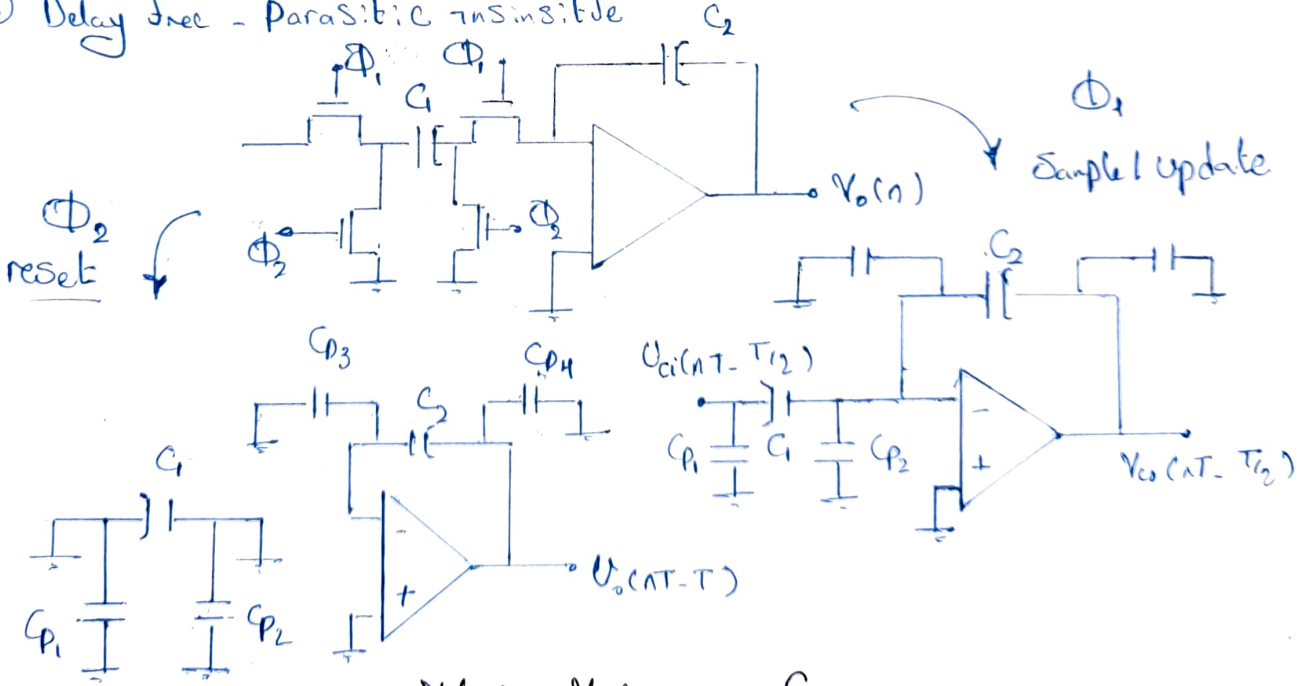


↳ dump its charge to gnd

↳ Charge Polarity changed
∴ non-inverting

$$\therefore H(z) = \frac{C_1}{C_2}\,\frac{z^{-1}}{1-z^{-1}} = \frac{C_1}{C_2}\,\frac{1}{z-1}$$

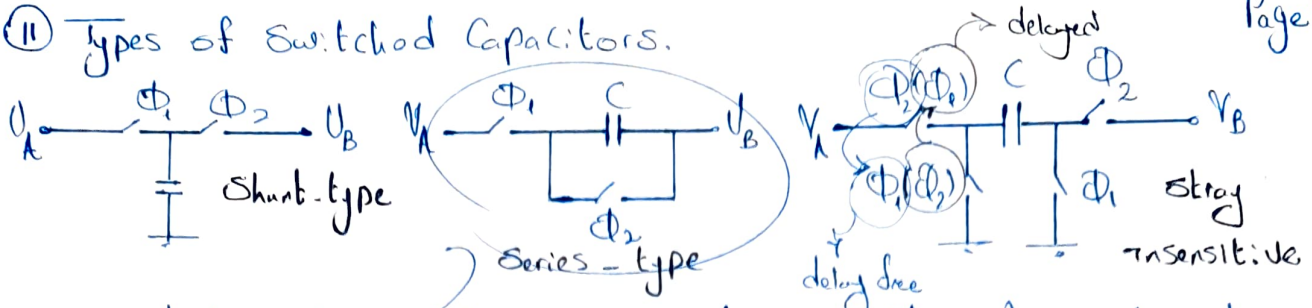
(b) Delay free - parasitic insensitive



$$V_o(n) = V_o(n-1) - \frac{C_1}{C_2}V_i(n)$$

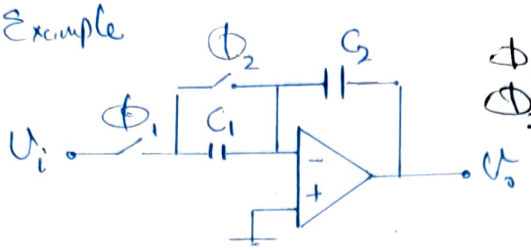
$$\therefore H(z) = -\frac{C_1}{C_2}\,\frac{1}{1-z^{-1}}$$

(11) Types of Switched Capacitors.

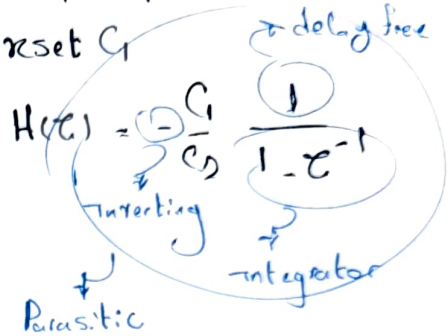


- Shunt- and Series-type are simple and cheap to implement
- Stray-insensitive SC requires 2 more switches

Example



Φ_1 Sample/update
Φ_2 reset C_1

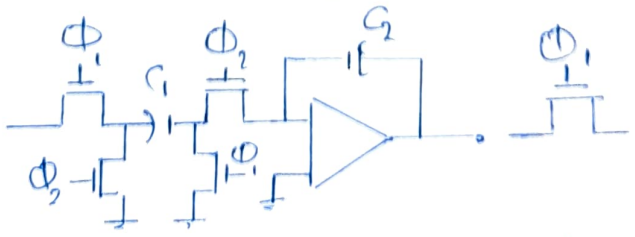


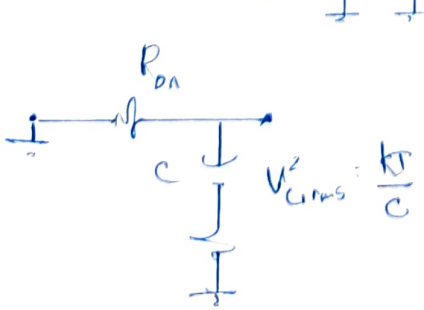
(12) Noise in SC Circuits

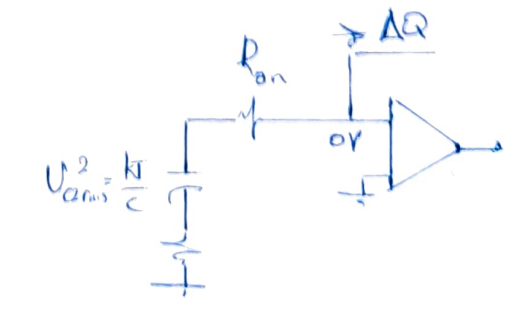
- for Sampled Noise: Noise density increase (noise folding) but total integrated noise power remains constant
- As the Circuit has two mode of operation, it also has 2 noise Components (Sampled in Φ_1 and CT in Φ_2)
- SC noise Cannot be Simulated using AC noise Simulation
  → use transient noise or Pnoise Analysis

$$\Delta Q_{rms}^2 = \Delta Q_{1(rms)}^2 + \Delta Q_{2(rms)}^2 = 2kTC$$

$$V_{in(rms)} = \sqrt{\frac{2kT}{C}}$$







(13) OTA offset Voltage.

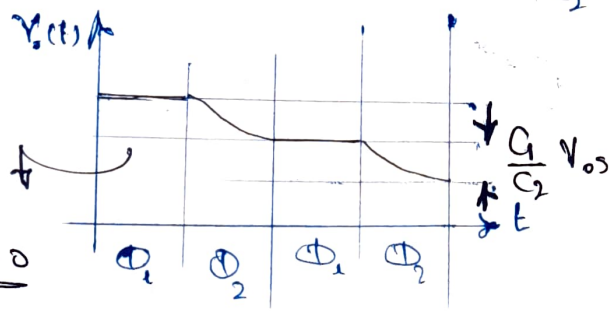
- For the circuit shown in the previous page

$$\Sigma Q(\Phi_1) = (V_o(n) - V_{os})C_2 + V_i(n)C_1$$

$$\Sigma Q(\Phi_2) = (V_o(n+1) - V_{os})C_2 - V_{os}C_1$$

$$\therefore V_i = 0 \rightarrow V_o(n+1) - V_o(n) = \frac{C_1}{C_2} V_{os} \rightarrow V_o(z) = \frac{C_1}{C_2} \frac{1}{z-1} V_{os}$$

(integrator)



even the circuit has no input ∴ the output will change

Note that $V_i = 0$

→ the output will change till it hits one of the rails

We can solve this using some techniques such

1 Auto-Zeroing.

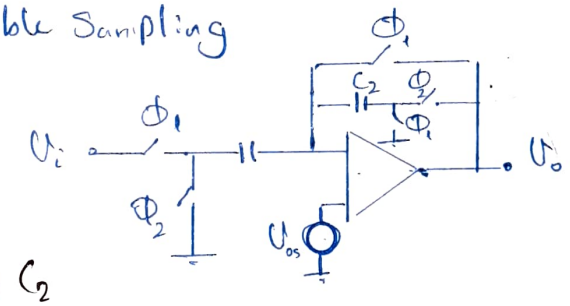
- Auto Zeroing (AZ) eliminates Voltage and reduces 1/f noise.

A.k.a Correlated double Sampling

$$\Sigma Q(\Phi_1) = [V_i(n) - V_{os}]C_1 - V_{os}C_2$$

$$\Sigma Q(\Phi_2) = -V_{os}C_1 + (V_o(n+1) - V_{os})C_2$$

$$\therefore H(z) = \frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2} z^{-1}$$



2 Chopping

Chopping is a technique used to improve accuracy.

- Sensitive signals are modulated to frequency bands where the signal processing is free of errors
- Mitigates the effect of DC offset, flicker noise, etc

- In differential circuits, Chopping is implemented easily by alternating between the differential branches