Analog Integrated Systems Design

LAB No.3 - Data Converters Specifications

- Objective

  - To be familiar with the leading manufacturers of data converters.
  - To be able to search for and read manufacturers datasheets.
  - To be familiar with the leading forums (conferences and journals) in IC design.
  - To be able to search for and read technical research papers.
  - To be able to analyze and compare data converters specifications.
  - To appreciate the gap between the FoM of industrial data converters and published papers.

- ADCs Comparison

Select one ADC from ADI, one ADC from TI, and one ADC from papers published in one of the following top forums (in the last 10 years):

- Journal of Solid State Circuits (JSSC)
- International Solid-State Circuits Conference (ISSCC)
- VLSI Symposium

The ADCs you select must meet the specifications below.

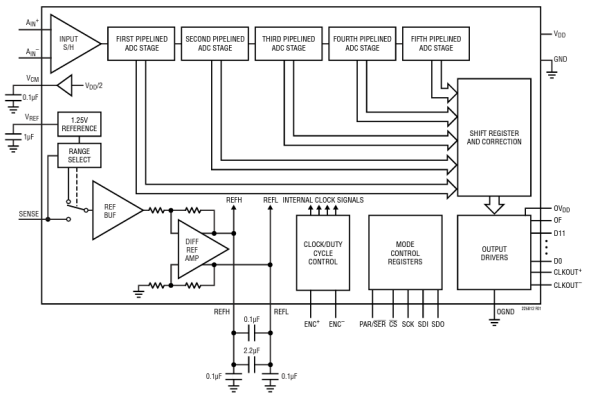
No. of bits	12
Sample rate	$\geq$ 1 MSps
No. of channels	1
Input type	Differential
Max DNL	$<$ 1 LSB
Max INL	$<$ 1 LSB
Power consumption	Minimum

Read the datasheets/papers and compare the following for the selected ADCs in a table.

ADI - LTC2256-12

12-Bit, 25Msps Ultralow Power 1.8v ADCs

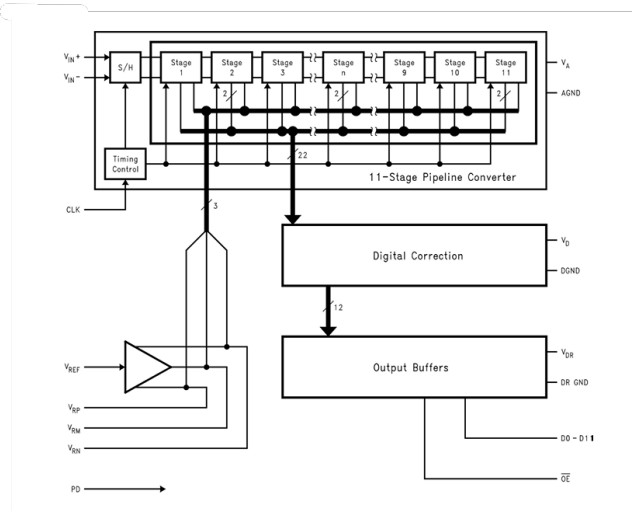
Architecture	Pipelined	Price	12.27 $
Min power supply (V)	1.7 V	Peak-to-peak input range (V)	1 – 2 V
Power consumption at 1 MSps (mV)	47 mW	Max DNL (LSB)	0.1 LSB
ENOB (bit)	11.41 bit	Max INL (LSB)	0.3 LSB
SNR (dB)	70.5 dB	SINAD (dB)	70.5 dB
SFDR (dB)	88 dB	Digital output format	Parallel
Internal reference	Yes	Internal sampling clock	Yes
FoM_W (fj/step)		FoM_S (dB)	



TI - ADC12010

12-Bit, 10MSPS, 160mW A/D

Architecture	Pipelined	Price	5.04 $
Min power supply (V)	4.75 V	Peak-to-peak input range (V)	$-0V$ to $(V_A - 0.5V)$
Power consumption (mV)	160 mW	Max DNL (LSB)	±0.3 LSB
ENOB (bit)	11.4 bit	Max INL (LSB)	±0.5 LSB
SNR (dB)	70 dB	SINAD (dB)	70 dB
SFDR (dB)	92 dB	Digital output format	Parallel
Internal reference	No	Internal sampling clock	No
FoM_W (fj/step)		FoM_S (dB)	



IEEE - A 12b 250MS/s Pipelined ADC with Virtual Ground Reference Buffers

Architecture	Pipelined	Price	N/A
Min power supply (V)	1.2 V	Peak-to-peak input range (V)	1.5 V
Power consumption (mV)	49.7 mW	Max DNL (LSB)	$-0.86/+0.52$ LSB
ENOB (bit)	10.84 bit	Max INL (LSB)	$-0.90/+1.08$ LSB
SNR (dB)	N/A	SINAD (dB)	67 dB
SFDR (dB)	84.6 dB	Digital output format	Parallel
Internal reference	No	Internal sampling clock	No
FoM_W (fj/step)	108.5 fj/step	FoM_S (dB)	160 dB