Mini-Project No. 3

Fully Differential Folded Cascode OTA

- Objective

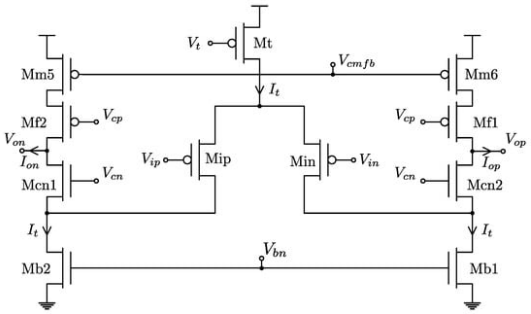
  Design a fully-differential folded cascode OTA with capacitive feedback that meets the specifications below.

Supply Voltage	1.2 V	Closed Loop Gain	2
Phase Margin	$\geq 70^{o}$	Closed Loop BW	10 MHz
Differential Output Swing	$\geq 0.6\ V\_pk - to - pk$	OTA Current Consumption	≤ 80 uA
CM Input Range	$0 \geq CM > 0.6$ V	CMFB Current Consumption	≤ 40 uA
Load	1 pF	DC Loop Gain	50 dB

- Steps

01 | Since CM input range is close to GND rail → I used PMOS input Stage

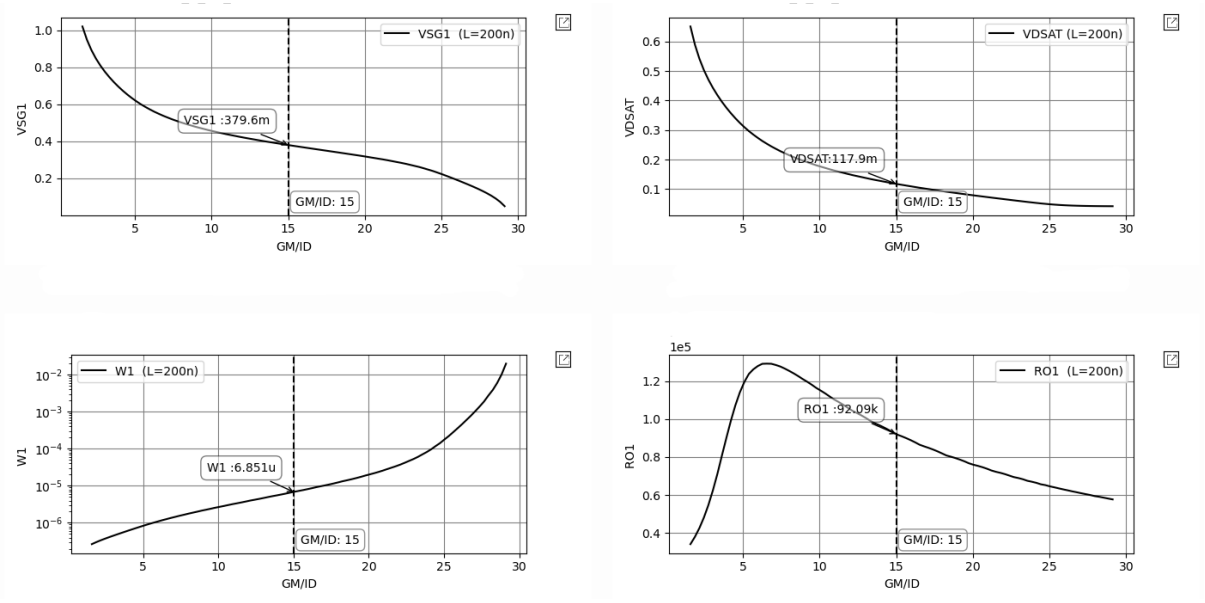
02 | Using the following topology



03 | Since this is a relatively difficult design, we will directly assume values for L and gm/ID based on designer's experience and folded cascode trade-offs matrix.

A | Input Pair

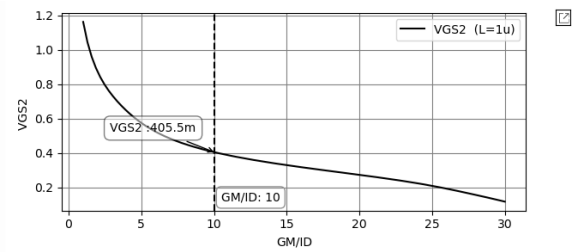
<u>Assume Short L = 0.2 um and gm/ID = 15, This maximizes the GBW (good efficiency) and minimizes the input capacitive loading (avoid reducing the DC LG).</u>

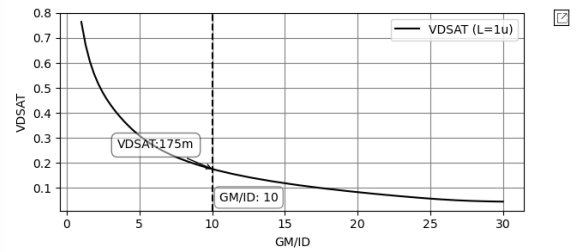


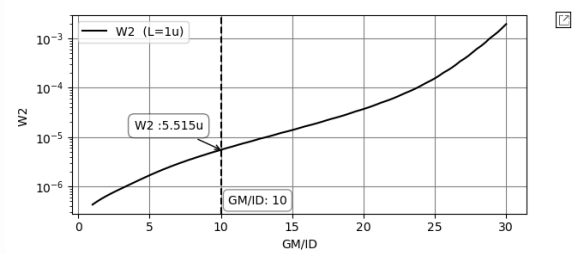
B | Current Mirrors

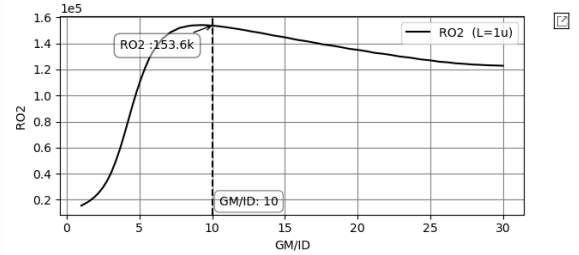
For the current source transistors use relatively long L and bias them in SI, L = 1 um and gm/ID = 10, These transistors contribute significant offset and noise. A large gm will not help the gain but will increase the noise.

- NMOS Current Mirror

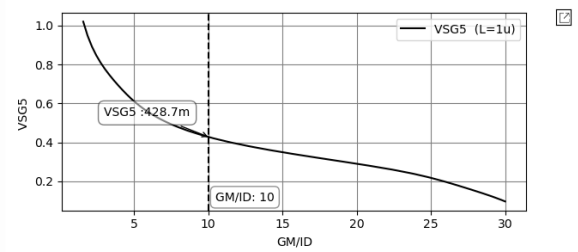


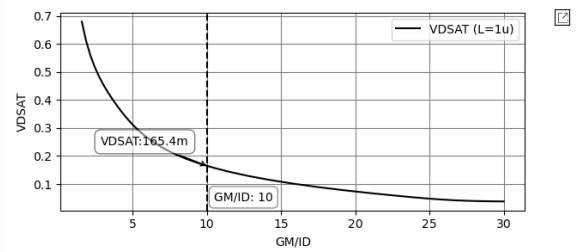


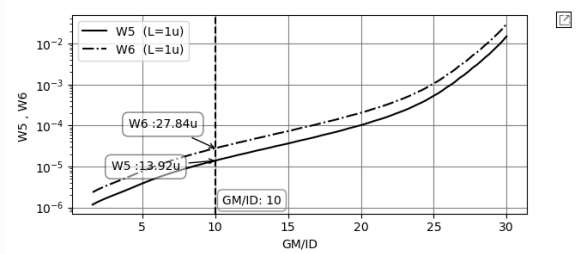


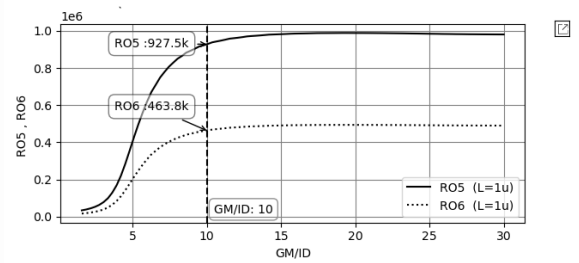


- PMOS Current Mirror





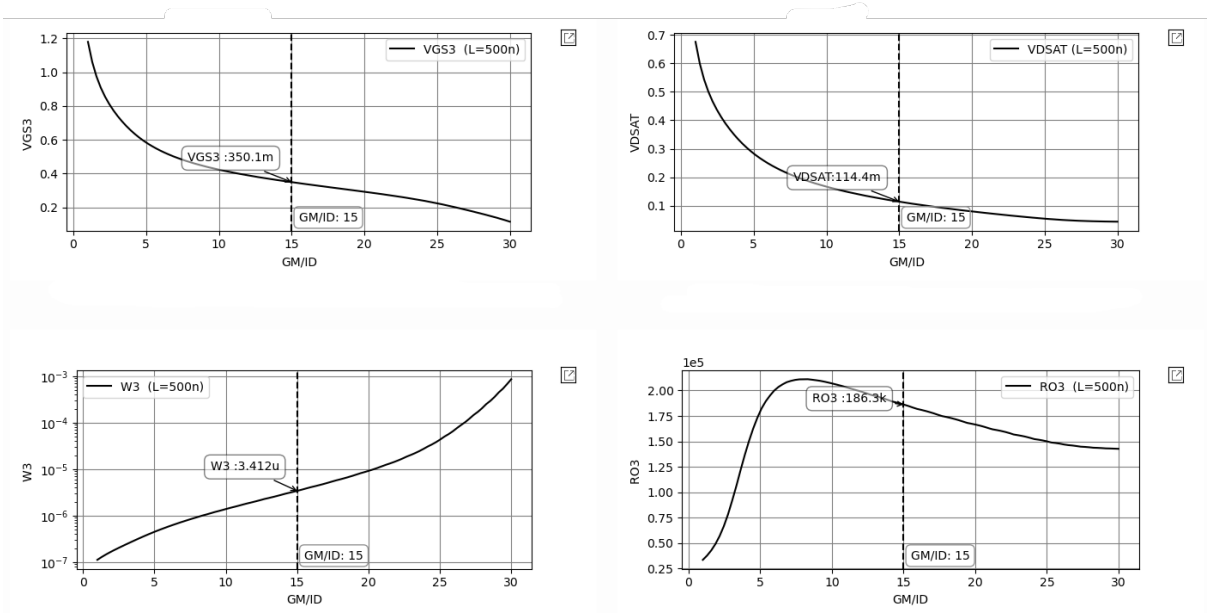




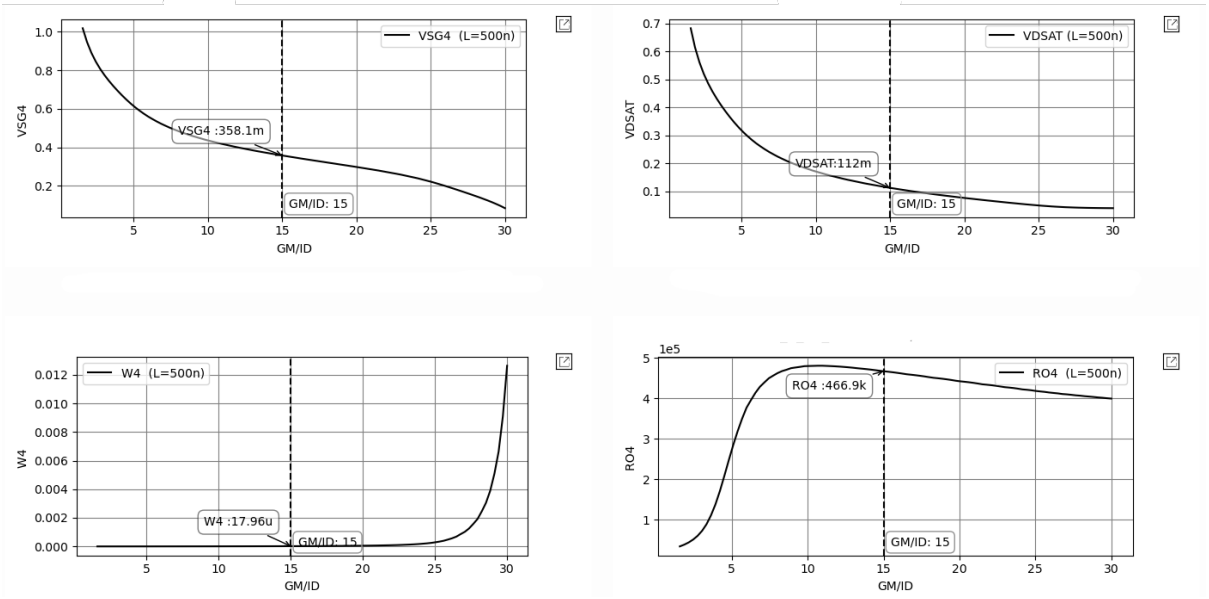
C | Cascode Transistors

For the cascode transistors use moderate L and bias them in MI or WI, L = 0.5 um and gm/ID = 15, These transistors do not contribute significant offset and noise, so they don't need to be large. A large gm helps the gain and doesn't increase the noise.

- NMOS Cascode



- PMOS Cascode

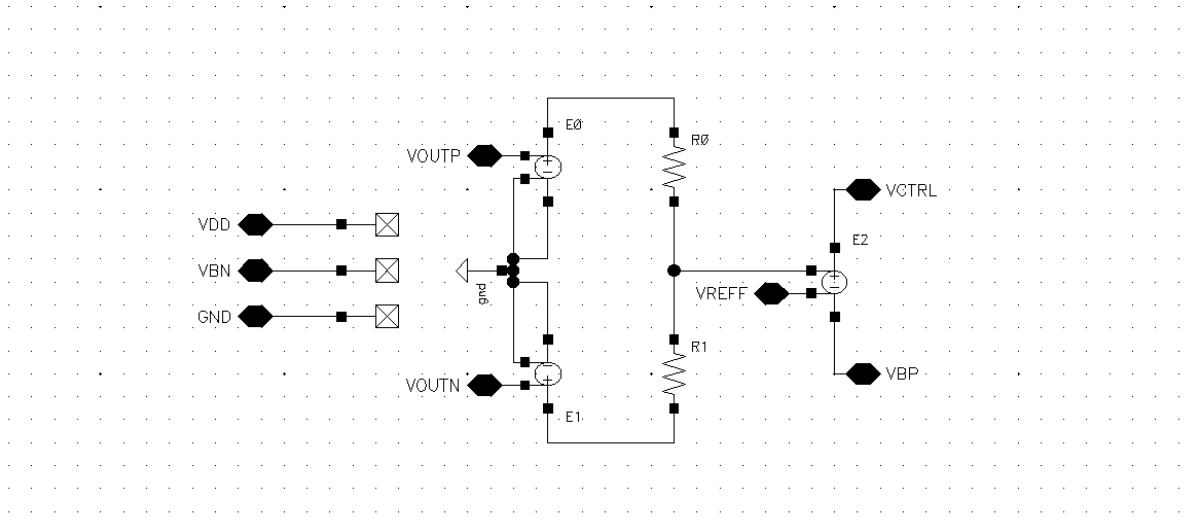


04 | From the assumed V*, select suitable biasing for the cascode transistors (VCASCP and VCASCN).

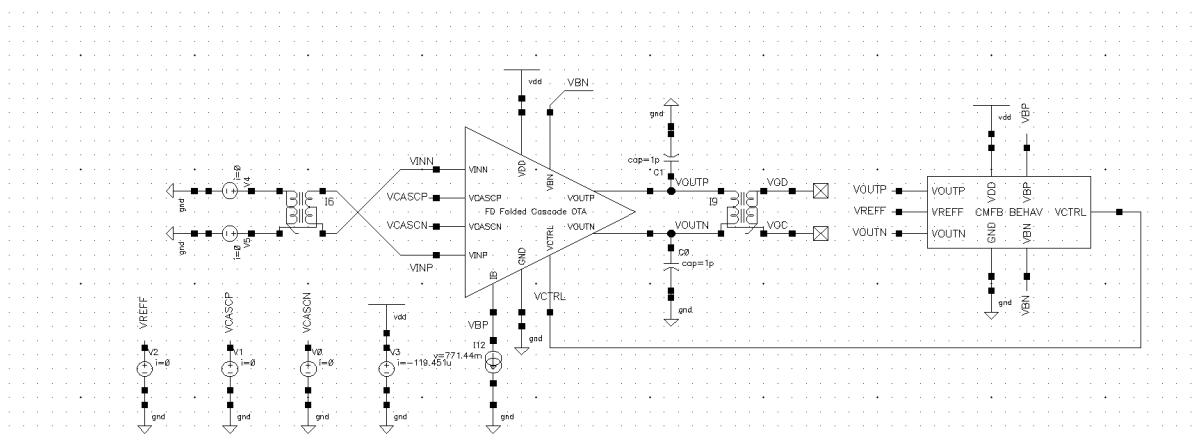
$$\text{VCASCN} = V_{GS3} + V_2^* = 350\ \text{mV} + 200\ \text{mV} = 550\ \text{mV}$$

$$\text{VCASCP} = -V_{SG4} - V_5^* + V_{DD} = -358.1\ \text{mV} - 200\ \text{mV} + 1.2 = 640\ \text{mV}$$

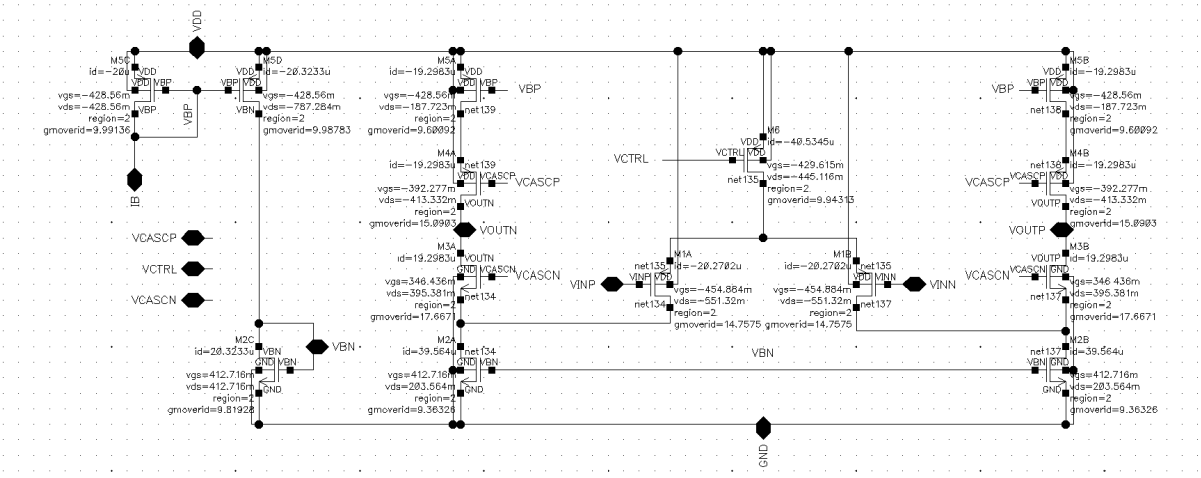
05 | We will start with a behavioral CMFB network similar to the one shown below. We use ideal buffers to avoid loading the OTA output with the CM sensing resistors. Note that we don't need high gain in the CMFB loop; thus, we use a gain = 1 in the error amplifier

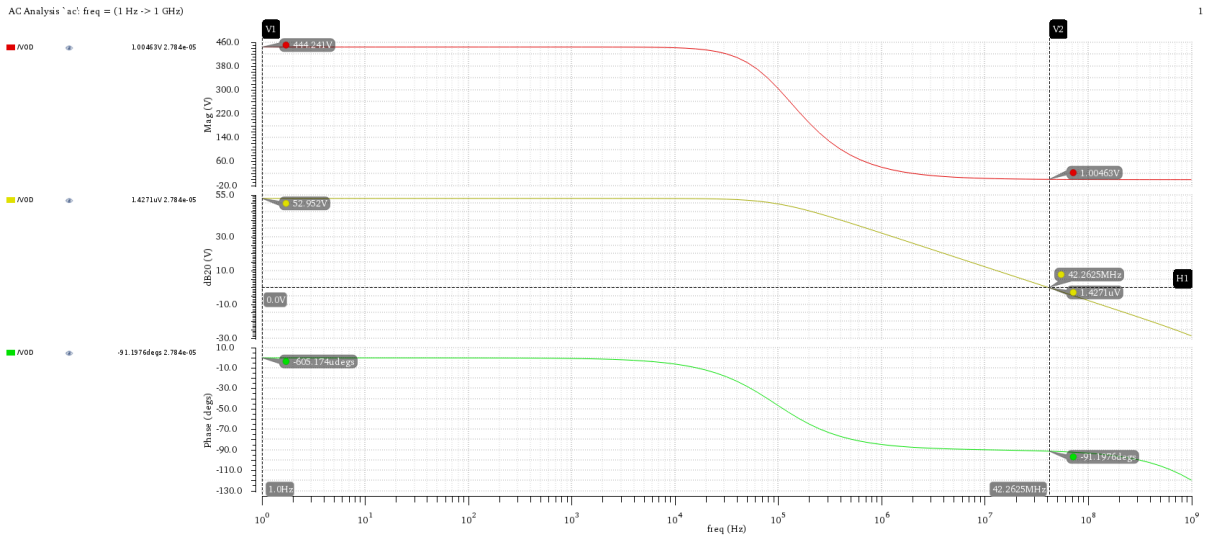


06 | Using calculated values and the behavioral CMFB in the following TB to get the initial points to tune design



07 | Apply DC operating points and AC analysis





08 | Since $A_{CL} = 2 = \frac{1}{\beta} \rightarrow \beta = \frac{1}{2} \rightarrow$ and $LG \approx \beta A_{OL} = 50\ dB \rightarrow A_{OL} \geq 56\ dB$

Since the obtained $A_{OL} = 52.9\ dB \rightarrow$ And $A_{OL} = g_{m1} * [g_{m5} r_{o5} r_{o4} \parallel g_{m2} r_{o2} r_{o3}] \rightarrow$ increase L_3 and $L_4 = 1.5\ um$