Analog Integrated Systems Design

Lecture 11
Comparators

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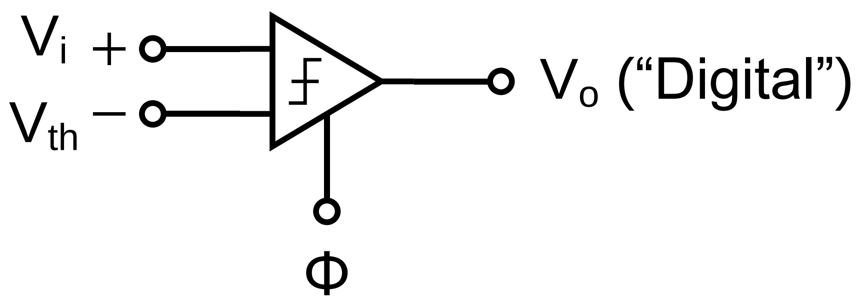
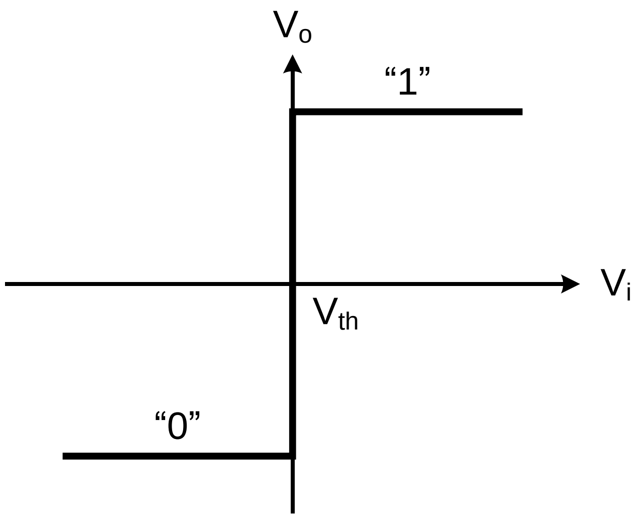
Comparator

- The comparator circuit is the location where the digital decision is made
  - "Where nature turns into bits"
- Detects the polarity of a differential analog input signal
  - Generates a digital output (1 or 0) accordingly
- Or compares a SE input to a threshold (reference) voltage
  - Threshold-crossing detector



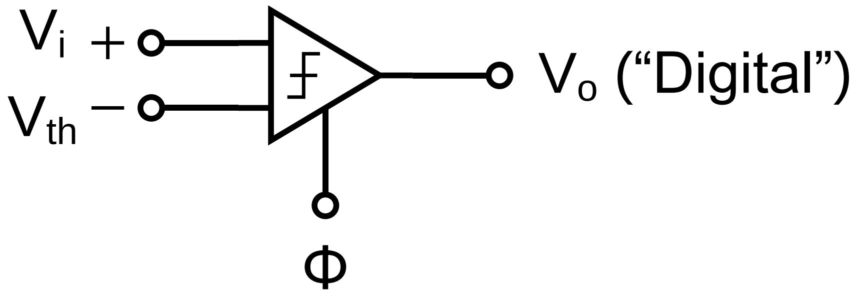
Circuit symbol



Transfer characteristic (ideal)

Comparators in ADCs

- Every analog-to-digital converter contains at least one comparator
- There are many different comparator implementations
  - There is NO universal "one design fits all" comparator
- Main design trade-off: accuracy and speed vs power consumption



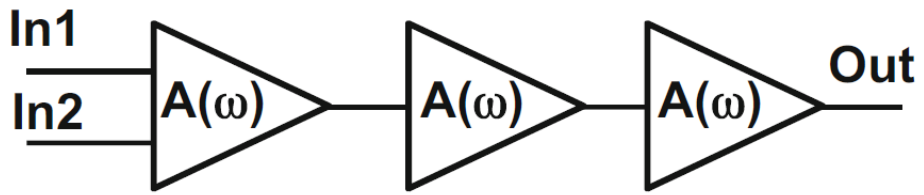
[Y. Chiu, EECT 7327, 2014]

Comparator Requirements

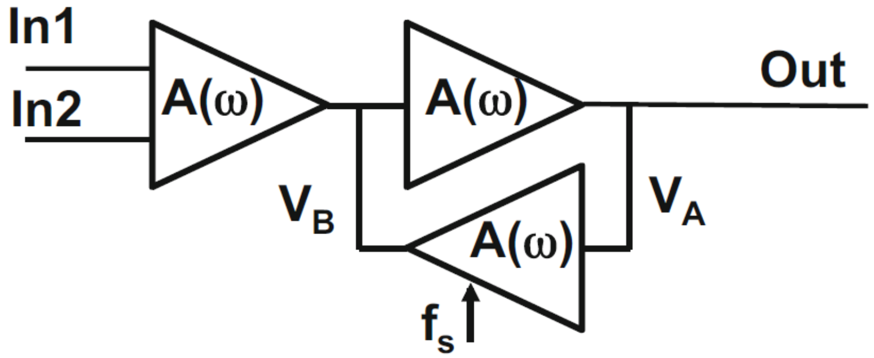
- Large amplification (fine resolution / high sensitivity)
  - Needs to translate mV or uV differential input to ‘0’ and ‘1’
- Wide bandwidth (high speed)
- Accuracy
  - Low input offset and low noise
- Low power consumption
- No memory (hysteresis)
  - Previous comparator decision should not affect the following
- No metastability
  - Any decision is better than no decision!
- Wide common mode input range
- High CMRR

Comparator Topologies

- Straight-forward amplification
  - Simple
  - Relatively slow



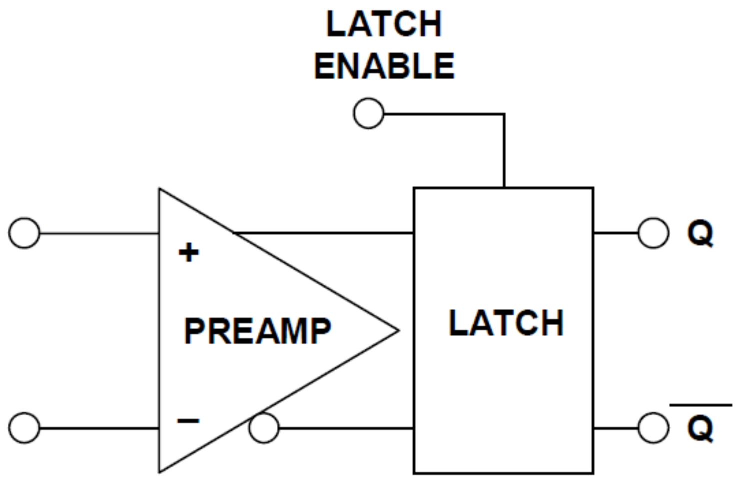
- **Latch comparator**
  - **A.k.a. clocked / dynamic / regenerative comparator**
  - **Clock is required**
  - **Built-in S/H**



[M. Pelgrom, 2017]

Pre-amplification

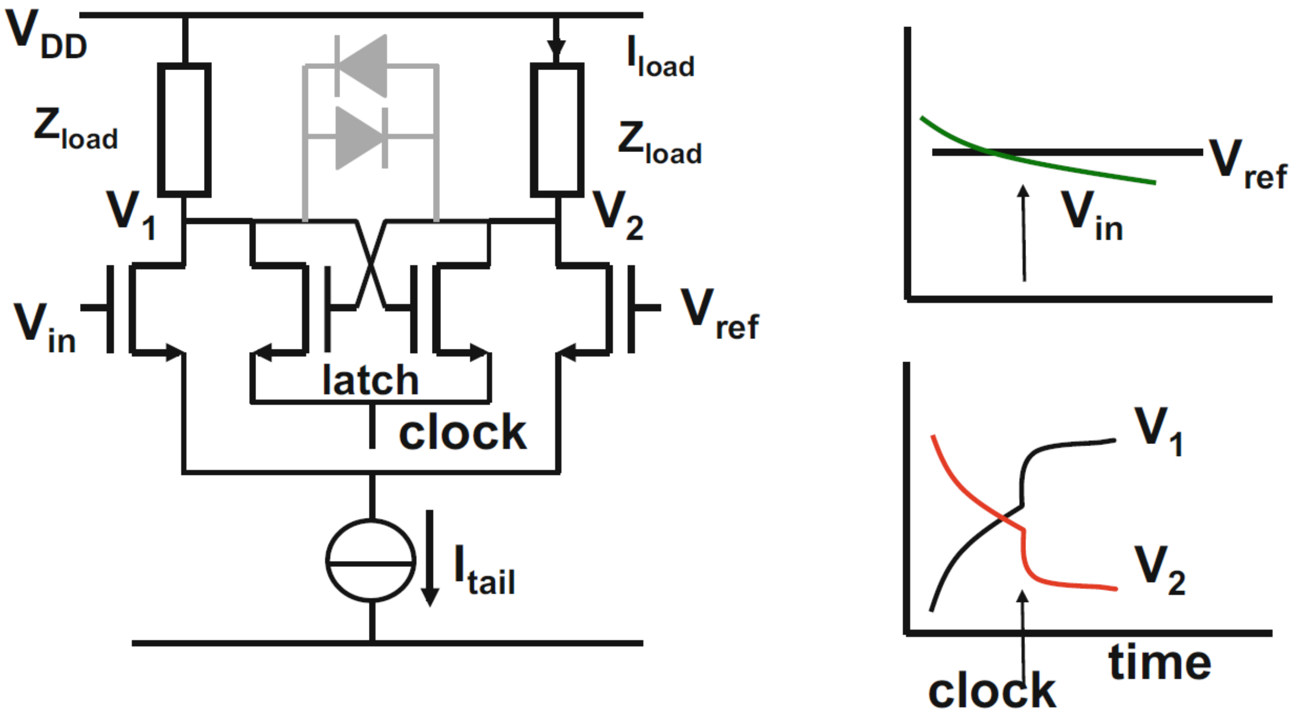
- A pre-amplifier is used before the regenerative section of the comparator is activated
  - Reduces the influence of mismatch in the regenerative section
  - Creates a form of isolation between the regeneration process and the input sources
  - No reason to boost the DC-gain to very high values (usually ≤ 10)
    - Low gain allows operations at high speed (large bandwidth)
    - Just sufficient to suppress latch mismatch and noise
- Most comparators use an input differential pair as a pre-amplifier



[W. Kester, ADI, 2005]

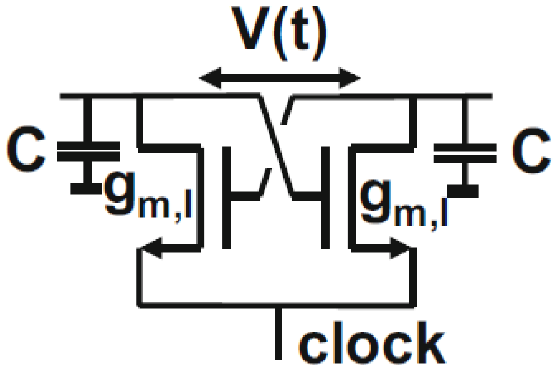
Regenerative Comparator Example

- After some amplification a positive feedback latch activated by a clock pulse will turn the latch on
  - The latch will amplify the small input voltage difference to a large signal



[M. Pelgrom, 2017]

Regenerative Latch Delay



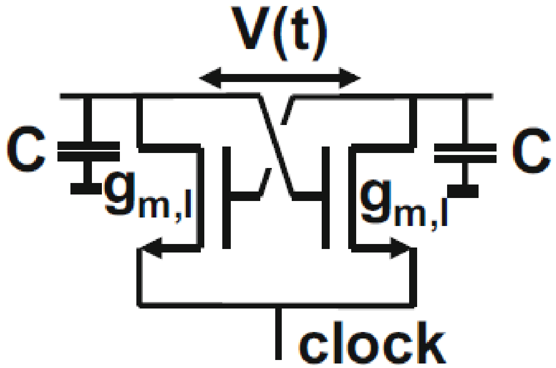
Regenerative Latch Delay

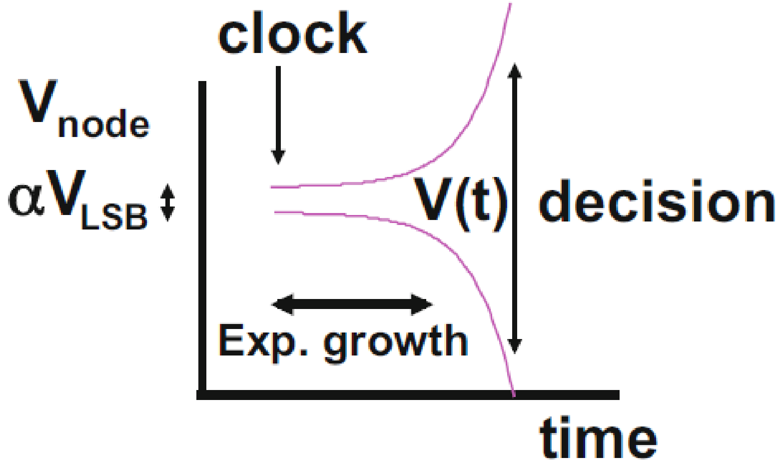
- Assume the pre-amplified latch input voltage $= \Delta V_{in} = \alpha V_{LSB}$ $(0 < \alpha < 1)$

$$\tau \approx \frac{C}{g_{m,l}}$$

$$V(t) = \Delta V_{in} e^{+t/\tau}$$

- The exponential signal growth makes a latch a fast decision element in a regenerative comparator
- The exponential growth will continue until some non-linear limiting mechanism takes action (e.g., approaching power rails)



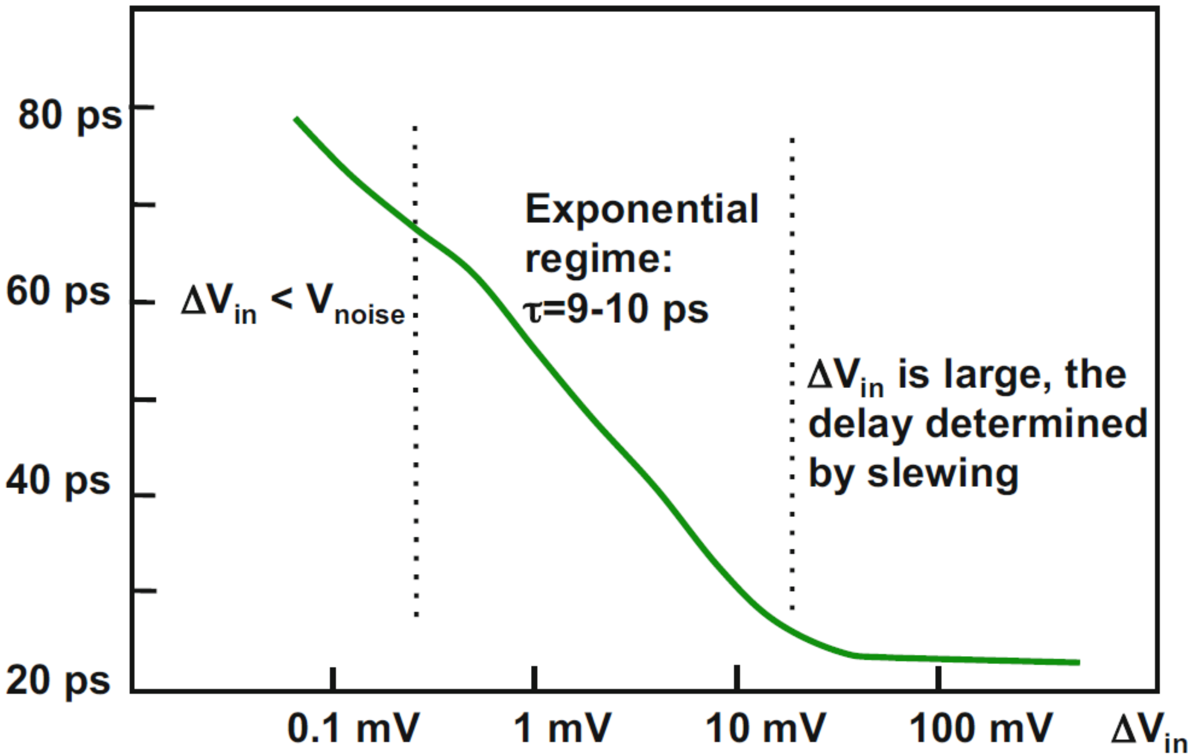


[M. Pelgrom, 2017]

Comparator Delay Example

- The time a comparator or latch needs to form a digital signal depends on the initial over-drive voltage
  - The input differential voltage determines the delay of the comparator

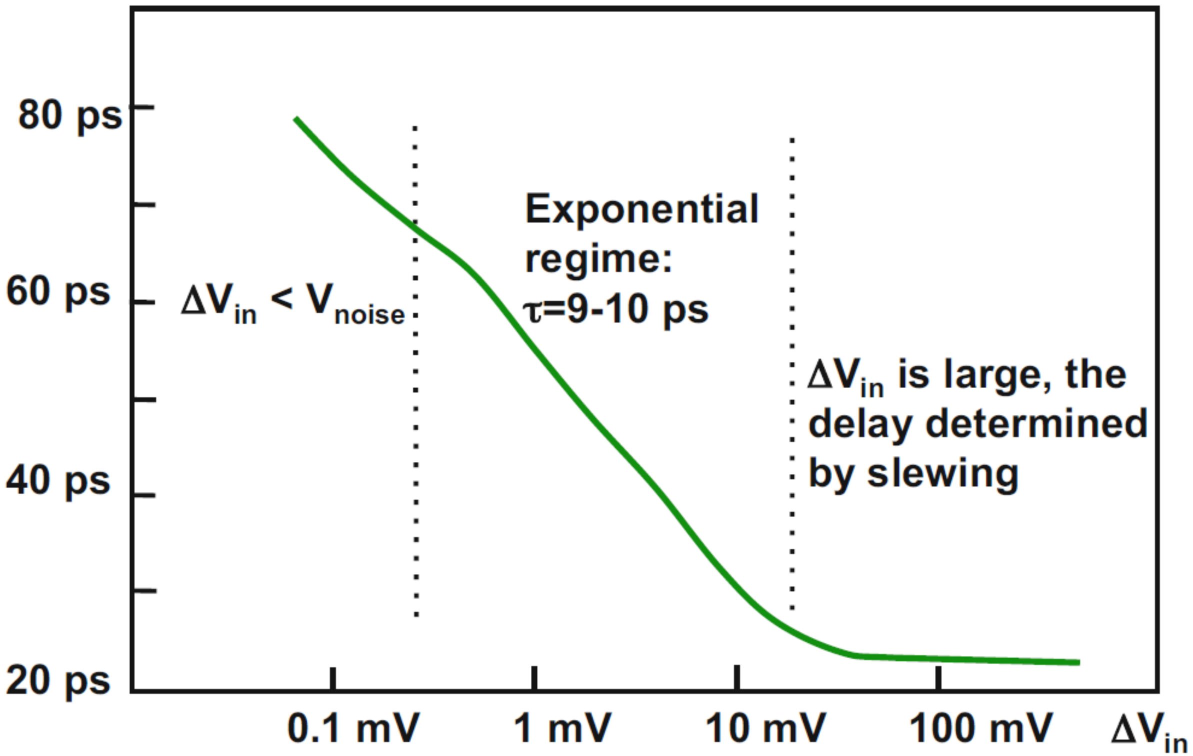
$$V(t) = \Delta V_{in} e^{+t/\tau} \rightarrow \; t_d = \tau \ln \frac{V_{FS}}{\Delta V_{in}} = \tau(\ln V_{FS} - \ln \Delta V_{in})$$



[M. Pelgrom, 2017]

Metastability

- For very small overdrive voltages, the comparator cannot reach a decision in the limited time of a clock period (T_S)
- The comparator will not generate a clear “zero” or “one” output level after time T_S
- The succeeding logical circuitry will behave ambiguously



Bit-Error Rate (BER)

- Assume the pre-amplified latch input voltage = αV_{LSB} $(0 < \alpha < 1)$
- Assume ambiguity happens when $V(T_S) < V_{FS}$

$$V(T_S) = \alpha V_{LSB} e^{+T_S/\tau} < V_{FS}$$

$$\alpha_{min} = \frac{V_{FS}}{V_{LSB}} e^{-T_S/\tau} = 2^N e^{-T_S/\tau}$$

- Assume V_{in} is uniformly distributed: $0 < \alpha < 1$

$$BER = \alpha_{min} = 2^N e^{-T_S/\tau}$$

Bit-Error Rate (BER)

- Assume V_{in} is uniformly distributed: $0 < \alpha < 1$

$$BER = \alpha_{min} = 2^N e^{-T_S/\tau}$$

- From a fundamental point of view the BER cannot be avoided completely
  - But can be made very small (10^{-13} is possible)
- Measures to improve the BER include:
  - Improving the latch speed with more current and smaller capacitances
  - Additional gain stages or a second latch
    - $\Delta V_{in} = \alpha V_{LSB}$ larger than V_{LSB} ($0 < \alpha < A$, where $A > 1$)
  - Using special decoding scheme to avoid large code errors in case of a metastable state

Comparator Offset Voltage

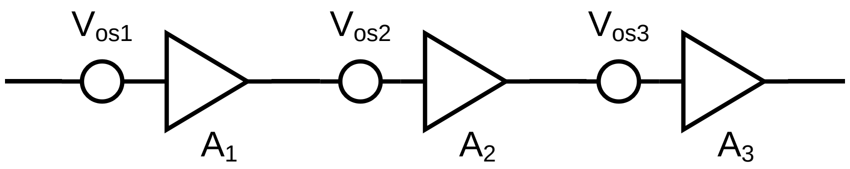
- In some types of ADCs the static random offset just generates a (random) DC-shift of the entire signal → offset error

- In other types of ADCs the input referred random offset is crucial because it impacts both INL and DNL
  - 0.5LSB > $3\sigma_{in,os}$

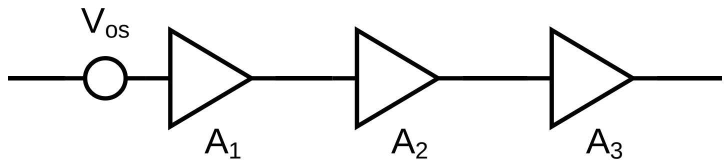
Static vs Dynamic Offset

- Offset voltage has static and dynamic components
  - Static offset:
    1. Systematic offset (due to systematic mismatch): can be minimized by good design and matched layout
    2. Random offset (due to random mismatch): reduced by using large devices but cannot be eliminated (Pelgrom's model)
    - Static offset is dominant in preamplifiers
  - Dynamic offset:
    - Due to imbalanced switching effects and capacitive load mismatch
    - Dynamic offset is dominant in latches

Multistage Preamplifier Offset



Individual stage



Total input-referred

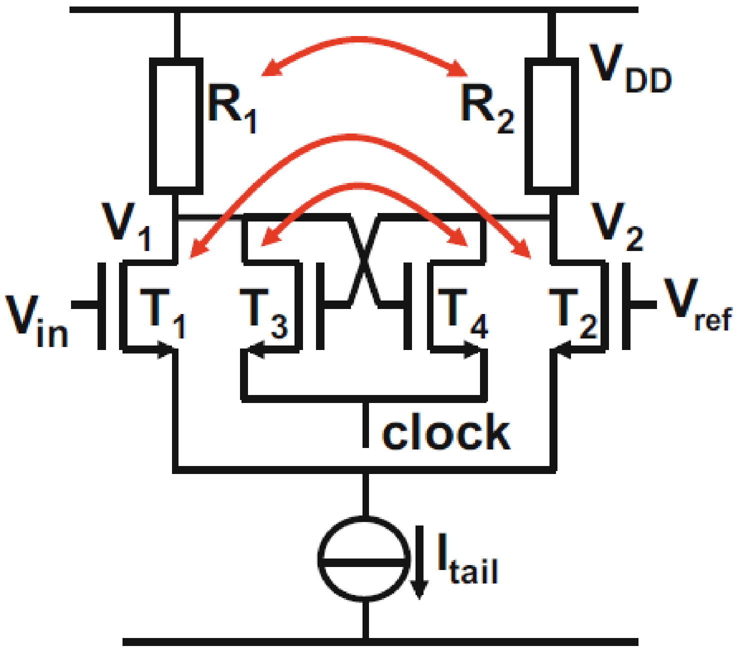
$$A_T = A_1 \cdot A_2 \cdot A_3$$

$$V_{os} = V_{os1} + \frac{V_{os2}}{A_1} + \frac{V_{os3}}{A_1 \cdot A_2}$$

 [Y. Chiu, EECT 7327, 2014]

Comparator Static Offset

$$\sigma_{Vin}^2 = \sigma_{VT,12}^2 + \frac{g_{m,34}^2}{g_{m,12}^2}\sigma_{VT,34}^2 + \frac{I_{load}^2}{g_{m,12}^2}\frac{\sigma_R^2}{R_{1,2}^2}$$

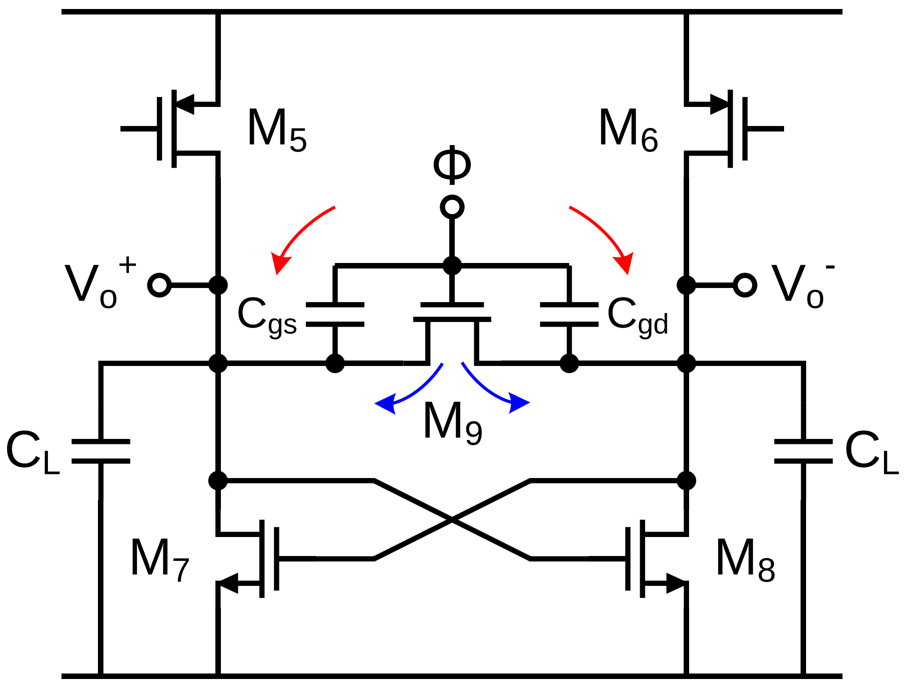


[M. Pelgrom, 2017]

Latch Dynamic Offset

- M5-6: input pair
- M7-8: cross-coupled load (regenerative)
- M9: reset switch

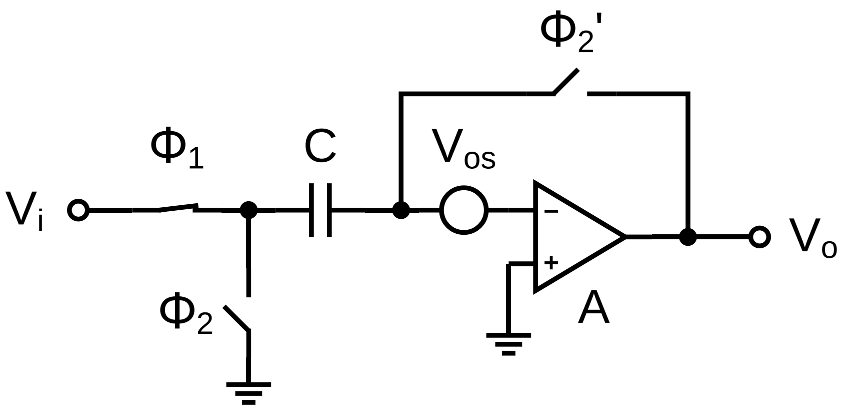
- Dynamic offset due to:
  - Imbalanced CI and CF
  - Imbalanced load capacitance
  - Mismatch between M_5 and M_6
  - Mismatch between M_7 and M_8
  - Clock routing



[Y. Chiu, EECT 7327, 2014]

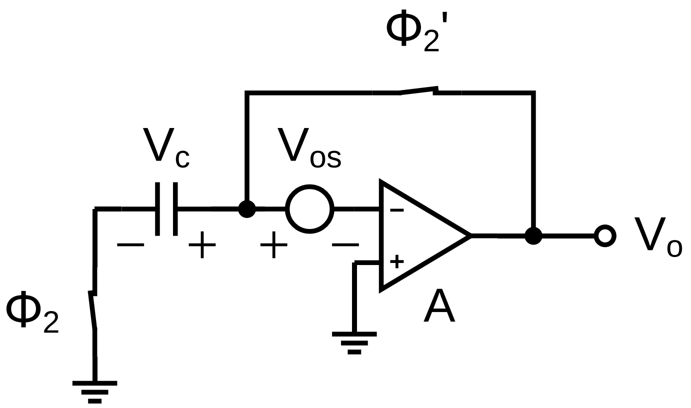
Input Offset Cancellation

- AC coupling at input with input-referred offset stored in C
- Two-phase operation
  - Phase (Φ2) is used to store offset



Input Offset Cancellation

- Offset Storage Phase – Φ_2
  - Closed-loop stability required (amplifier in unity-gain feedback)

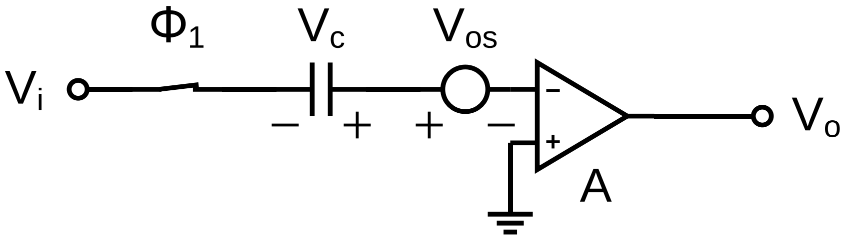


$$
\begin{aligned}
V_c &= -A(V_c - V_{os}) \\
&= \frac{A}{1+A} \cdot V_{os} \\
&\approx V_{os}
\end{aligned}
$$

<u>Ref</u>: J. L. McCreary and P. R. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques. I," *JSSC*, vol. 10, pp. 371-379, issue 6, 1975.

Input Offset Cancellation

- Amplifying Phase – Φ_1
  - Offset cancellation is incomplete if A is finite
  - Input AC coupling attenuates signal gain



$$V_o = -A(V_{in} + V_c - V_{os}) = -A\left(V_{in} - \frac{V_{os}}{1+A}\right)$$

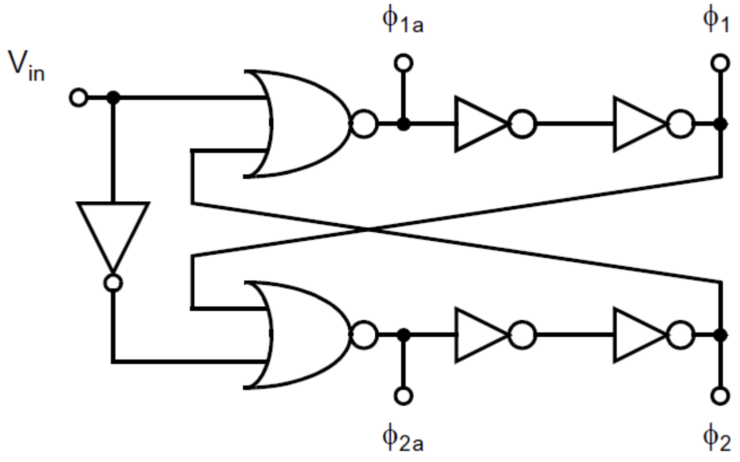
Input - referred offset :

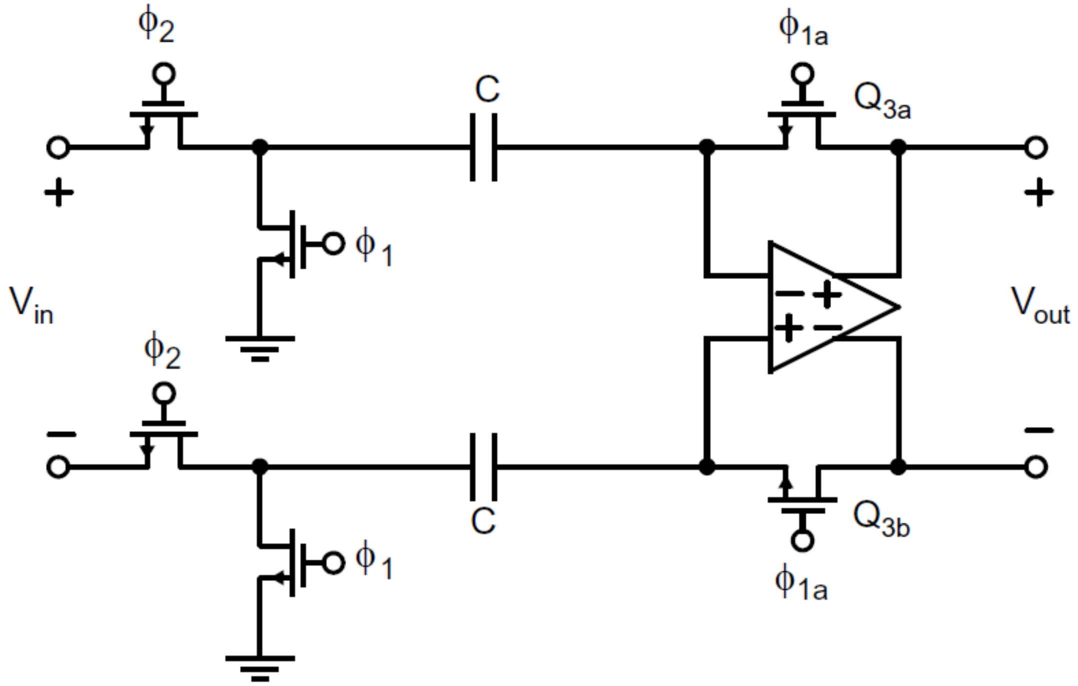
$$V_{os,in} = \frac{V_{os}}{1+A}$$

[Y. Chiu, EECT 7327, 2014]

Input Offset Cancellation

- Fully differential operation to mitigate charge injection and clock feedthrough errors.
  - Necessary for any high precision switched-capacitor integrated circuits

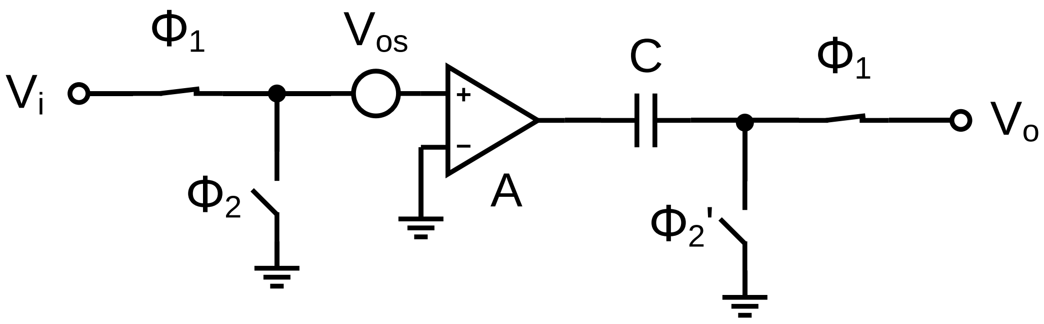




[Johns and Martin, 2012]

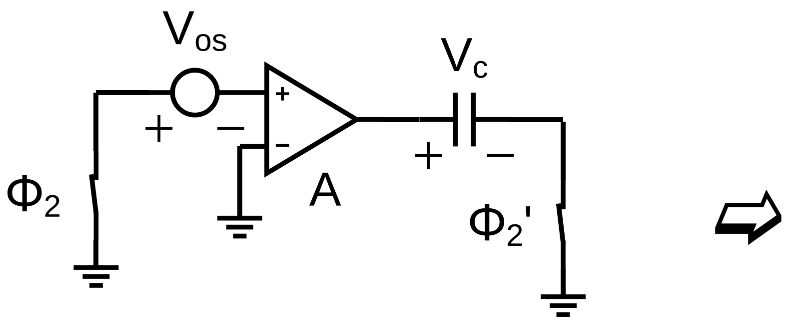
Output Offset Cancellation

- AC coupling at output with offset stored in C
- The gain (A) must be small and stable (independent of Vo)
- Does not work for high-gain amplifier



Output Offset Cancellation

- Offset Storage – Φ_2
  - Closed-loop stability is not required
  - CF (clock feedthrough) and CI (charge injection) of Φ2' gets divided by A when referred to input

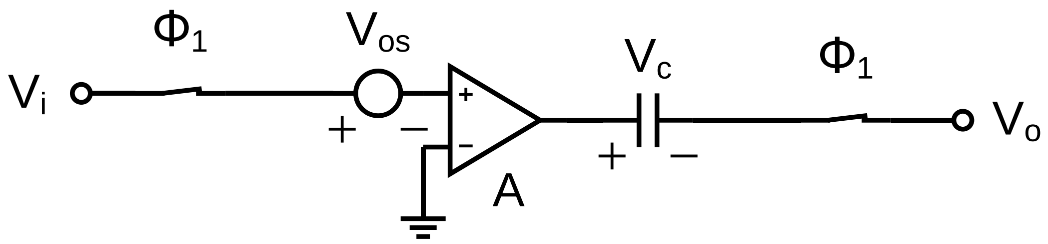


$$V_c = A(-V_{os}) = -AV_{os}$$

Ref: R. Poujois and J. Borel, “A low drift fully integrated MOSFET operational amplifier,” JSSC, vol. 13, pp. 499-503, issue 4, 1978.

Output Offset Cancellation

- Amplifying Phase – Φ_1
  - Cancellation is complete if A is constant (independent of Vo)
  - AC coupling at output attenuates signal gain



$$\begin{aligned} V_o &= A(V_i - V_{os}) + AV_{os} \\ &= AV_{in} \end{aligned}$$

$\Rightarrow$

Input-referred offset:

$V_{os,in} = 0$

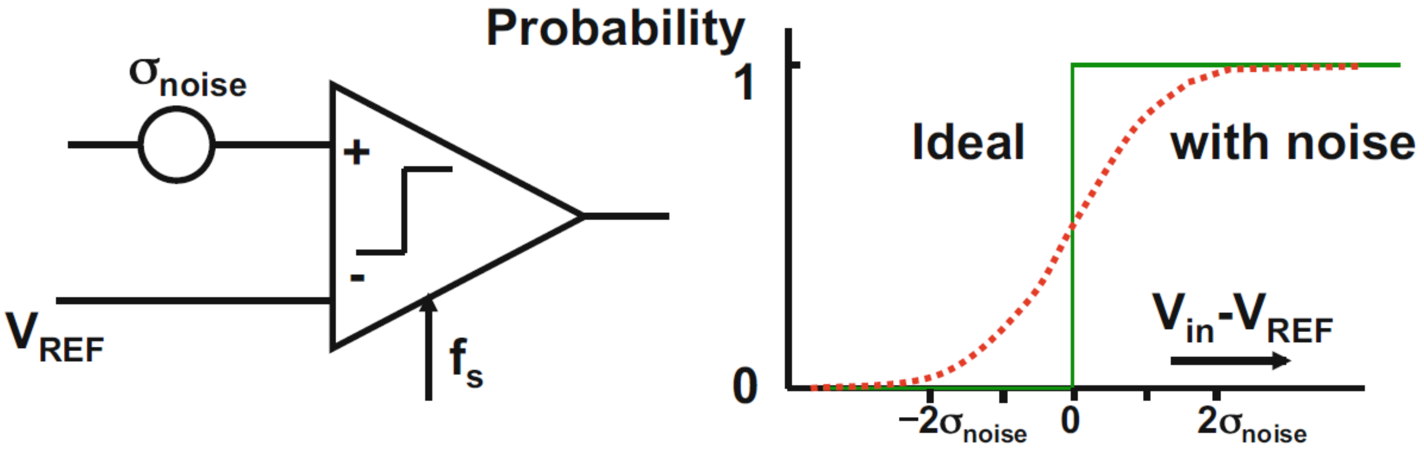
Comparator Noise

- The input referred noise voltage acts as time varying input offset
- If the thermal noise dominates:

$$v_{nout,rms}^2 = v_{nin}^2(f) \times A_v^2 \times B_N = \frac{4kT\gamma_{eff}}{g_m} \times A_v^2 \times B_N$$

$$v_{nin,rms} = \sqrt{\frac{4kT\gamma_{eff}}{g_m} \times B_N}$$

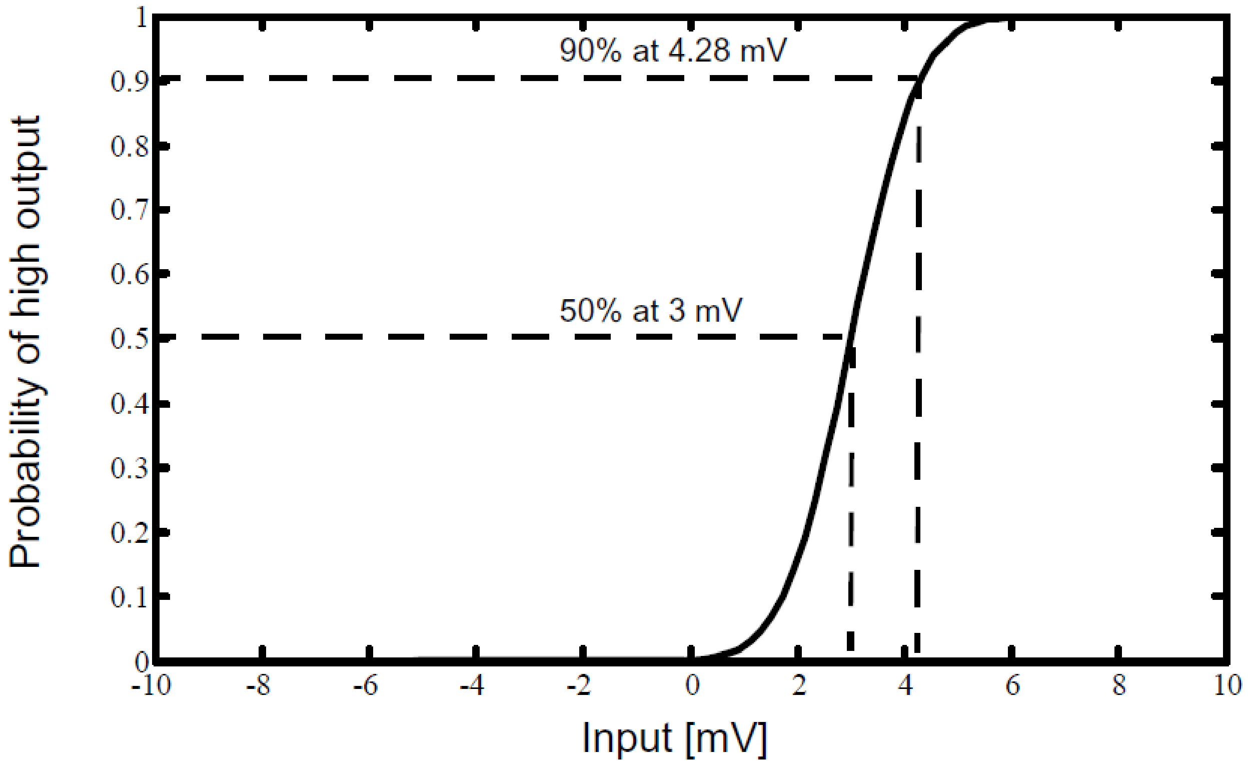
- Trade-off between noise, speed, and power consumption



[M. Pelgrom, 2017]

Quiz: Offset and Noise

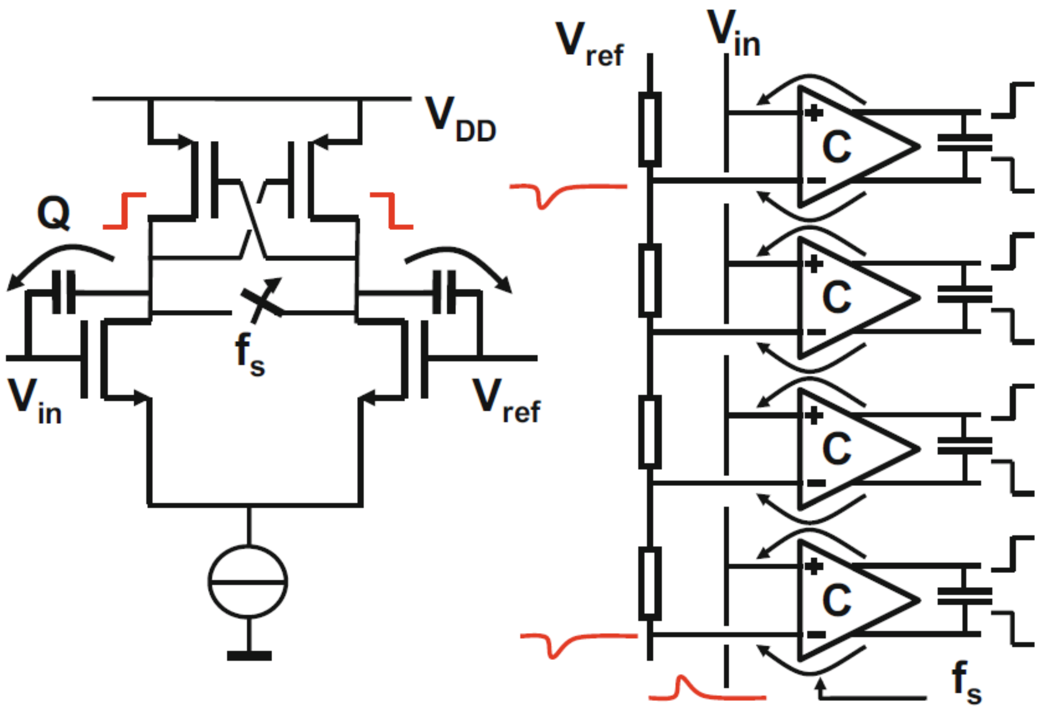
- Calculate the offset and noise from the shown measured comparator characteristics.



[Johns and Martin, 2012]

Kickback Noise

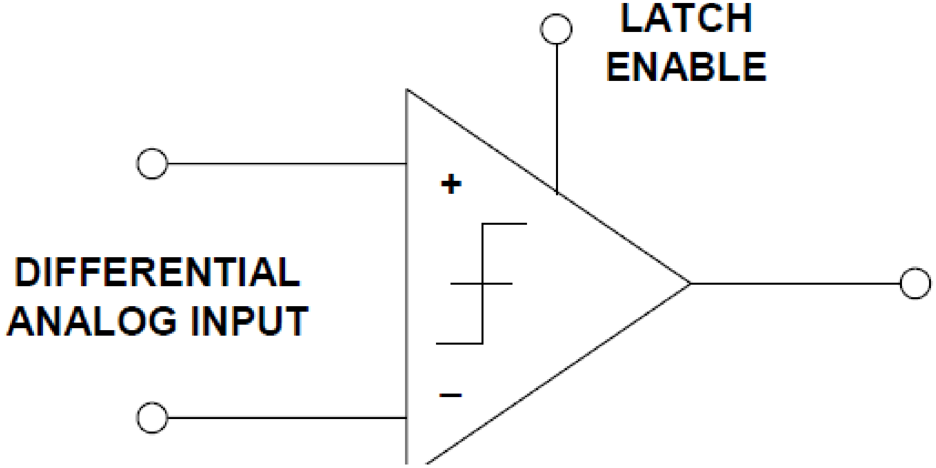
- The output has sharp voltage transitions
- C_{gd} will pass these fast edges to V_{in} and V_{ref} causing "kickback"
  - Reference voltage disturbance must settle before next sample
- Reducing C_{gd} by reducing sizing will make mismatch worse
- The output swing can be reduced by using limiting circuits

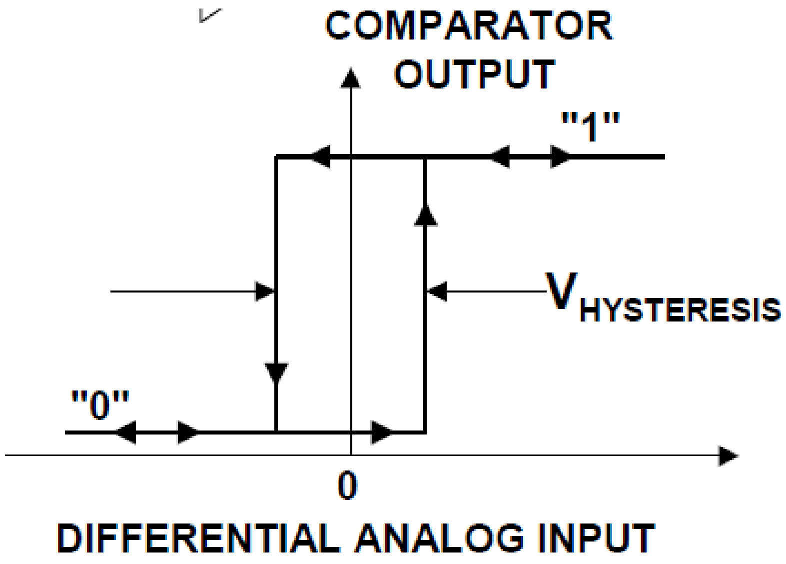


[M. Pelgrom, 2017]

Hysteresis

- Hysteresis: the comparator remembers its previous state.
- Either intentionally or as an unwanted consequence of the topology.
- Schmitt-trigger comparators use the hysteresis threshold to avoid unwanted transitions in case of noise signals
- The resolution of the comparator can be no less than the hysteresis
  - Large values of hysteresis are generally BAD for a high resolution comparator

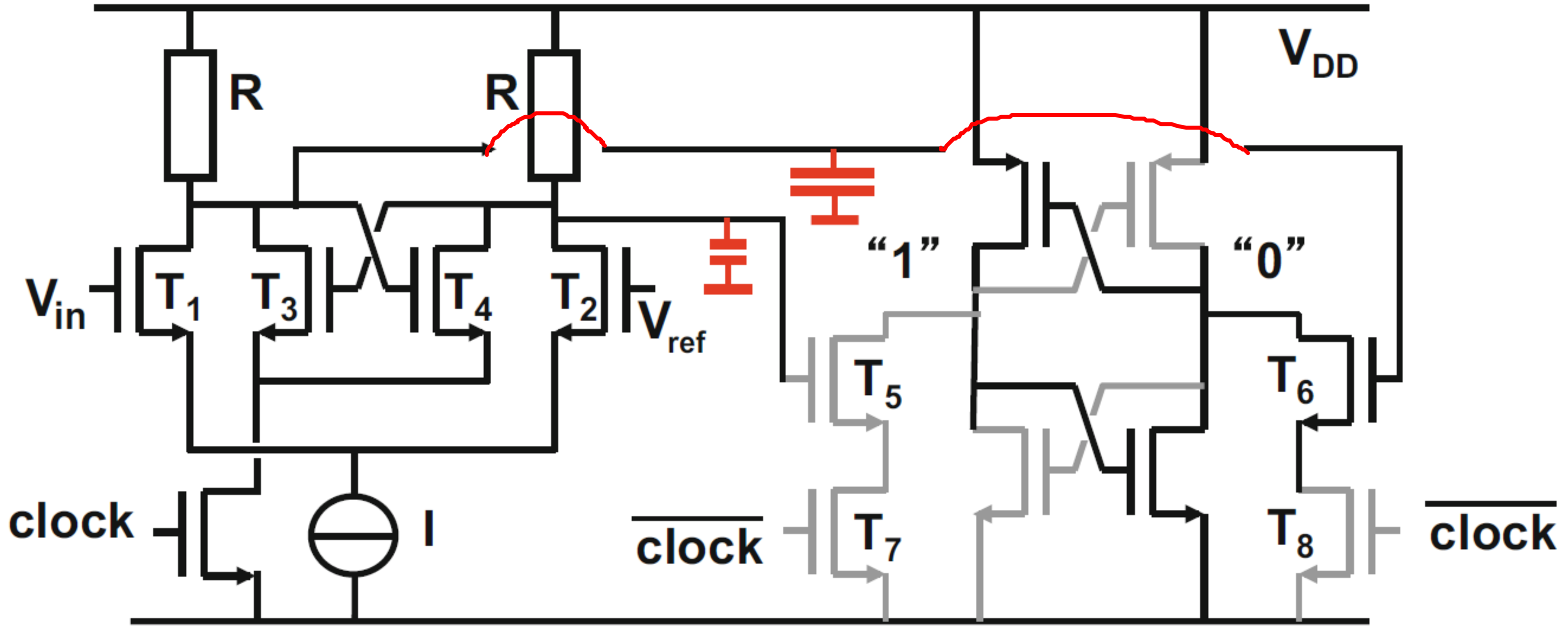




[W. Kester, ADI, 2005]

Hysteresis Example

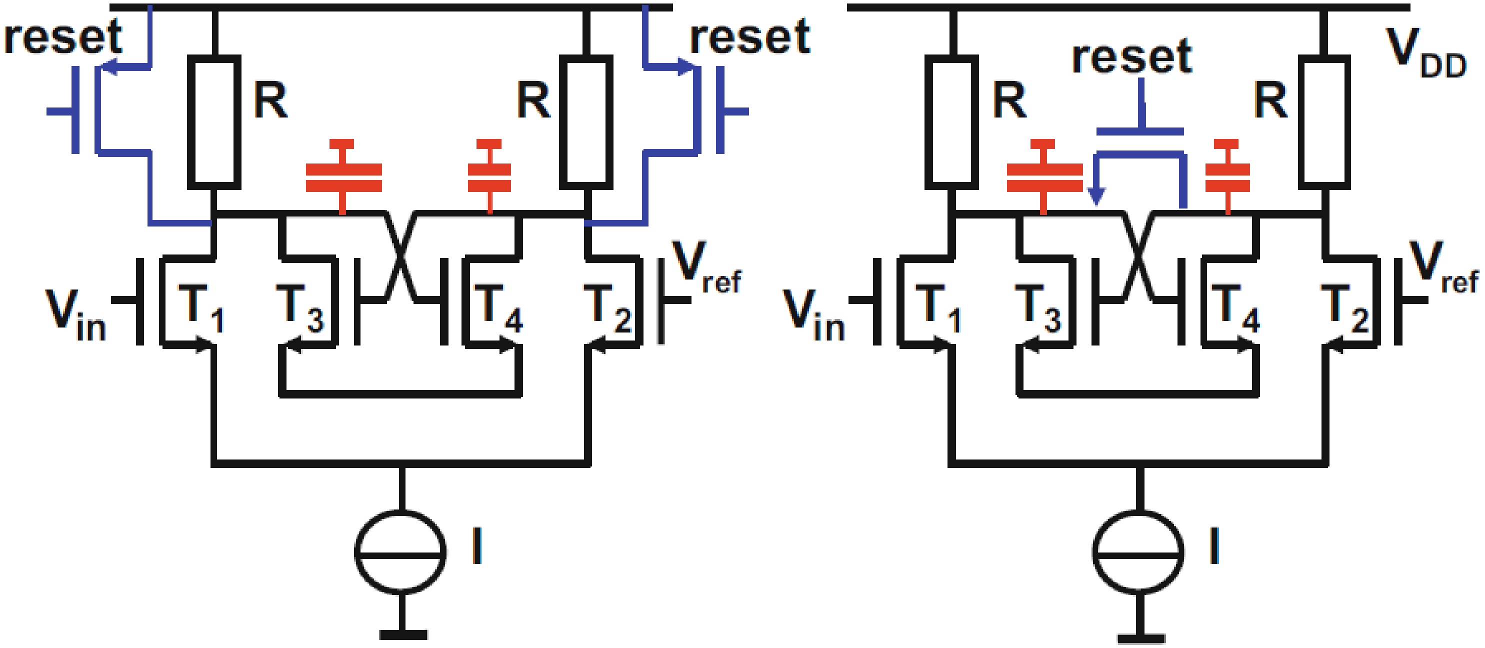
- A pre-latch stage that is connected to a second stage consisting of a full digital latch activated by the inverse clock
- For the example below: ON transistor (T6) has much higher capacitance than T5
- The unequal capacitive loading favors a similar signal in the first latch ➔ The consequence is a comparator with hysteresis.



[M. Pelgrom, 2017]

Removing Hysteresis

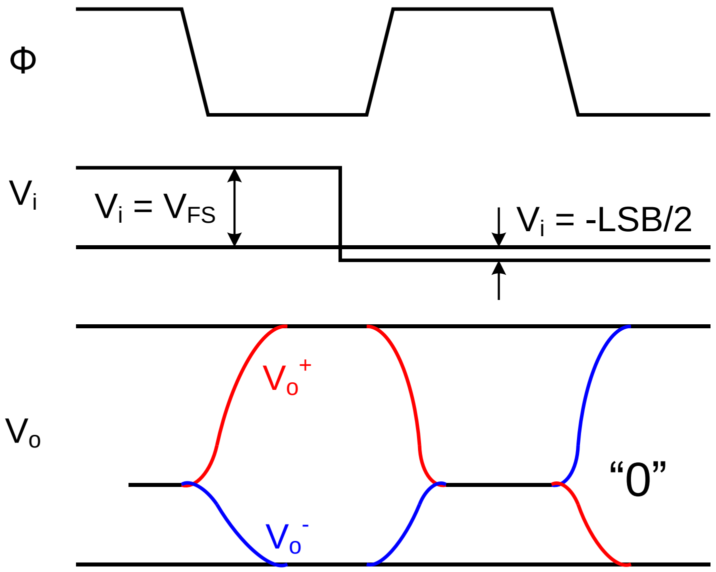
- The previous state can be removed by resetting the latch in the comparator



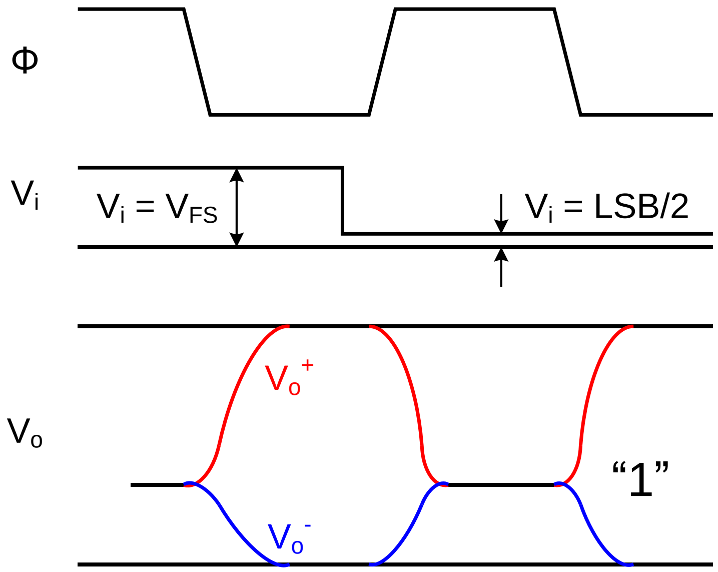
[M. Pelgrom, 2017]

Overdrive Recovery Test

- A small input (±0.5 LSB) is applied to the comparator input in a cycle right after a full-scale input is applied
  - The comparator should be able to resolve to the right output in either case → memoryless



Case I

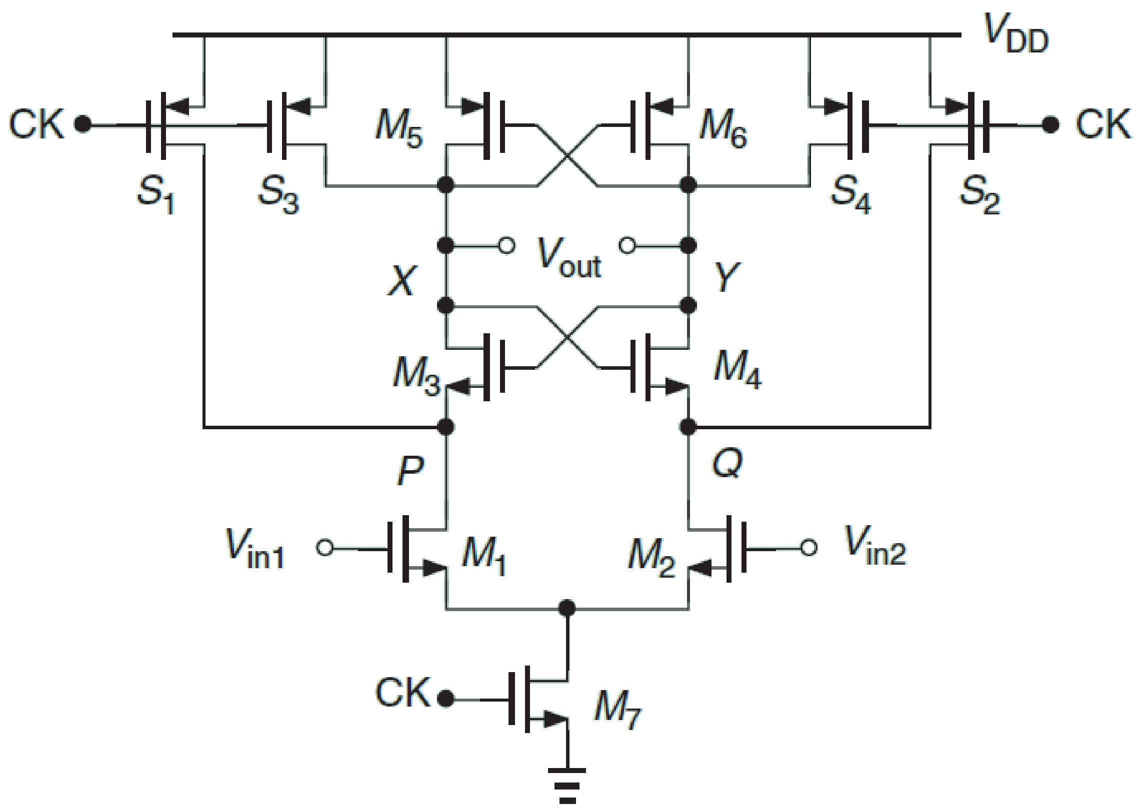


Case II

[Y. Chiu, EECT 7327, 2014]

The StrongArm Latch

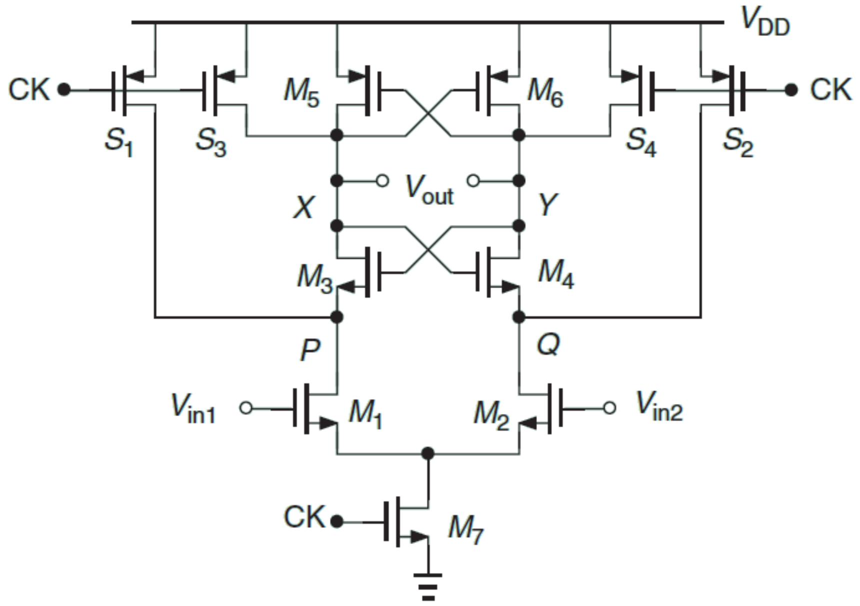
- A popular latch design used in the StrongARM MPU in the 1990s
  - The input offset is relatively large (pre-amp or calib required)
  - Many modified versions exist

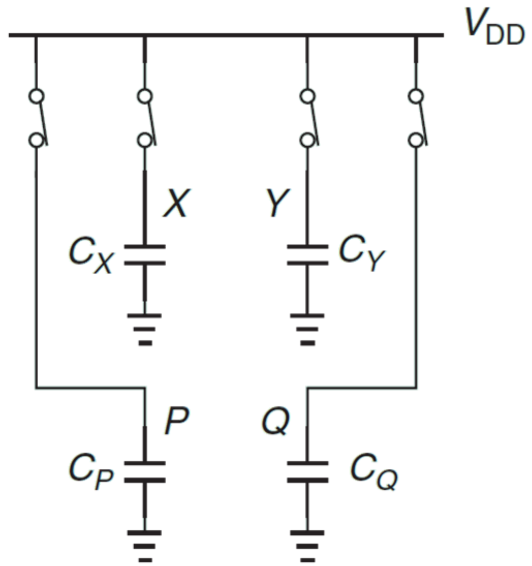


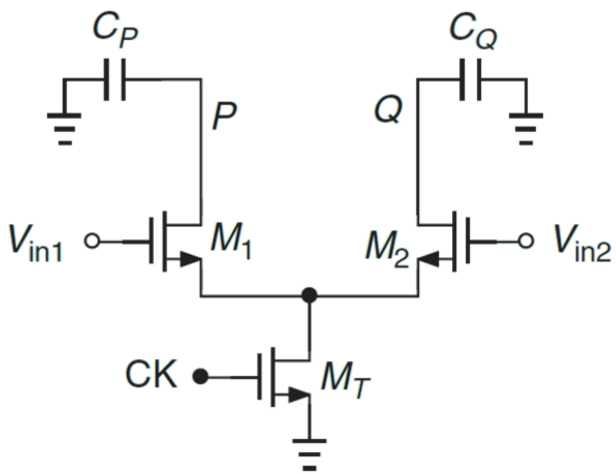
[B. Razavi, 2015]

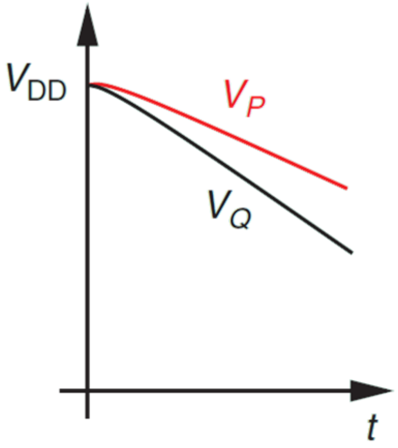
The StrongArm Latch

- Precharge phase: CK = 0
- S1-4
  - Reset the latch and remove previous states (hysteresis)
  - Keep M3-6 initially off reducing their offset contribution
- Amplification phase: CK = 1





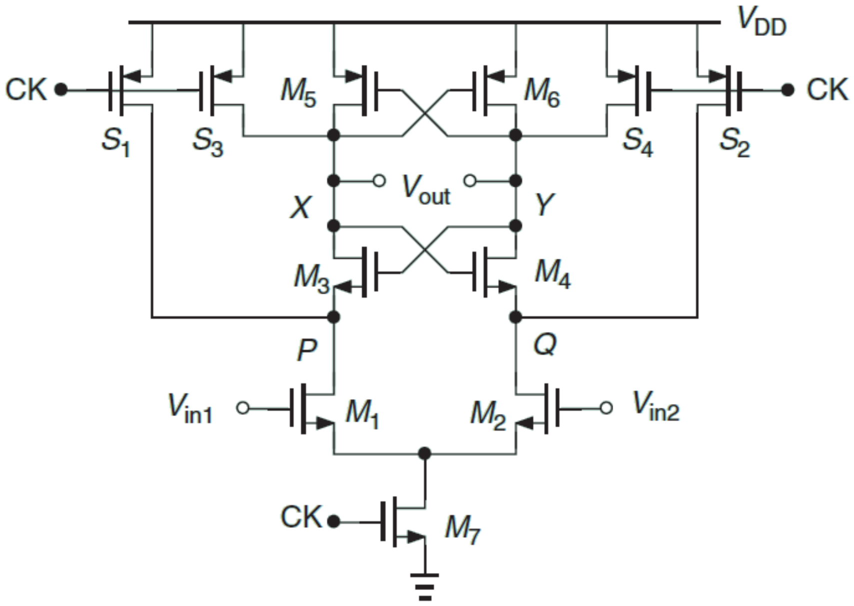


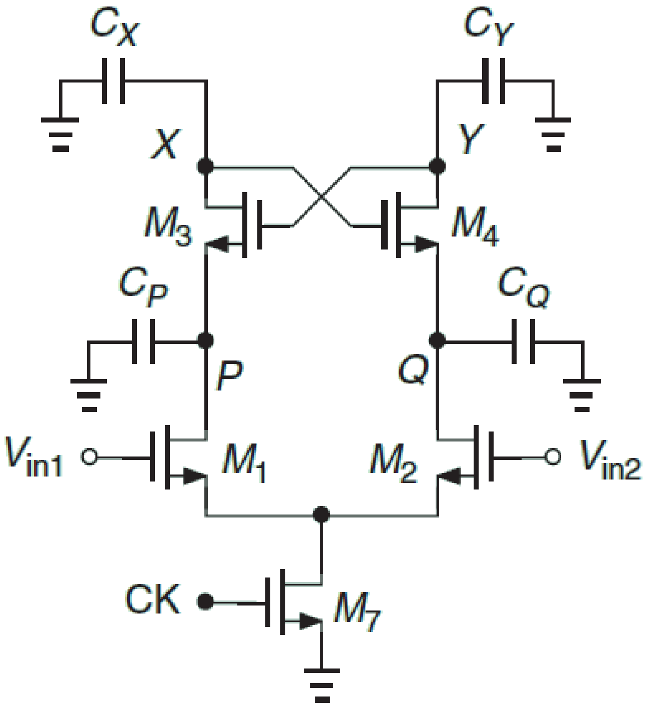


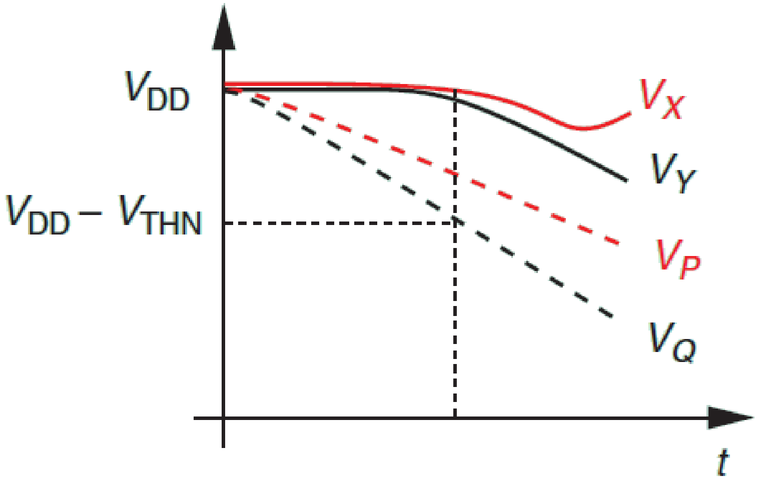
[B. Razavi, 2015]

The StrongArm Latch

- NMOS cross-coupled pair (M3,4) turns on
- M3,4 and M5,6 act as cross-coupled CMOS inverters
  - No static current flows



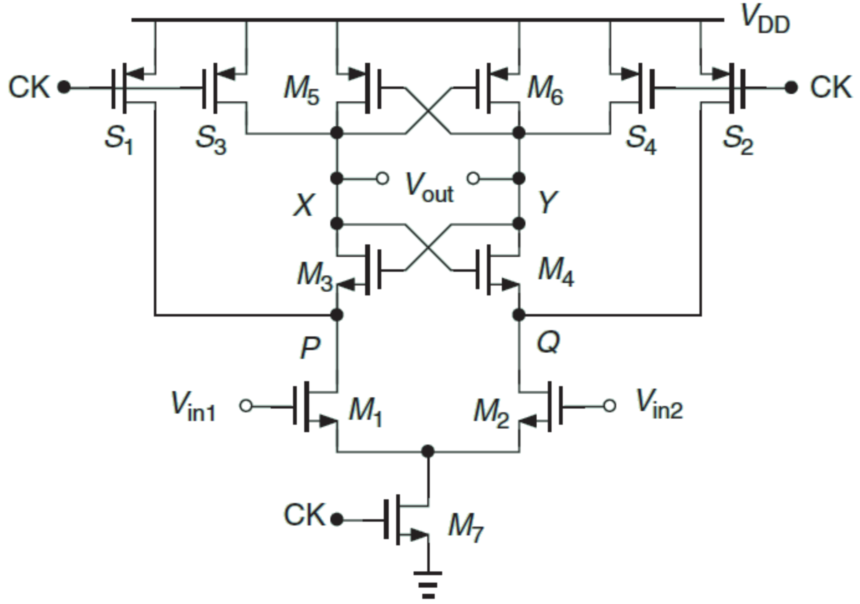


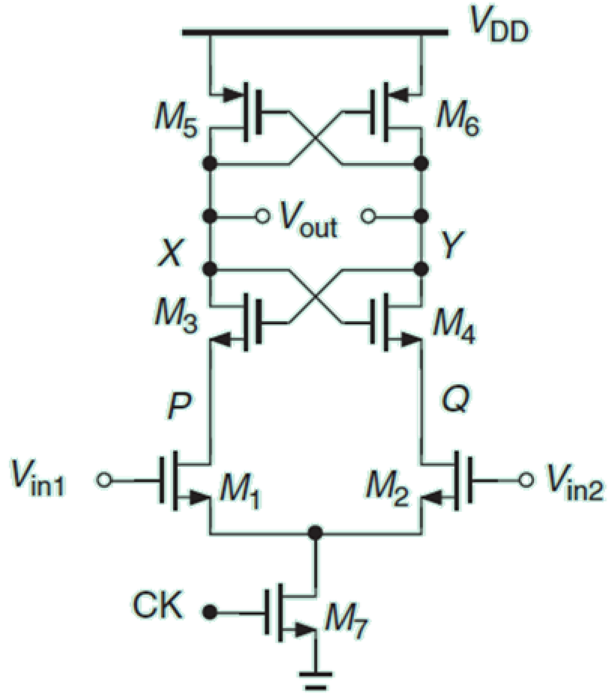


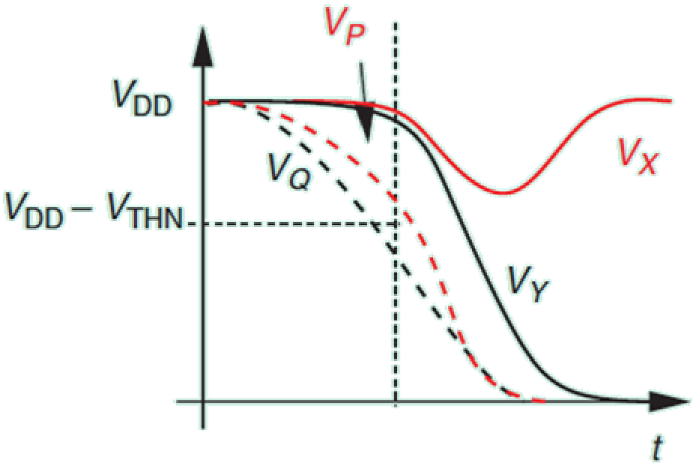
[B. Razavi, 2015]

The StrongArm Latch

- PMOS cross-coupled pair (M5,6) turns on
- Positive feedback brings one node to VDD and the other to GND



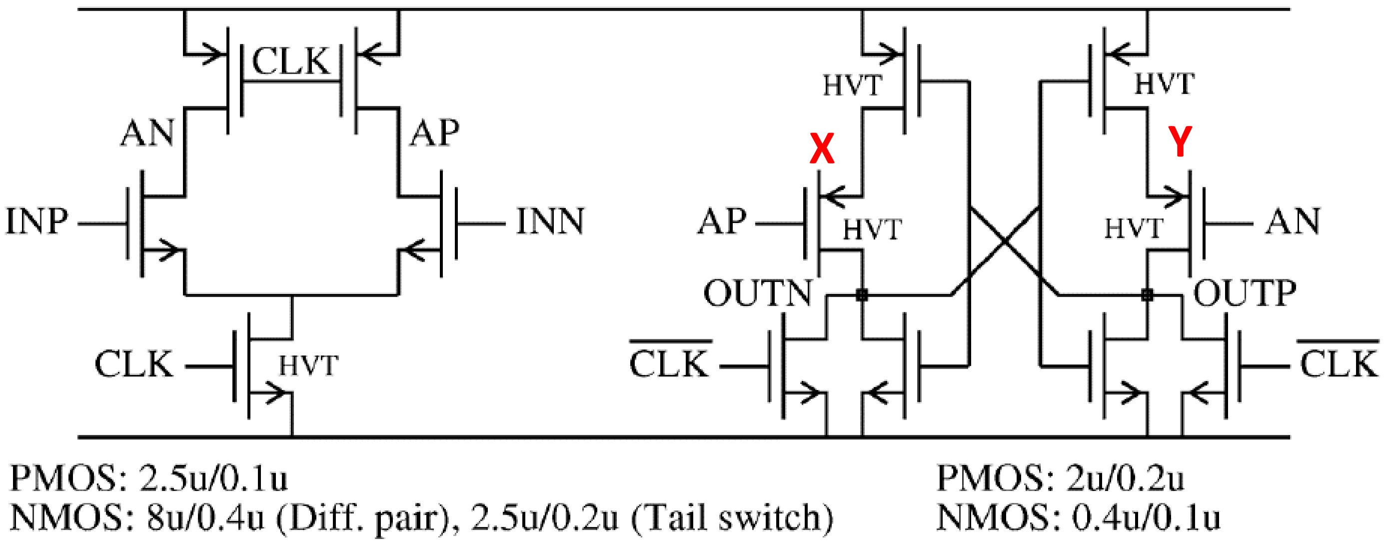


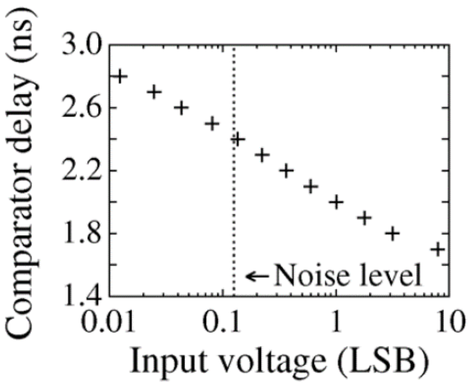


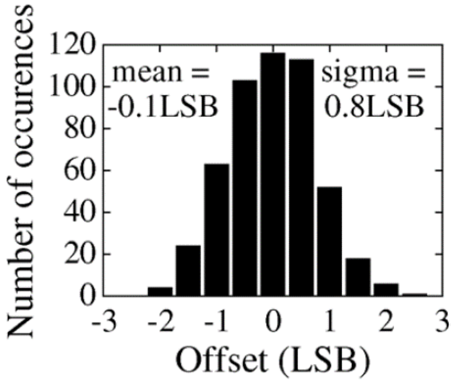
[B. Razavi, 2015]

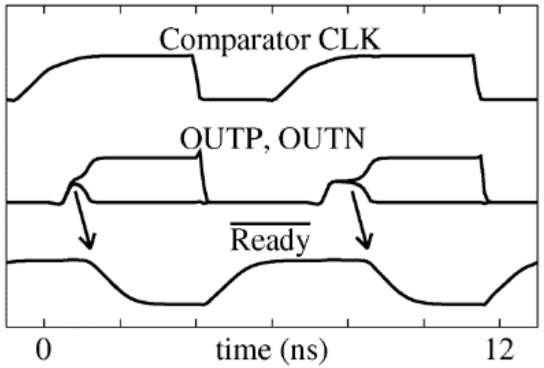
Fast Low-leakage Dynamic Comparator

- Comparator for low-power 8-bit SAR ADC (LSB = 3.2mV)









[P. Harpe et. al., JSSC, 2011, 46, 1585-1595]

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Thank you!