Analog Systems Design

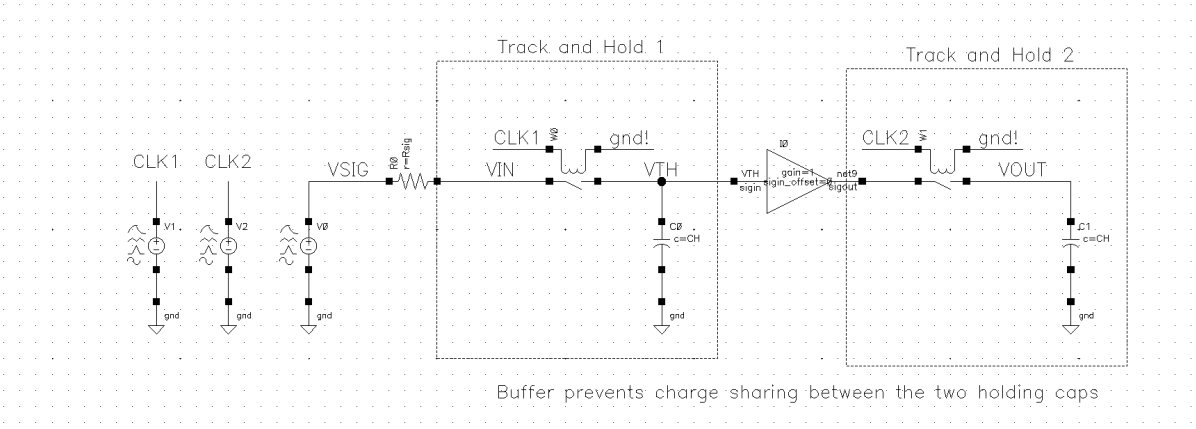
Lab No. 02 - Sampling and Quantization

1. Objective

- To be familiar with the operation of simple T&H and S&H circuits.
- To be able to do spectral analysis and calculate various performance metrics using FFT.
- To understand and apply the coherent sampling condition.
- To calculate the effect of FFT number of points on the noise floor.
- To be familiar with behavioral modeling and Verilog-A.
- To be familiar with the effect of quantization on SNR.

2. PART 1: Ideal Track & Hold and Sample & Hold

- Create a schematic consists of two T&H circuits separated by an ideal buffer (to prevent charge sharing between the two hold capacitors)



- Use ideal switch (R-open = 1 T @ V = 0.4 * V_{DD} & R-closed = 1 @ V = 0.6 * V_{DD})
- Use input signal with the following parameters

Type	Sinusoidal
Input frequency	F_{in}
Amplitude	$V_{pk} = V_{DD}/4$
DC offset	$V_{DC} = V_{DD}/2$

- Use two uncorrelated clocks

	Clock No. 1	Clock No. 2
Type	Pulse	Pulse
Zero Value	0	0
One Value	V_{DD}	V_{DD}
Period	$T_S = 1/f_s$	$T_S = 1/f_s$
Pulse Width	$T_{ON} = 0.4\ T_S$	$T_{ON} = 0.4\ T_S$
Delay	0	$0.5\ T_S$
Rise and Fall Time	T_{RF}	T_{RF}

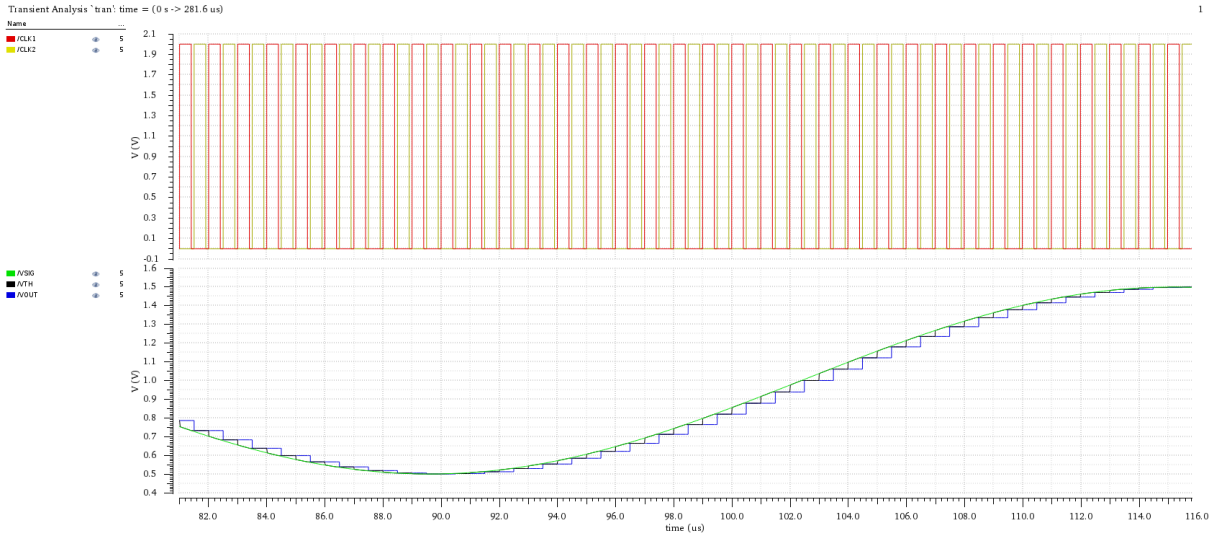
- Create an adexl view with added parameters
- N_{CYC} : the number of the input signal cycles
- NFFT : the number of the FFT points
- Ts is the sampling period = 1 / fs

- T_{STOP} is the simulating time and it is extended by a half period T_{DROPE} this half period is dropped before doing the FFT to avoid simulator artifact when simulator start and start-up artifacts in real circuits
- N_{CYC}, NFFT, F_{IN} are selected to satisfy the coherent sampling condition

- Full the parameters as following

Rsig	1K	Fin	NCYC/NFFT * $1/T_S$ = 19.53125 kHz
T_S	1 u → f_s = 1 MHz	V_{DD}	2
T_{ON}	0.4 T_S	V_{DC}	$V_{DD}/2$
T_{RF}	1 ns	V_{PK}	$V_{DD}/4$
NFFT	2**8 = 256	T_{DROP}	0.5 * (1/Fin) = 25.6 u
N_{CYC}	5	T_{STOP}	(N_{CYC} * 1/Fin) + T_{DROP} = 281.6 u

- Transient Analysis



- Use spectrum assistant to plot FFT (see Appendix)
- What is the power of the peak signal (in dB)? Why?

  -6.02 dB, because the input signal is 0.5 V_{FS} = $20\log 0.5 = -6.02$ dB
- How many bins are occupied by the test signal?

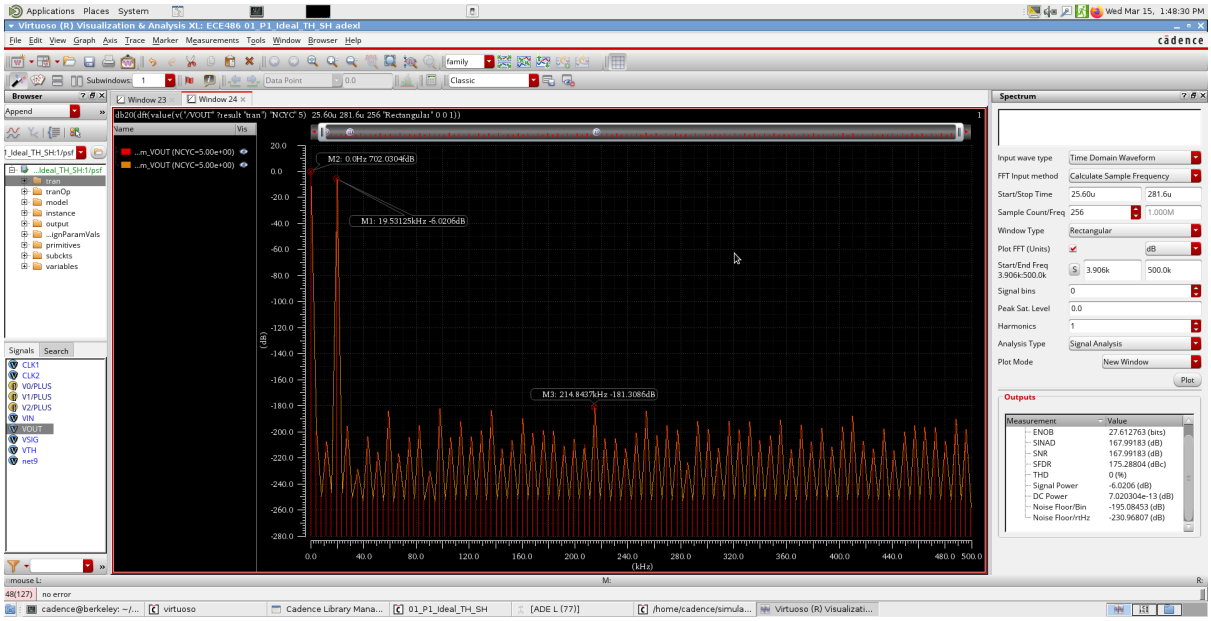
  One, because of the system is linear, coherent testing and the input is single frequency signal
- What is the noise floor (in dBFS)?

  -195.08453 dB
- What is the relation between the SNR, NFFT, Signal Power, and Noise Floor?

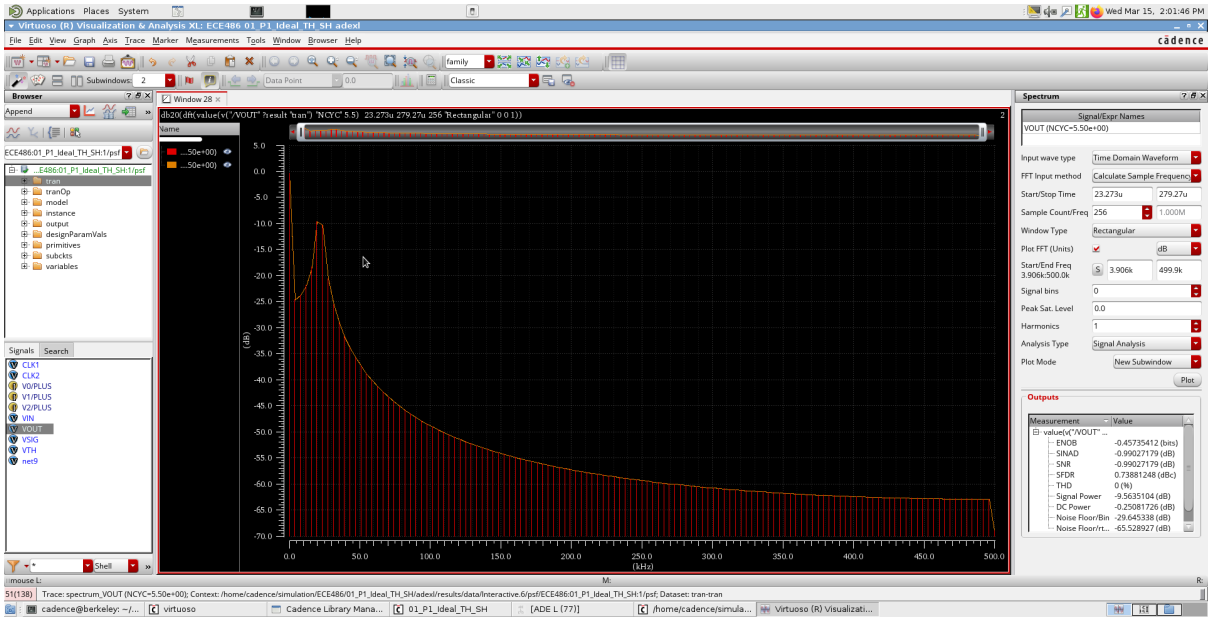
$$FFT_{\text{Noise Floor}} = 10\log\left(\frac{V_{LSB}^2}{12}\right) - 10\log\left(\frac{NFFT}{2}\right) = 10\log(\text{Sig Power}) - SNR - 10\log\left(\frac{NFFT}{2}\right)$$

- If the sampling is ideal, what is the source of error that causes the noise floor?

  Due to Cadence numerical errors

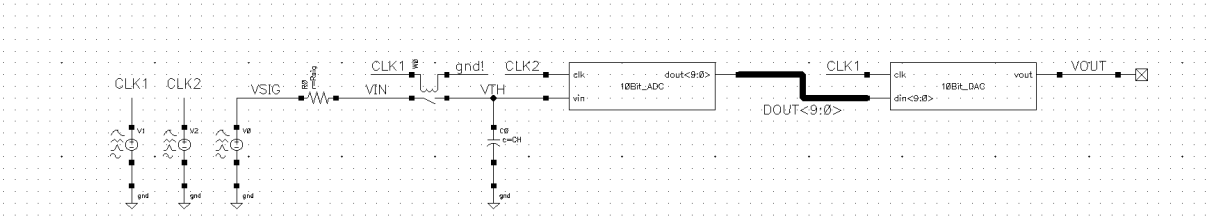


- Change NCYC to 5.5 and re-simulate. Note that the start and stop time in the DFT will change from the previous case. Plot the new FFT. Observe the spectral leakage.

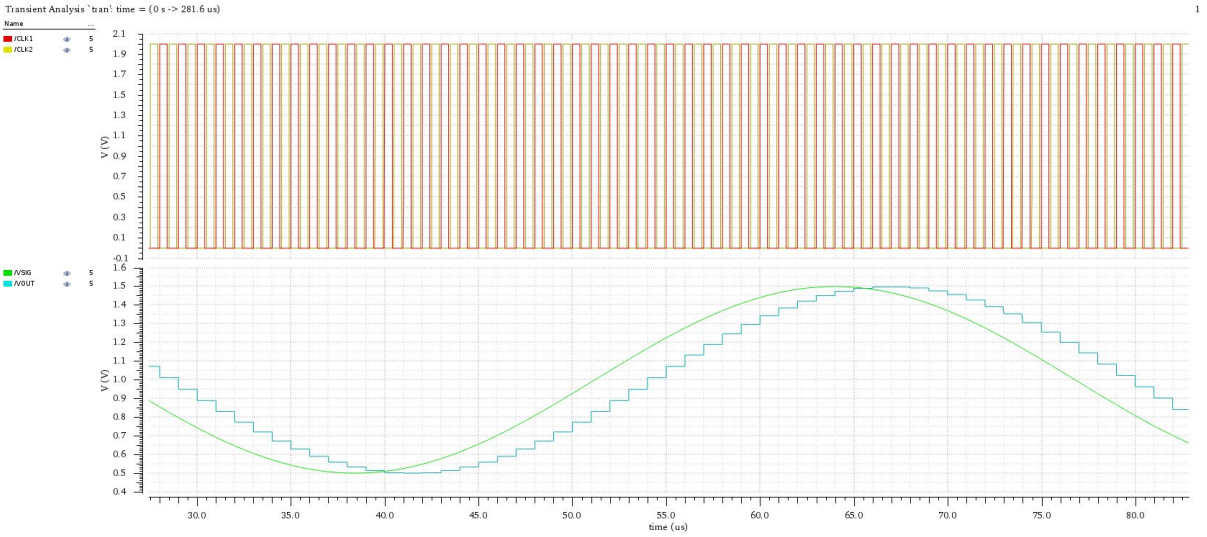


The leakage is due to abrupt transition because NCYC doesn't equal an integer number so Coherent condition is not satisfied leading to Spectral Leakage.

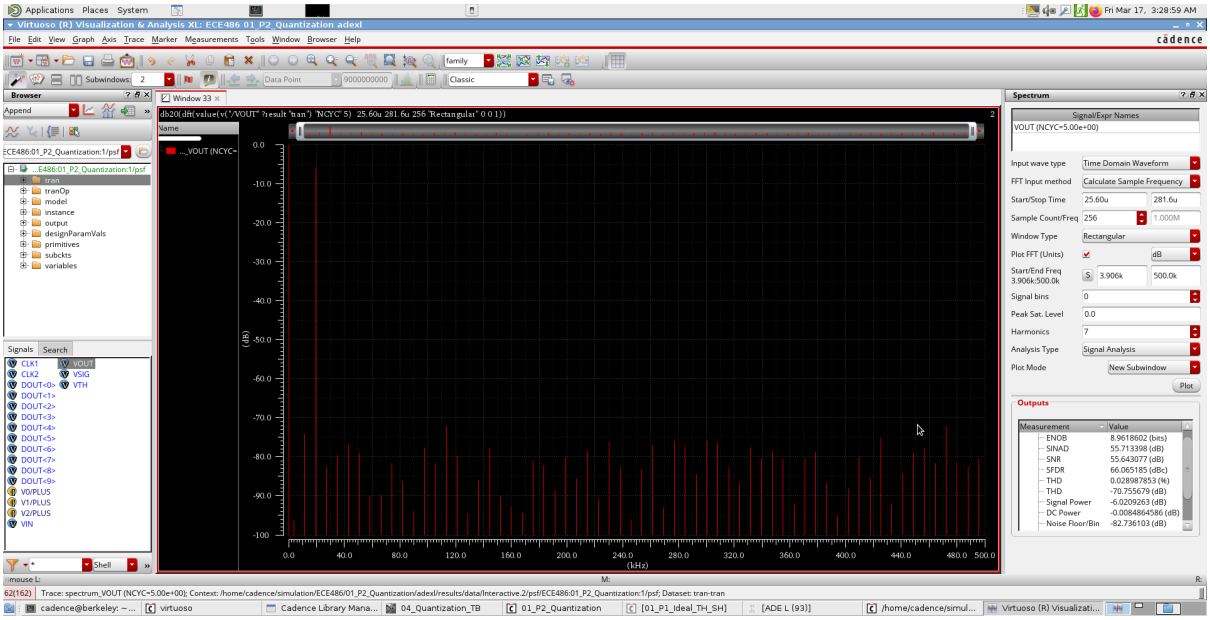
3. PART 2: Quantization
   - Use Modelwriter to create a veriloga model for a 10-bit ADC. Create a symbol for the generated view.
   - Similarly, use Modelwriter to create a veriloga model for a 10-bit DAC. Create a symbol for the generated view.
   - Create a new testbench



   - Plot the transient waveforms and study the timing relations between different signals.

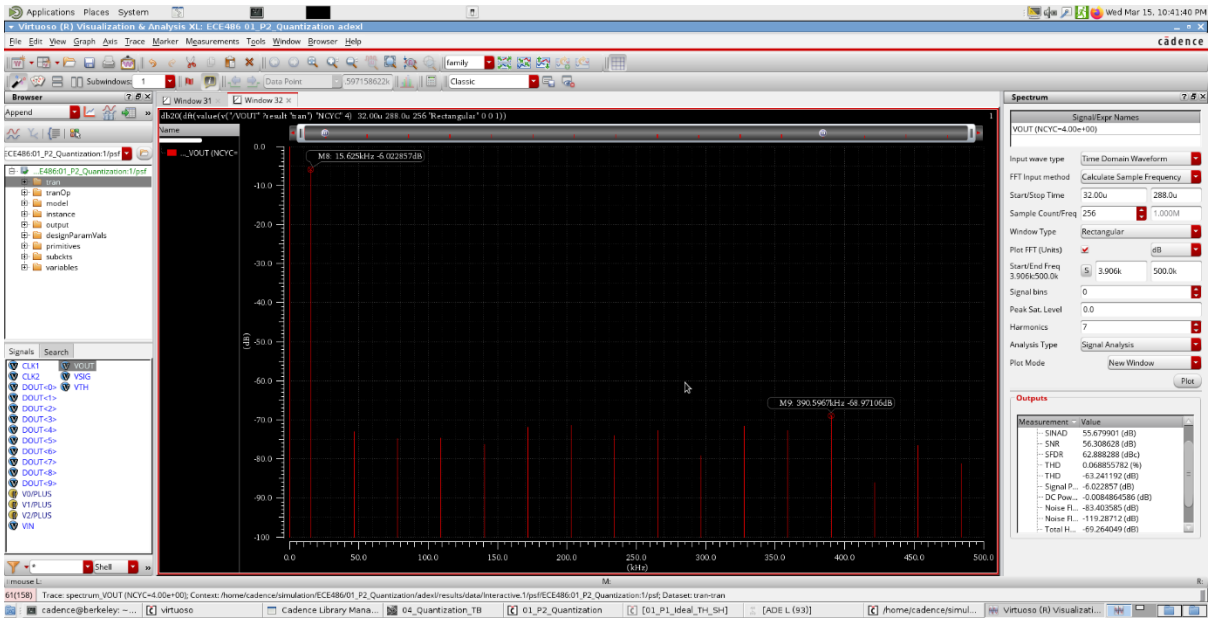


   - Analyze the DAC output using the spectrum assistant. The result will be as shown below (zoom in y-axis from 0 to -100dB). Compare the SNR, ENOB, Signal Power, DC Power, and Noise Floor with the expected theoretical values.



	Theoretical	Analytical
SNR = 6.02 N + 1.76 dB	60.2 + 1.76 = 61.96 dB	55.64 dB
ENOB = SINAD − 1.76/6.02	8.9618	8.9618
Sig Power = $10 \log V_{DD}^2/16$	-6.02	-6.02
DC Power = $10 \log V_{DD}^2/4$	0	0.00848
Noise Floor = $10 \log V_{LSB}^2/12 - 10 \log M/2$	-86.049	-82.736

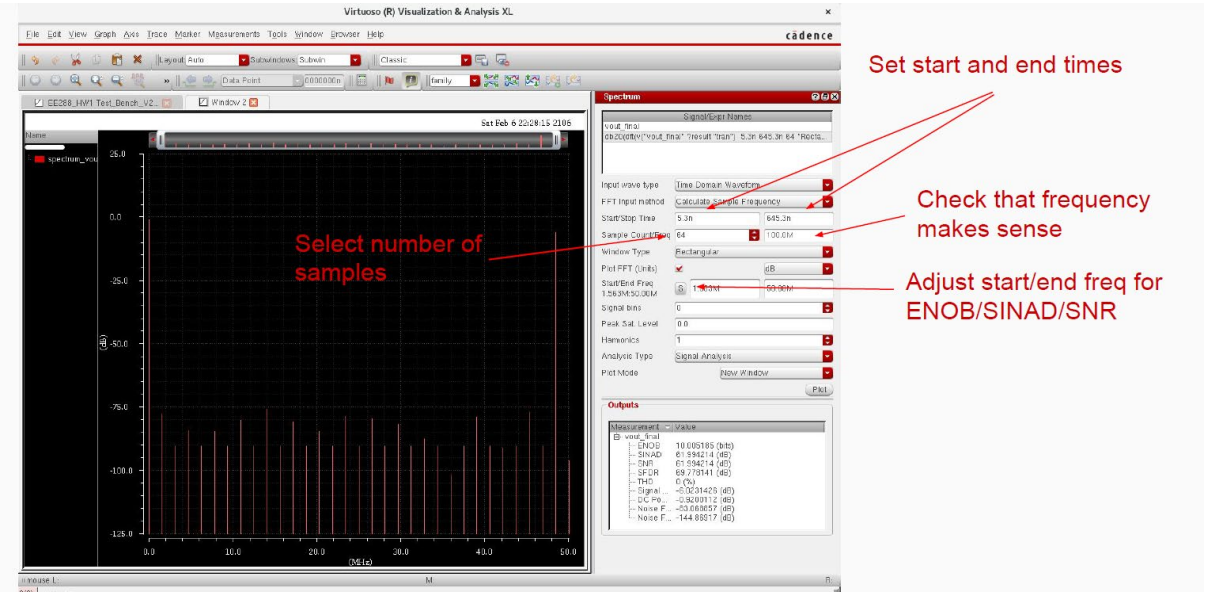
- Record the value of the SFDR.
  66.065 dBc
- Change NCYC to 4 and re-simulate (now NFFT/NCYC = integer). Plot the new FFT (zoom in y-axis from 0 to -100dB). Note that the start and stop time in the DFT will change from the previous case. Compare the new SFDR with the previous one. Comment.



- SFDR will change to 62.88 dBc

SFDR of the second case is smaller because there's correlation between the sampling frequency and the input frequency so the Harmonics power will not spread which means there will be Higher harmonics Since, SFDR = Signal power − highest noise power so SFDR will decrease or in simpler words the sampling frequency and the test tone are corelated which makes the quantization error periodic causing more spurs in the frequency domain which decrease the SFDR while in the first case they aren't corelated which makes the error random and spreads it in frequency domain making it behave more like white noise.

- Appendix
- Set parameters for spectrum



- Adding continuous line over spectral lines