Analog Integrated Systems Design

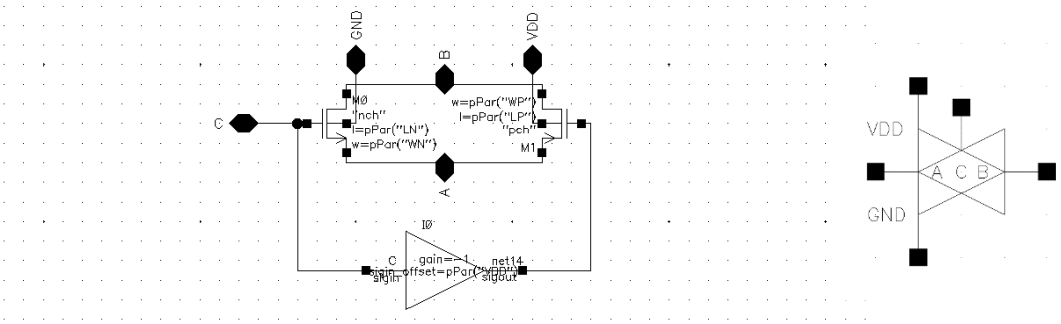
LAB No.4 - Sample and Hold circuits

- Objective

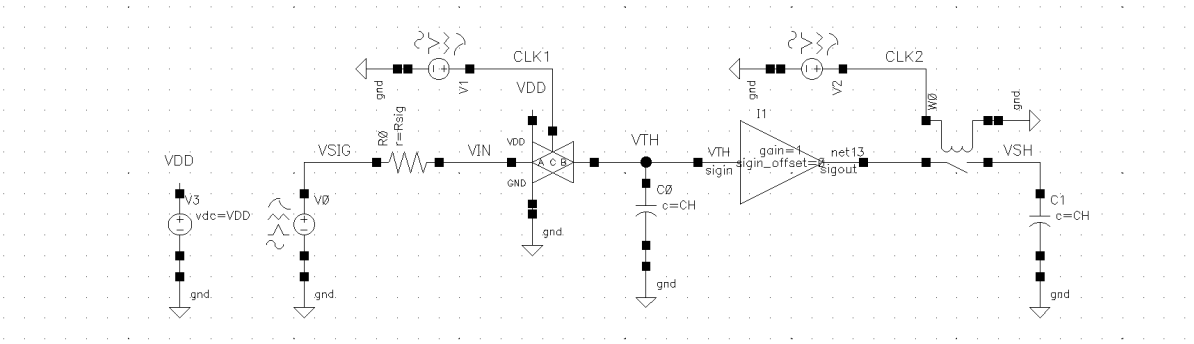
  - To be familiar with the artifacts of S&H circuits.
  - To appreciate the importance of bottom-plate sampling.
  - To appreciate the importance of fully differential operation.

- **S/H Artifacts**

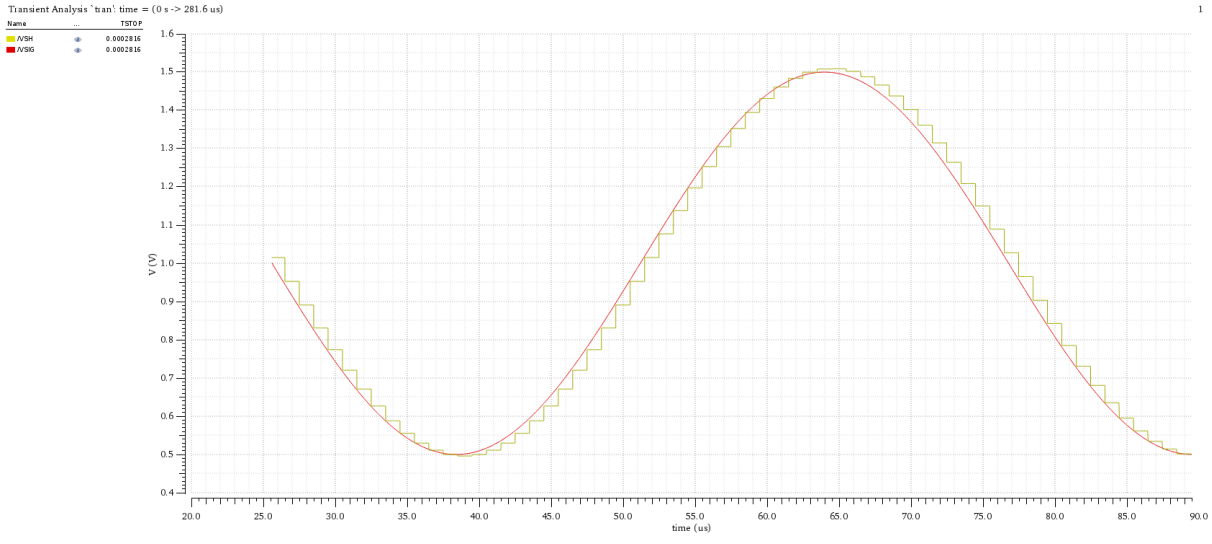
01 | Create Transmission Gate Cell



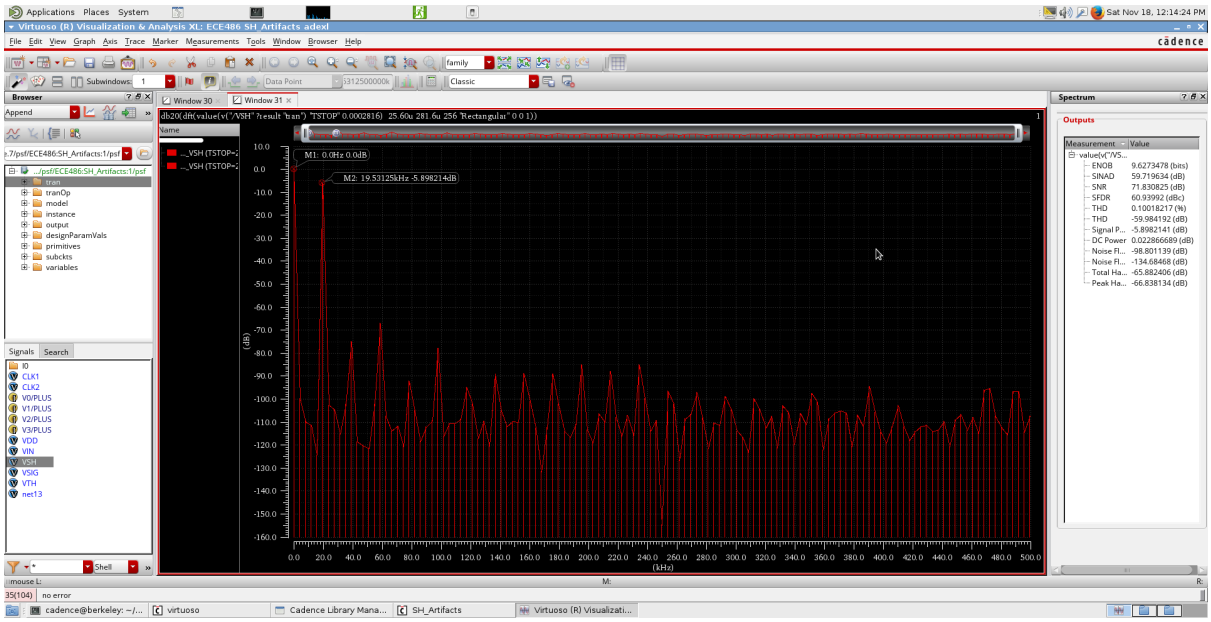
02 | The schematic is similar to ideal S/H, but the first ideal switch is replaced by a transmission gate.



03 | Run transient analysis. Plot VSIG and VTH overlaid. Zoom in to observe the S&H artifacts



04 | Use the Spectrum Assistant to plot FFT for VSH. Compare the results below with Lab 02 Part 1 results in a table.



Test	Output	Nominal	Spec	Weight	Pass/Fail
Training:02_SAH_TB:1	DC power	22.87m			
Training:02_SAH_TB:1	ENOB	9.627			
Training:02_SAH_TB:1	SFDR	60.94			
Training:02_SAH_TB:1	Sig power	-5.898			
Training:02_SAH_TB:1	SINAD	59.72			
Training:02_SAH_TB:1	SNB	-99.12			
Training:02_SAH_TB:1	SNR	72.15			
Training:02_SAH_TB:1	THDdB	-59.96			

(a)

Test	Output	Nominal	Spec	Weight	Pass/Fail
Training:02_SAH_TB:1	DC power	702f			
Training:02_SAH_TB:1	ENOB	27.61			
Training:02_SAH_TB:1	SFDR	175.3			
Training:02_SAH_TB:1	Sig power	-6.021			
Training:02_SAH_TB:1	SINAD	168			
Training:02_SAH_TB:1	SNB	-197			
Training:02_SAH_TB:1	SNR	170			
Training:02_SAH_TB:1	THDdB	-172.1			

(b)

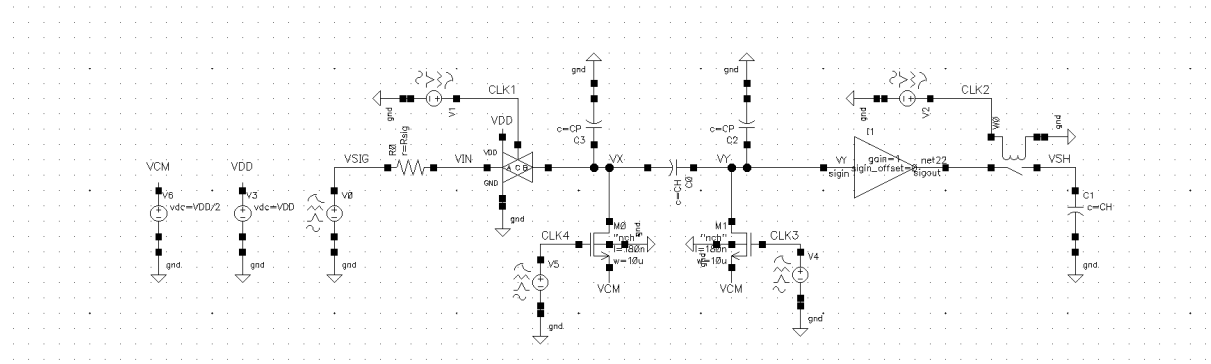
(a) Spectrum parameters for VSH with TG (b) Spectrum parameters for VSH with ideal switch

05 | Comment on the differences.

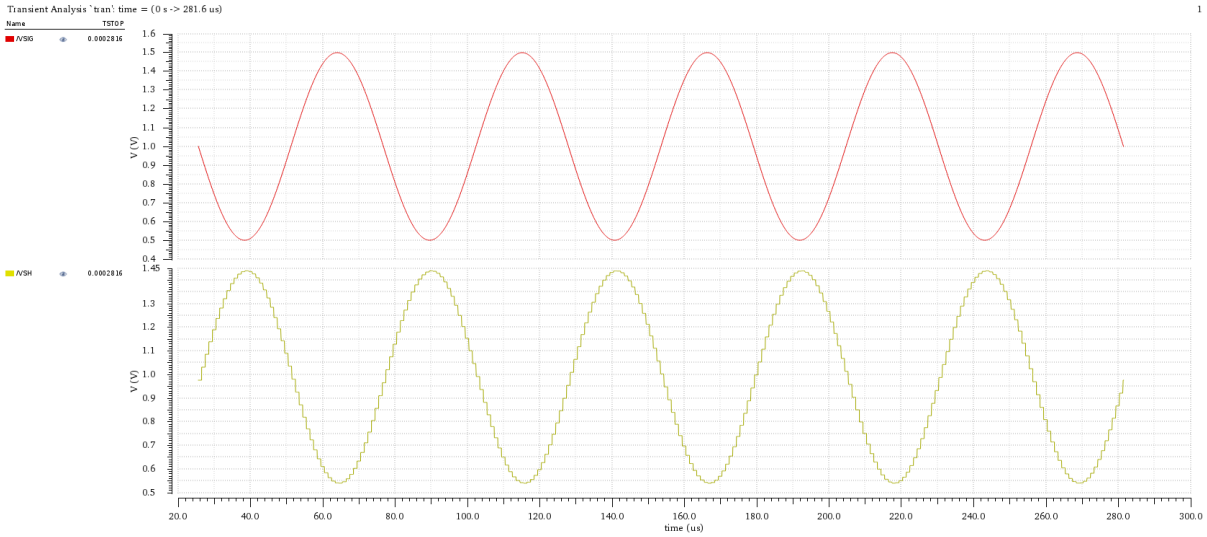
There's a huge difference between the results in Lab 2 (Ideal) and Lab 4 all of that because we introduced Transmission gate Switch which is made of transistors which are nonlinear elements which introduced non-linearity to the system introducing harmonics and noise leading to increase in the total harmonic distortion and decreasing ENOB ,SINAD , SNR & SFDR.

- **Bottom plate Sampling**

01 | Construct the circuit shown below. Bottom plate sampling is used. The capacitors "CP" model the parasitic capacitors at VX and VY.



02 | Run transient analysis. Observe the timing relations between different signals.

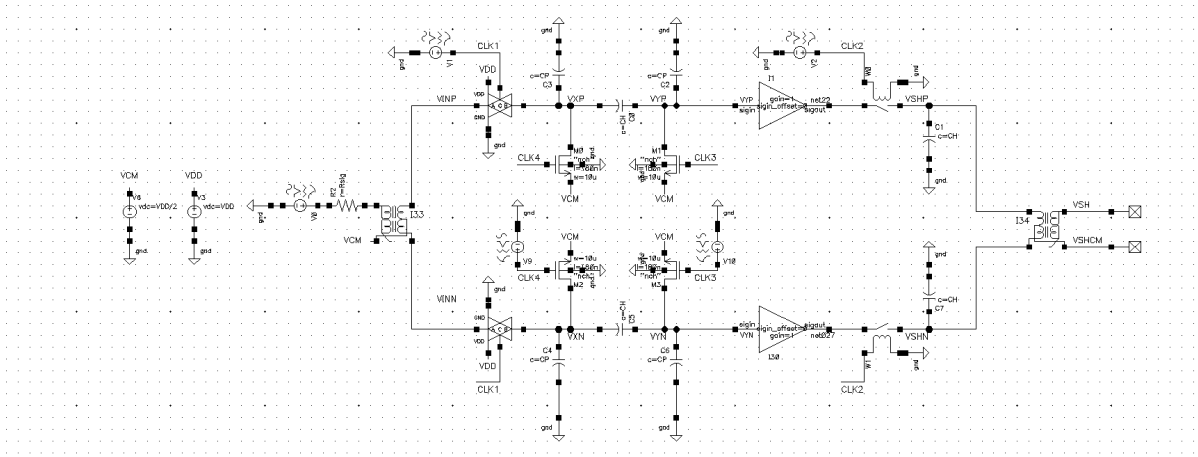


03 | Use the Spectrum Assistant to plot FFT. Compare the results below with Part 1 results in a table. Comment on the differences.

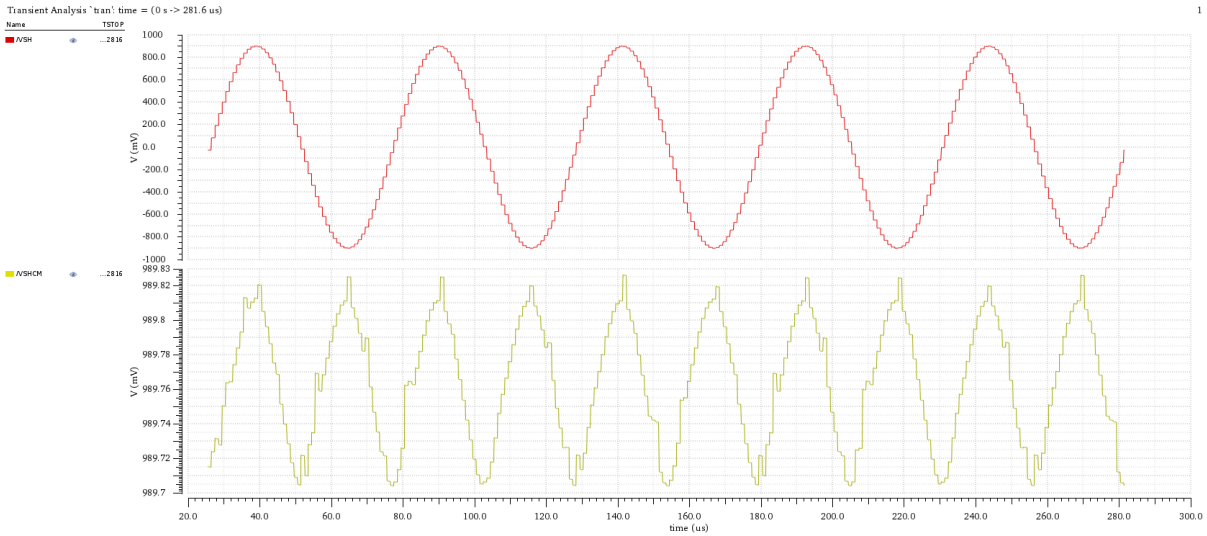
There's an improvement in the system ENOB improved significantly SINAD,SNR and SFDR increased and THD decreased that's because bottom-plate sampling decreases the non-linearity in the system by making the charge injection less independent on input signal.

- **FD Operation**

01 | Modify the schematic to be fully differential as shown below

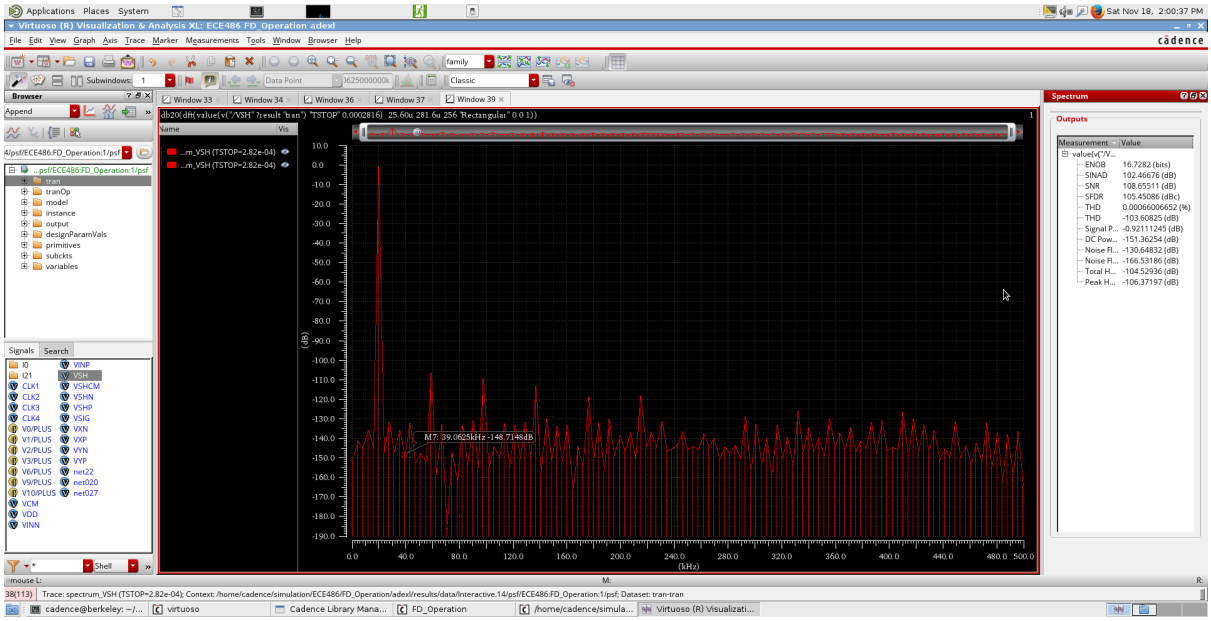


02 | Plot the differential output and the common mode output vs time. Comment on the peak-to-peak differential output. Comment on the common output waveform.

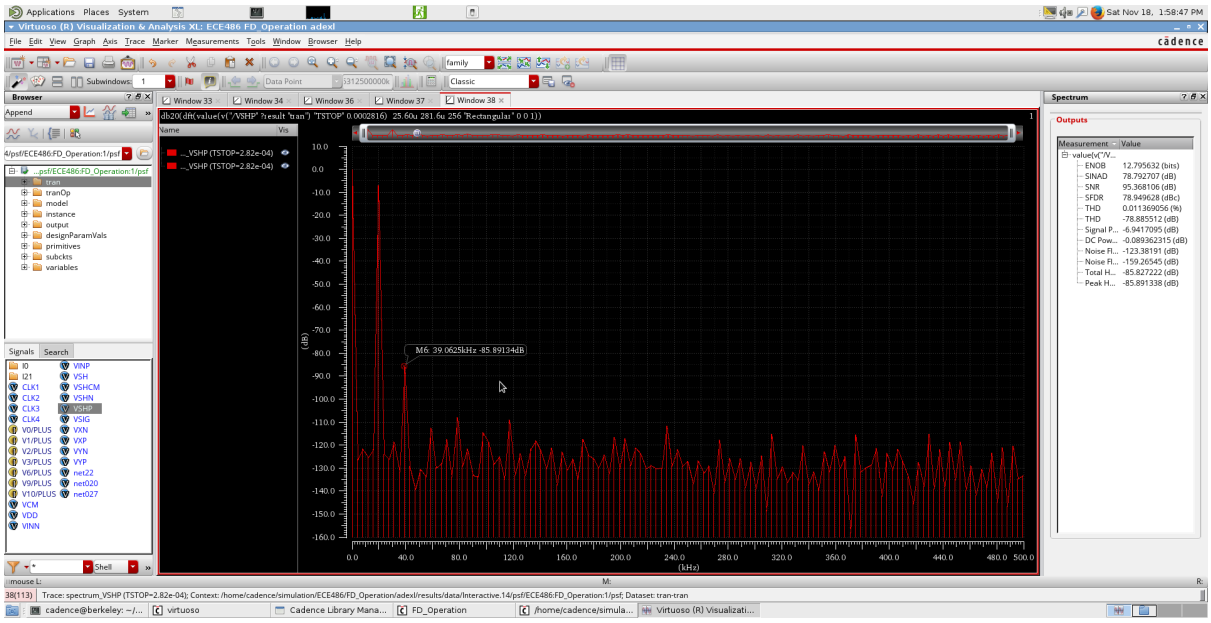


The peak-to-peak differential output is slightly attenuated that's due to the presence of parasitic caps which attenuates the signal, the common mode is composed of the rejected DC component and Even order harmonics and the dominant second order that's why the common mode signal has double the frequency of the differential mode signal and on DC level.

03 | Use the Spectrum Assistant to plot FFT of the positive half output VSHP and the differential output VSH. Compare the 2nd harmonic power in VSHP and VSH spectrum. Compare the results below for VSHP and VSH



VSH



VSHP

There's an improvement in the system using differential operation because the differential operation rejects the common mode noise and even order harmonics which improves ENOB ,SINAD,SNR and SFDR and THD and that's what we see from the results.