Analog Integrated Systems Design

Lab 02: Sampling and Quantization - Cadence

Mar. ۲۸, 2022

1. Ideal Track & Hold and Sample & Hold

1. Create a new cell. Construct the circuit shown below. The schematic consists of two T&H circuits separated by an ideal buffer.

Note that if we don't use a buffer, charge sharing will occur between the two hold capacitors.

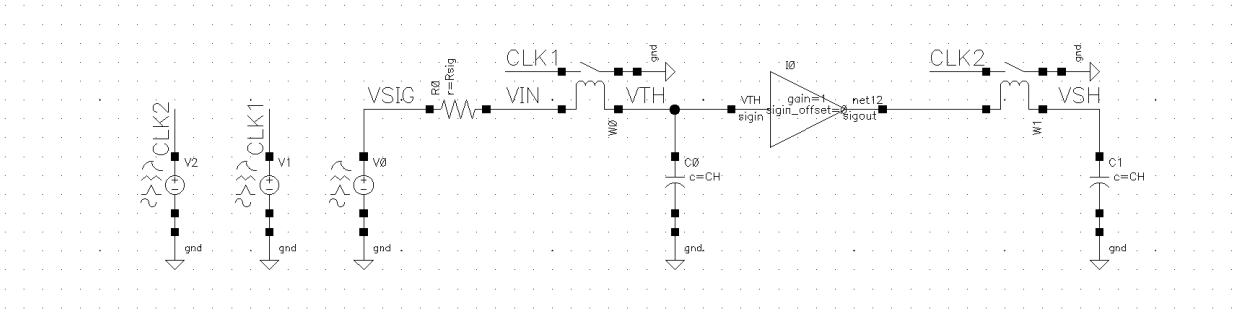


Figure 1.1: Ideal sample and hold circuit

8. Run transient analysis. Plot VSIG, VTH, and VSH overlaid. Zoom in to observe the difference between T&H (VTH) and S&H (VSH).

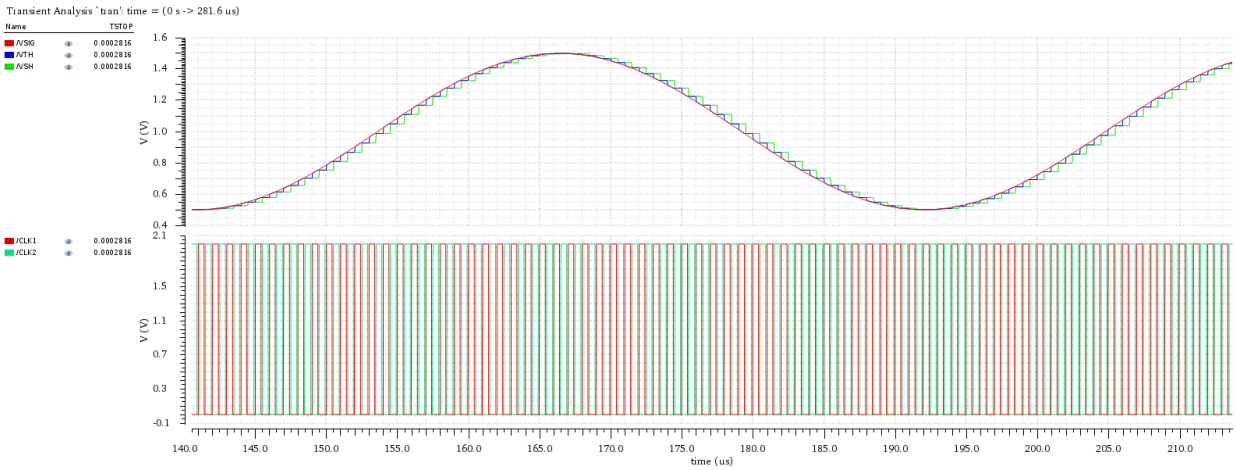


Figure 1.2: VSIG Vs VTH Vs VSH

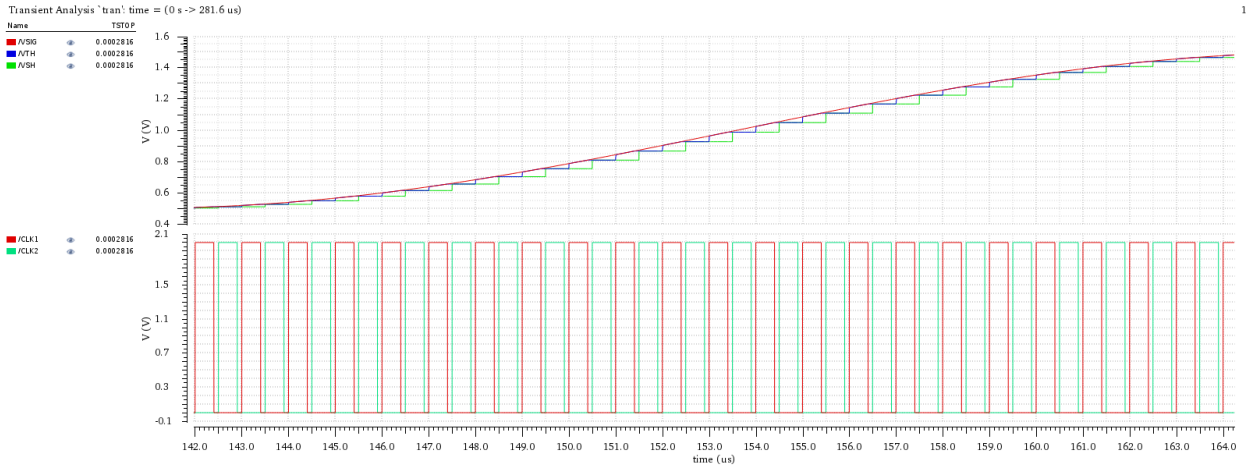


Figure 1.2: VSIG Vs VTH Vs VSH

9. Use the Spectrum Assistant to plot FFT. Familiarize yourself with the different options in the Spectrum Assistant window.

   a. What is the power of the peak signal (in dB)? Why?

   b. How many bins are occupied by the test signal?

   c. What is the noise floor (in dBFS)?

   d. What is the relation between the SNR, NFFT, Signal Power, and Noise Floor?

   e. If the sampling is ideal, what is the source of error that causes the noise floor?

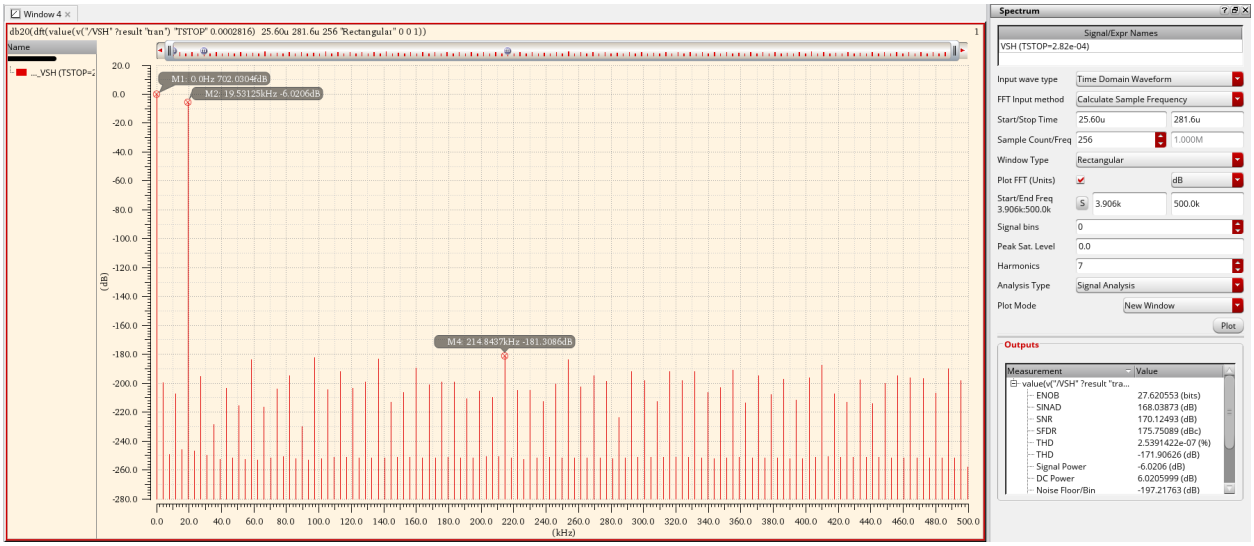


Figure 1.3: Spectrum of VSH @ NCYC = 5

a. - 6.02 dB = $10 \log_{10} 0.5^2$

b. 1

c. -197.2

d. $\text{FFT}_{\text{noise floor}} = 10 \log {V_{lsb}^2}/{12} - 10 * \log {\text{NFFT}}/{2} = 10 \log(\text{Sig}_{\text{power}}) - \text{SQNR} - 10 \log {\text{NFFT}}/{2}$

e. Because of numerical errors and nonlinearities and distortion components of the input sine wave

10. Change NCYC to 5.5 and re-simulate. Note that the start and stop time in the DFT will change from the previous case. Plot the new FFT. Observe the spectral leakage.

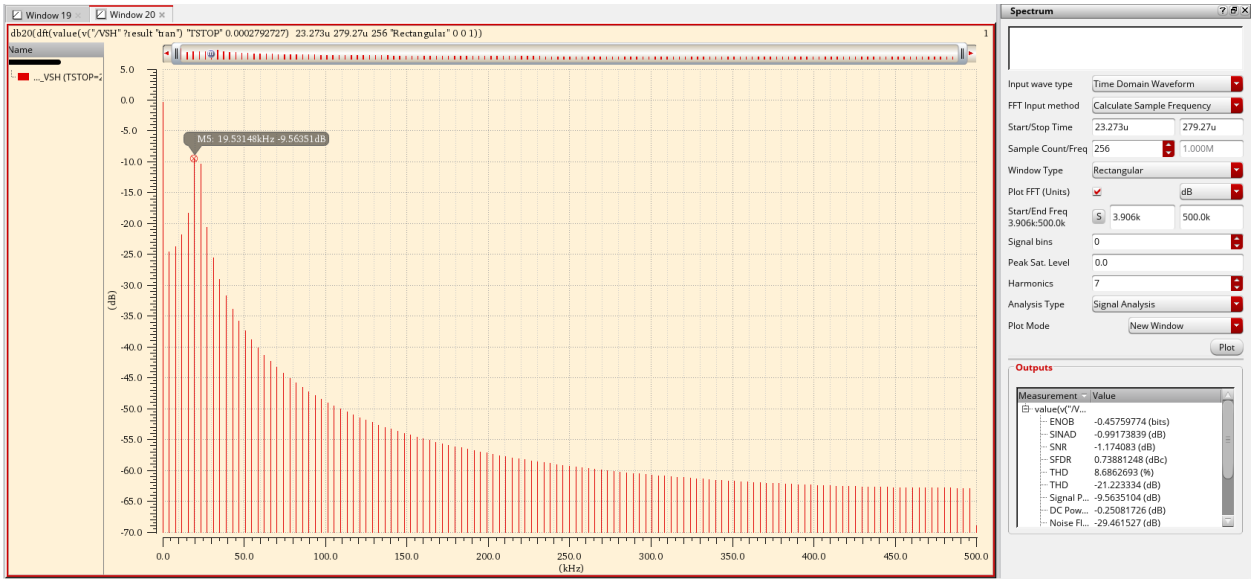


Figure 1.4: Spectrum of VSH @ NCYC = 5.5

The leakage is due to abrupt transition because NCYC doesn't equal an integer number so Coherent condition is not satisfied leading to Spectral Leakage.

2. Quantization

1. Use Modelwriter to create a veriloga model for a **10-bit** ADC. Create a symbol for the generated view.

2. Similarly, use it to create a veriloga model for a 10-bit DAC. Create a symbol for the generated view.

3. Create a new testbench as shown below.

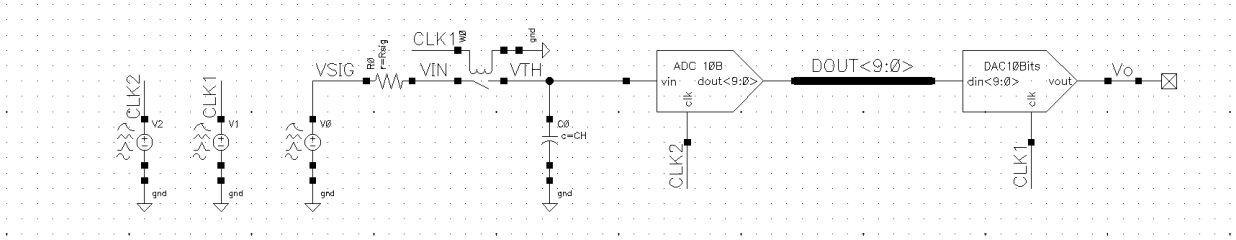


Figure 2.1: Quantization TB

4. Create a new adexl view. Set global variables as in Part 1. Set transient analysis as in Part 1.

5. Plot the transient waveforms and study the timing relations between different signals.

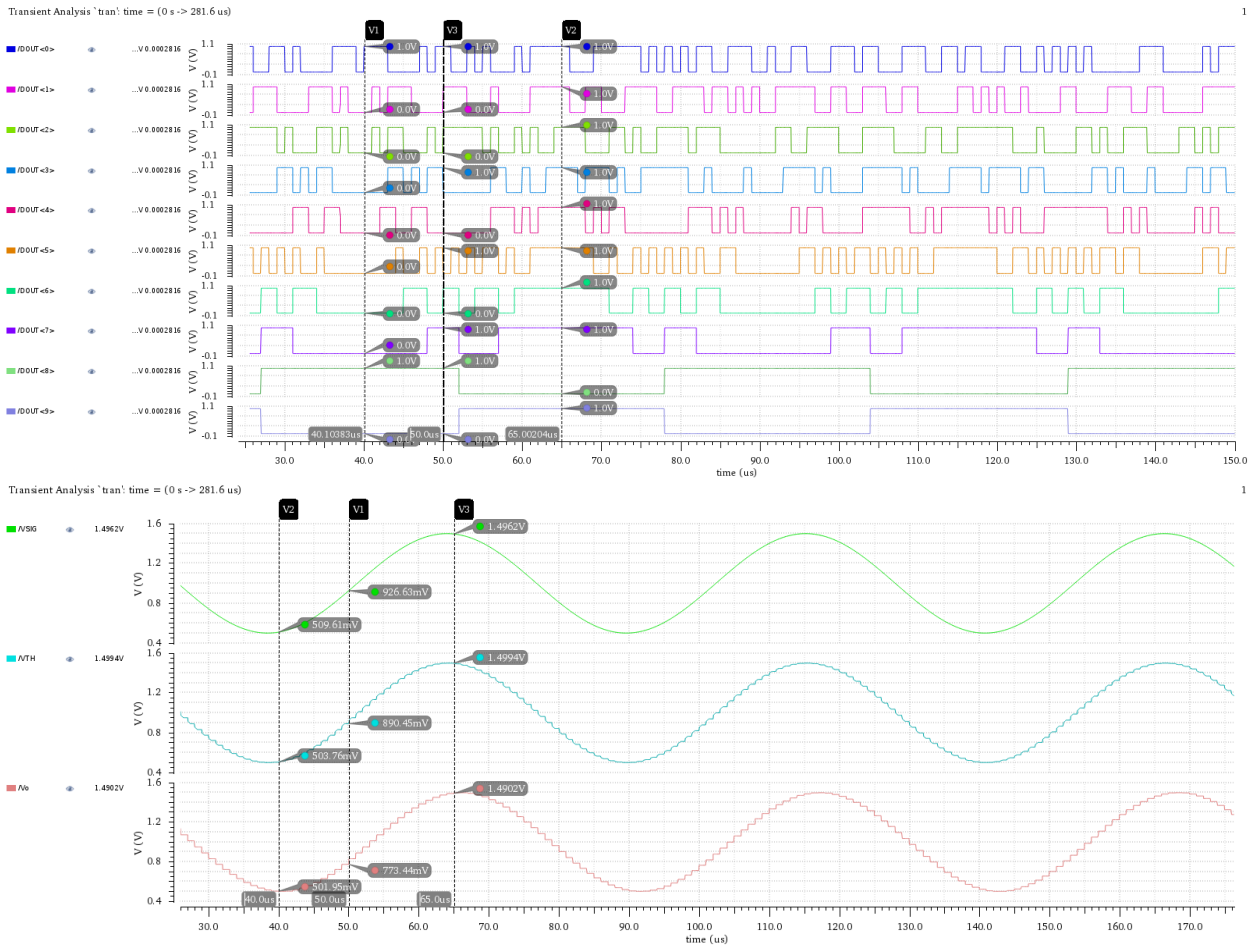
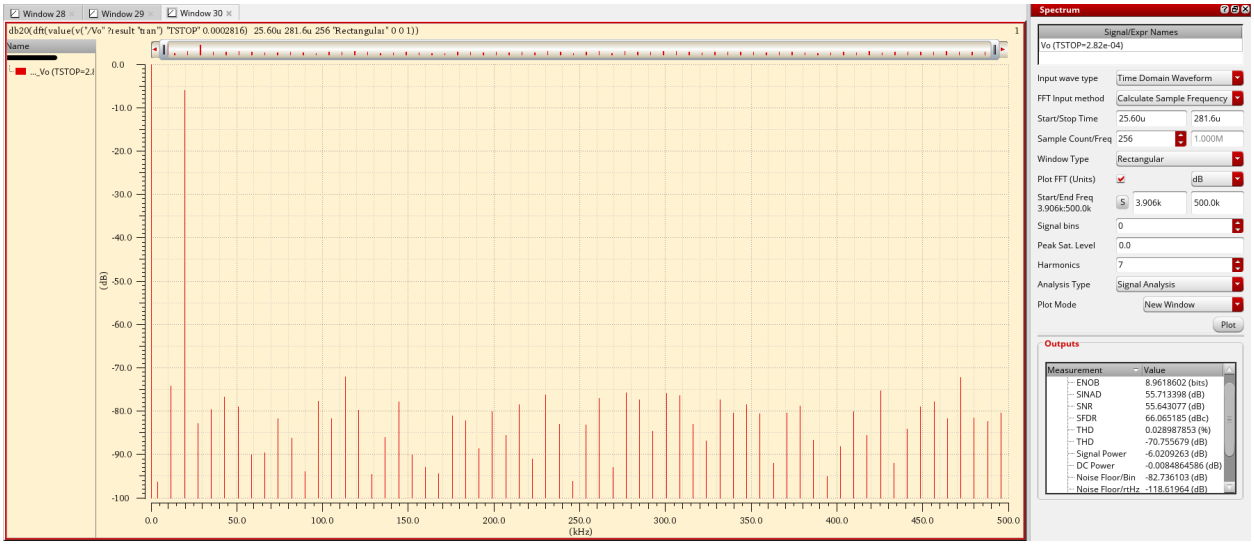


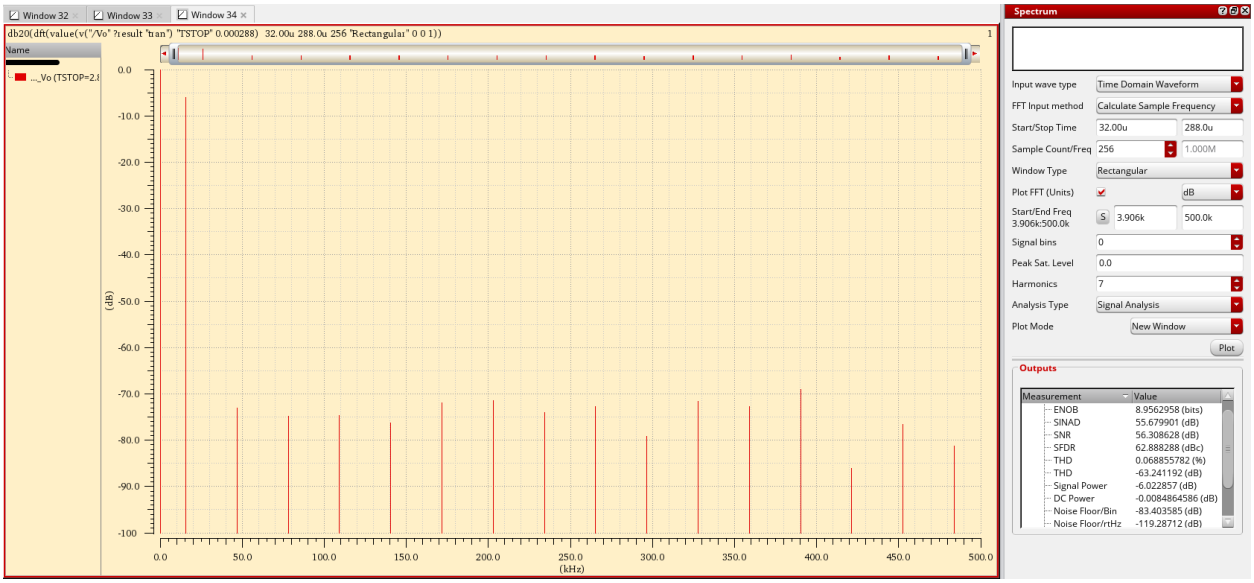
Figure 2.2: (a) ADC digital output (b) DAC analog output Vs ADC analog input

6. Analyze the DAC output using the spectrum assistant. The result will be as shown below. Compare the SNR, ENOB, Signal Power, DC Power, and Noise Floor with the expected theoretical values.



	Expected theoretical	Simulator
SNR	$6.02 * N + 1.76 = 6.02 * 10 + 1.76 = 61.96$ dB	55.64 dB
ENOB	10 Bits	8.96 Bits
Signal Power	$10 \log 0.5^2 = -6.02$ dB	- 6.02 dB
DC power	$10 \log 1^2 = 0$	0.00848 dB
Noise Floor	$SNR - 10 \log M/2 = 61.96 - 10 \log 128 = -83.03$ dB	- 82.73 dB

8. Change NCYC to 4 and re-simulate. Plot the new FFT. Note that the start and stop time in the DFT will change from the previous case. Compare the new SFDR with the previous one. Comment.



	NCYC = 5	NCYC = 4
SFDR	66.065 dB	62.888 dB

SFDR of the second case is smaller because there's correlation between the sampling frequency and the input frequency so the Harmonics power will not spread which means there will be Higher harmonics Since, SFDR = Sig power – max (noise power) so SFDR will decrease or in simpler words the sampling frequency and the test tone are corelated which makes the quantization error periodic causing more spurs in the frequency domain which decrease the SFDR while in the first case they aren't corelated which makes the error random and spreads it in frequency domain making it behave more like white noise.

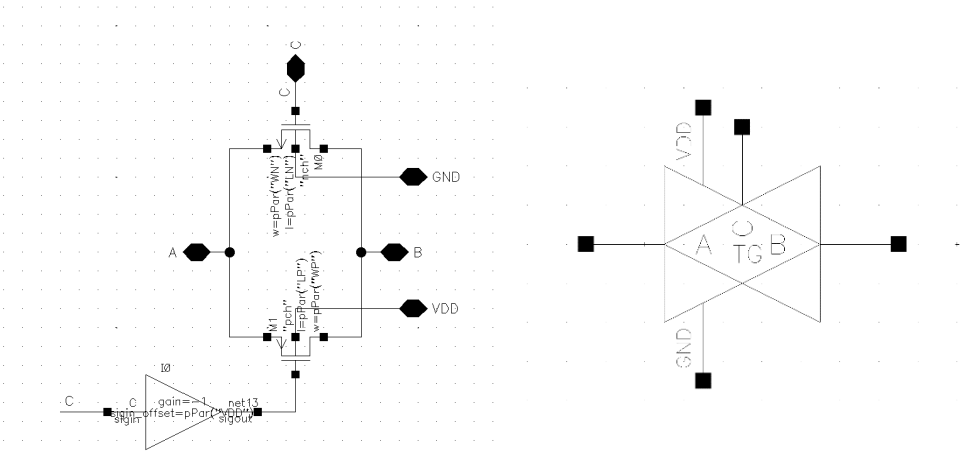
Analog Integrated Systems Design

Lab 04: Sample and Hold circuits

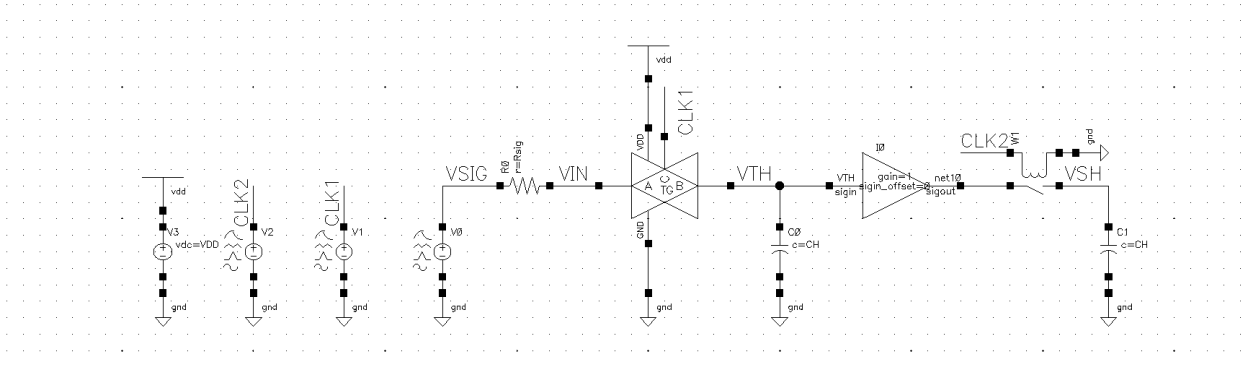
Apr. ٤, 2022

1. S&H Artifacts

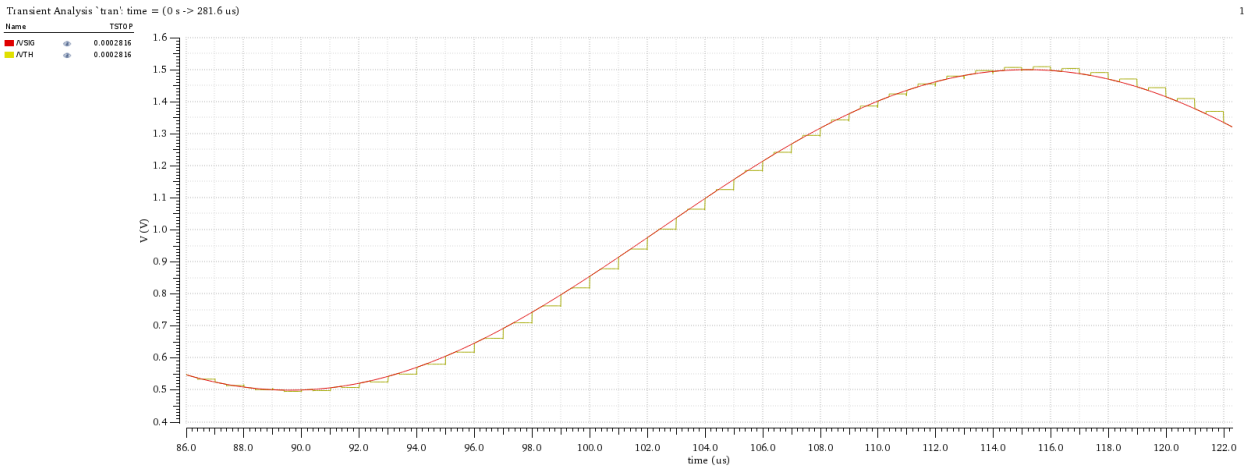
1. Create a new cell. Construct the circuit shown below. The schematic consists of two T&H circuits separated by an ideal buffer.



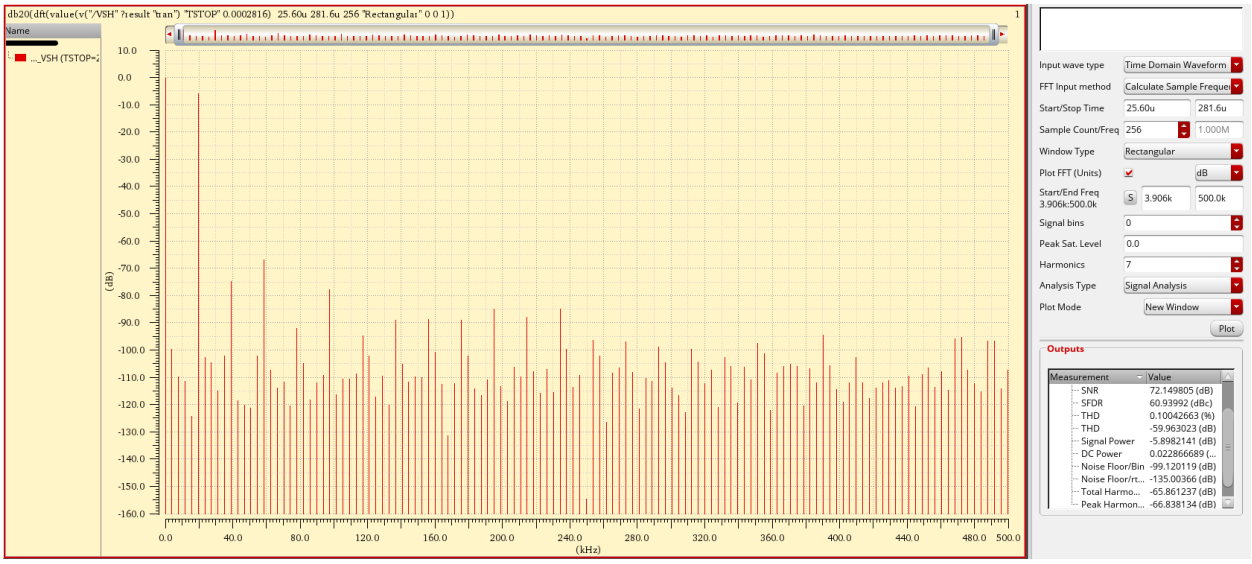
2. Modify the circuit as shown below. The schematic is similar to Lab 02 Part 1, but the first ideal switch is replaced by a transmission gate (TG). For the TG, set LN = LP = technology minimum and WN = WP = 10um.



3. Run transient analysis. Plot VSIG and VTH overlaid. Zoom in to observe the S&H artifacts.



3. Use the Spectrum Assistant to plot FFT for VSH. Compare results below with Lab 02 Part 1 results in a table. Comment on the differences.



Test	Output	Nominal	Spec	Weight	Pass/Fail
Training:02_SAH_TB:1	DC power	22.87m			
Training:02_SAH_TB:1	ENOB	9.627			
Training:02_SAH_TB:1	SFDR	60.94			
Training:02_SAH_TB:1	Sig power	-5.898			
Training:02_SAH_TB:1	SINAD	59.72			
Training:02_SAH_TB:1	SNB	-99.12			
Training:02_SAH_TB:1	SNR	72.15			
Training:02_SAH_TB:1	THDdB	-59.96			

(a)

Test	Output	Nominal	Spec	Weight	Pass/Fail
Training:02_SAH_TB:1	DC power	702f			
Training:02_SAH_TB:1	ENOB	27.61			
Training:02_SAH_TB:1	SFDR	175.3			
Training:02_SAH_TB:1	Sig power	-6.021			
Training:02_SAH_TB:1	SINAD	168			
Training:02_SAH_TB:1	SNB	-197			
Training:02_SAH_TB:1	SNR	170			
Training:02_SAH_TB:1	THDdB	-172.1			

(b)

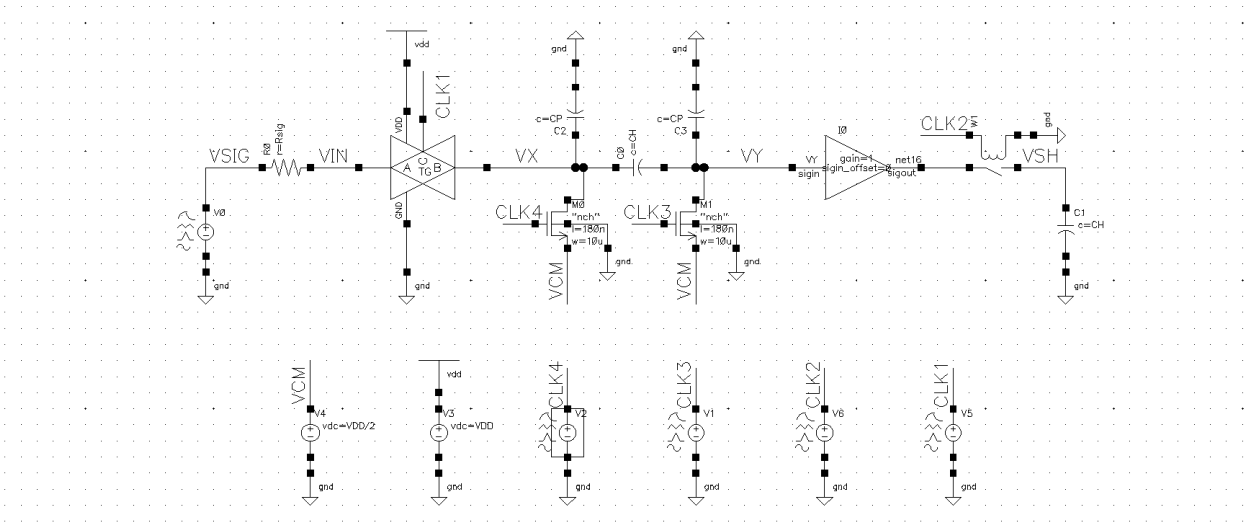
Table 1: (a) Spectrum parameters for VSH with TG (b) Spectrum parameters for VSH with ideal switch

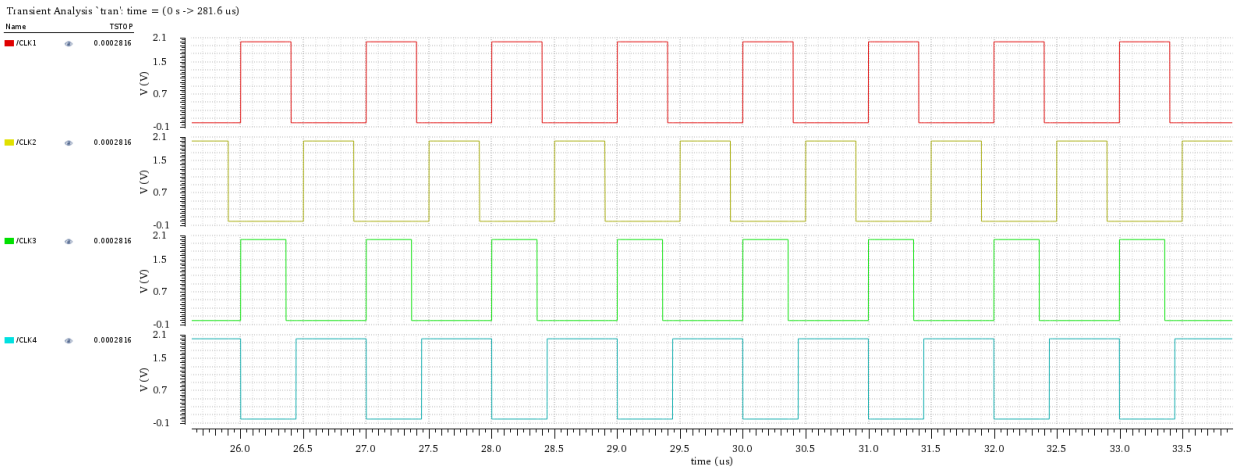
Comment:

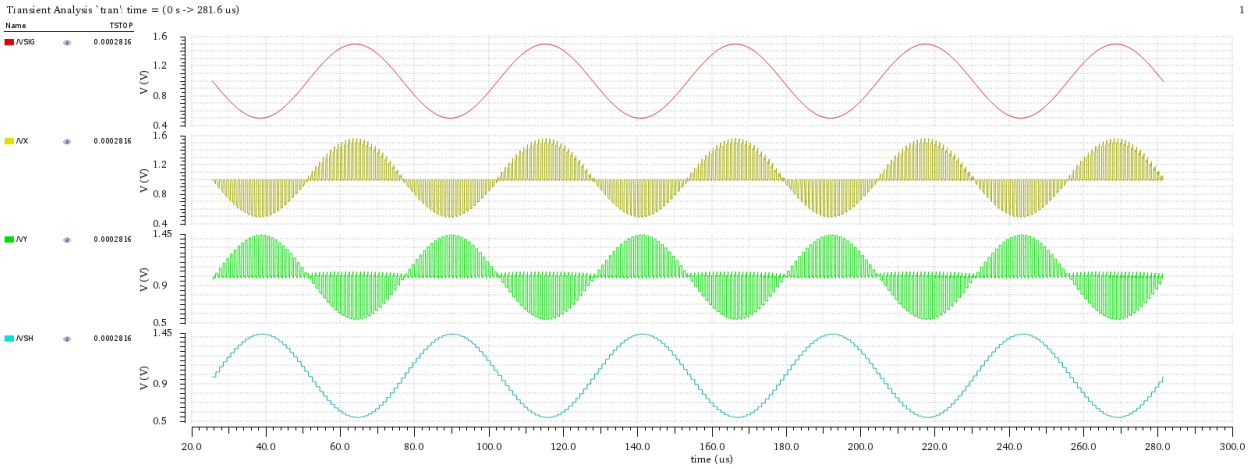
Adding only a TG to the sample and hold circuit makes large changes as it introduce nonlinearities e.g., CI and CF to the circuit where it is a nonlinear elements introducing harmonics and noise leading to increase in the total harmonic distortion and decreasing ENOB ,SINAD , SNR & SFDR.

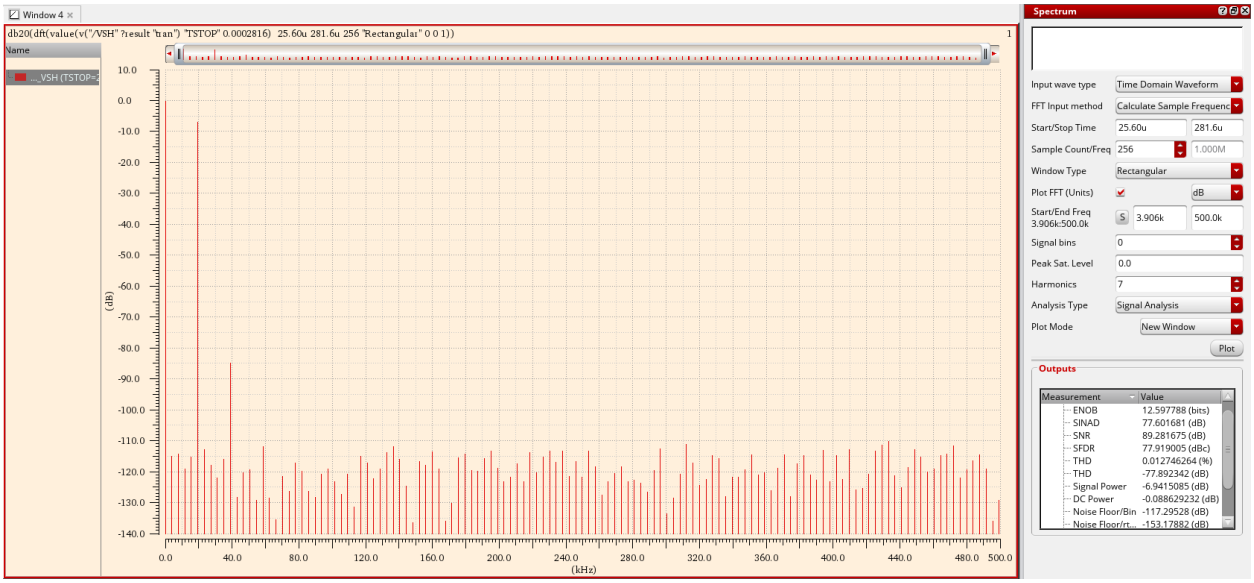
2. Bottom Plate Sampling

1. Copy the testbench to a new cell. Construct the circuit shown below. Bottom plate sampling is used. The capacitors “CP” model the parasitic capacitors at VX and VY.






Transient Analysis `tran': time = (0 s -> 281.6 us)
Name
TSTOP
/VSIG
0.0002816
/VX
0.0002816
/VY
0.0002816
/VSH
0.0002816
V (V)
time (us)


Window 4
Name
Spectrum
Input wave type
Time Domain Waveform
FFT Input method
Start/Stop Time
25.60u
281.6u
Sample Count/Freq
256
1.000M
Window Type
Rectangular
Plot FFT (Units)
dB
Start/End Freq
3.906k:500.0k
3.906k
500.0k
Signal bins
Peak Sat. Level
Harmonics
Analysis Type
Signal Analysis
Plot Mode
New Window
Plot
Outputs
Measurement
Value
ENOB
12.597788 (bits)
SINAD
77.601681 (dB)
SNR
89.281675 (dB)
SFDR
77.919005 (dBc)
THD
0.012746264 (%)
THD
-77.892342 (dB)
Signal Power
-6.9415085 (dB)
DC Power
-0.08862932 (dB)
Noise Floor/Bin
-117.29528 (dB)
(dB)
(kHz)