Spec.			
Two Stage Miller Compensated OTA			
Supply voltage	1.2	CMIR	0.2 : 0.6 V
Static gain error	<= 0.05 %	Output swing	0.2 – 1 V
CMRR @ DC	>= 74 dB	Load	5 pF
Phase margin	>= 60 degree	Buffer CL rise time (10% to 90%)	<= 70 ns
OTA current consumption	<= 60 uA	Slew rate (SR)	5 V/us

- Steps

General Considerations

01 | As CMIR is closer to the GND rail → use PMOS input pair for the 1st stage

02 | The current mirror load of the second stage should be the same as the current tail of the first stage (PMOS) since they are both current mirrors so the second stage input transistor should be NMOS, Also the VGS of the second stage input pair should be the same as VGS of the current mirror load of first stage (NMOS) to cancel the offset.

03 | Assume $C_c = 0.5\ C_L = 2.5\ pF$

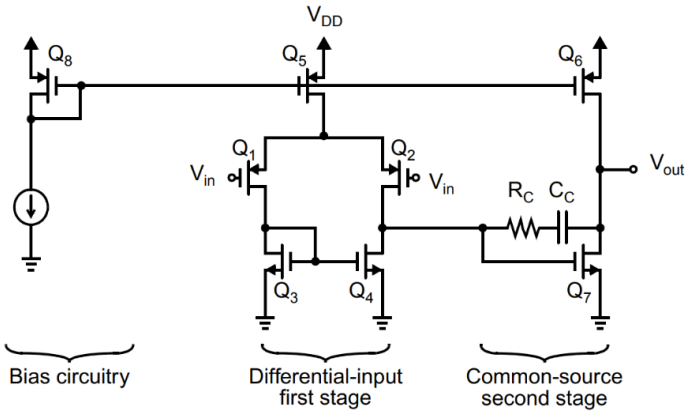
04 | $\because SR = \frac{I_{B1}}{C_C} = \frac{5}{10^6} \rightarrow I_{B1} = 12.5\ uA \rightarrow I_{B2} = I_{total} - I_{B1} = 60\ uA - 12.5\ uA = 47.5\ uA$

05 | $\because t_{rise} = 2.2\ \tau = 2.2\ RC = \frac{2.2}{2\pi\ BW_{CL}} = 70\ ns \rightarrow BW_{CL} = 5\ MHz$

06 | $\therefore BW_{CL} = UGF_{CL} = \frac{g_{m1,2}}{2\pi\ C_C} = 5\ MHz \rightarrow g_{m1,2} \geq 78.5\ uS \rightarrow g_{m1,2} = 125\ uS$

07 | $\because A_{VCL} = \frac{A_{VOL}}{1+\beta A_{VOL}} = \frac{1}{\frac{1}{A_{VOL}}+1} = 1 - \frac{1}{A_{VOL}} \rightarrow \epsilon_s = \left|\frac{Actual-ideal}{ideal}\right| * 100 \rightarrow \frac{0.05}{100} \geq \left|\frac{1-\frac{1}{A_{VOL}}-1}{1}\right| = \frac{1}{A_{VOL}}$

08 | $\therefore A_{VOL} \geq 2000 = 66\ dB$



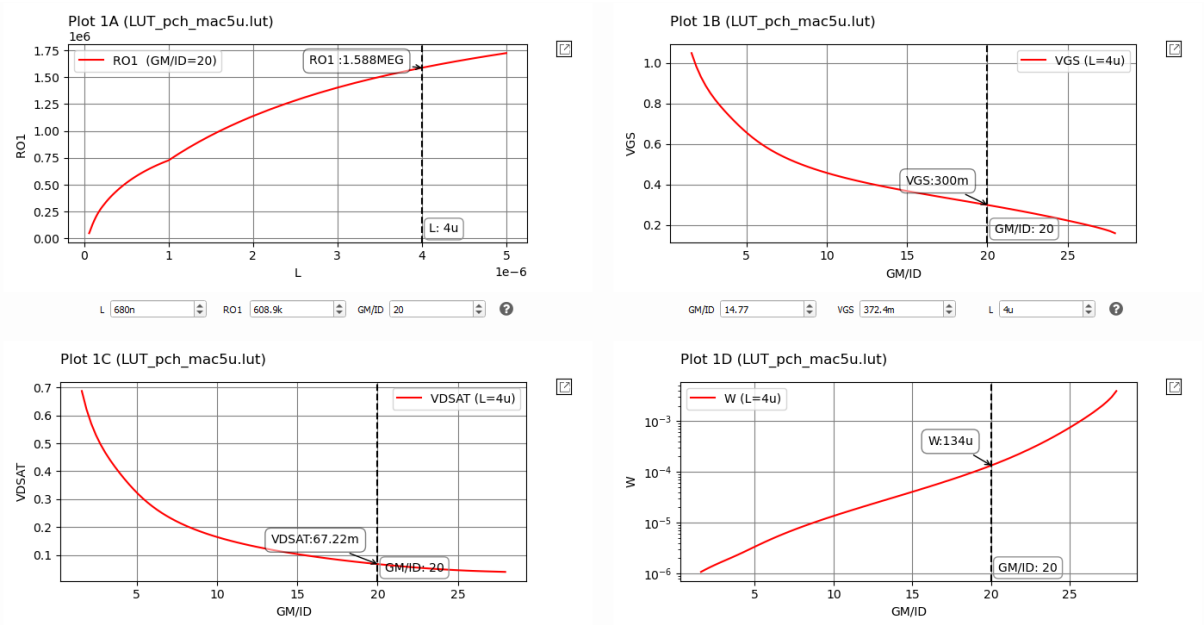
Sizing of M1,2

09 | We assign higher gain to the first stage as it has lower current so we can get higher gain easier, also we need higher gain to get high CMRR, also to reduce the input referred noise of the second stage. If we want to get higher gain of the second stage, we should use cascaded devices which limits output swing.

10 | $A_{V1} = 65 = 36.02\ dB$ and $A_{V2} = 31 = 31\ dB$

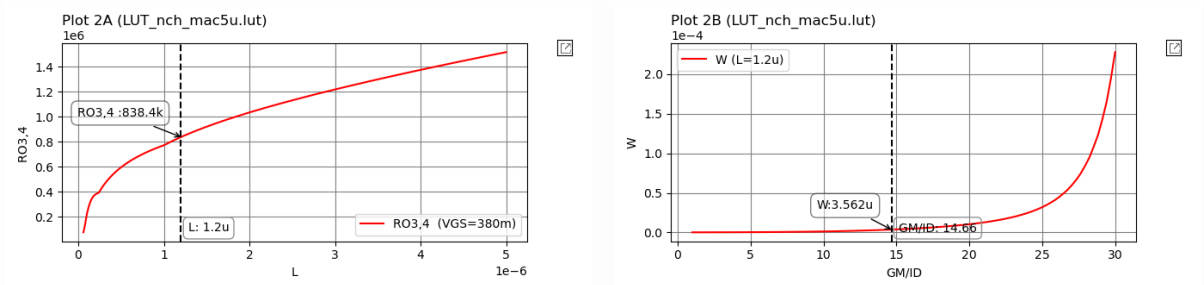
11 | $\frac{g_{m1,2}}{I_D} = \frac{125\ uS}{6.25\ uA} = 20\frac{S}{A} \rightarrow A_{V1} = g_{m1,2} \times R_{out1} = g_{m1,2} \times r_{o1,2} \parallel r_{o3,4}$

12 | Assume $r_{o1,2} = 2r_{o3,4} = r_o \rightarrow A_{V1} = g_{m1,2} \times \frac{r_o}{3} \geq 65 \rightarrow r_{o1,2} = 1.56\ M\Omega$ and $r_{o3,4} = 780\ K\Omega$



Sizing of M3,4

13 | $\text{CMIR}_\text{L} = -\text{V}_{\text{SG1,2}} + \text{V}^*_{1,2} + \text{V}_{\text{GS3,4}} \leq 0.2\ \text{V} \rightarrow \text{V}_{\text{GS3,4}} < 0.4 \rightarrow \text{V}_{\text{GS3,4}} = 0.38\ \text{V}$ and $\text{r}_{\text{o3,4}} = 780\ \text{k Ohm}$

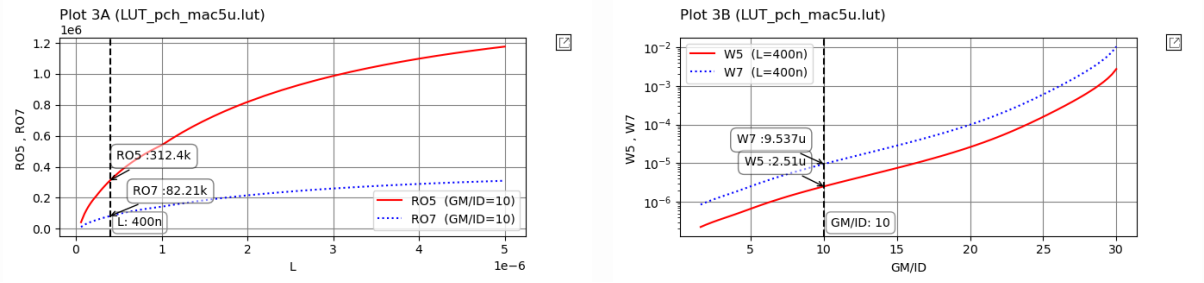


Sizing of M5,7

14 | Set $\text{L}_5 = \text{L}_7$ and $\text{V}_{\text{GS5}} = \text{V}_{\text{GS7}}$

15 | $\text{CMRR} = 5012 = \text{g}_{\text{m1,2}} \times \text{r}_{\text{o1,2}} \times \text{g}_{\text{m3,4}} \times \text{r}_{\text{o5}} \rightarrow \text{r}_{\text{o5}} \geq 280\ \text{k Ohm}$

16 | $\text{CMIR}_\text{H} = -\text{V}_{\text{SG1}} - \text{V}^*_5 + \text{V}_{\text{DD}} > 0.6\ \text{V} \rightarrow \text{V}^*_5 \leq 300\ \text{mV} \rightarrow$ Choose $\text{V}^*_5 = \text{V}^*_7 = 200\ \text{mV} \rightarrow \frac{\text{gm}_{5,7}}{\text{I}_\text{D}} = 10$



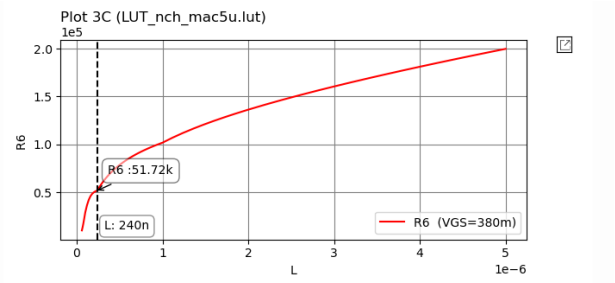
Sizing of M6

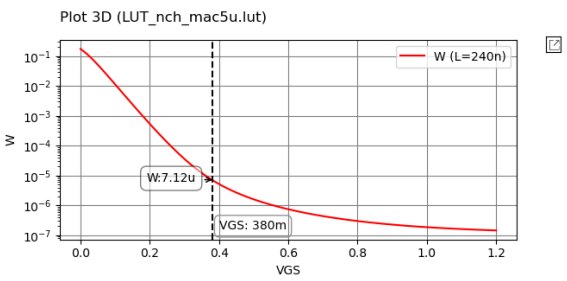
17 | Set $\text{V}_{\text{SG6}} = \text{V}_{\text{SG3,4}}$ to cancel the systematic offset

18 | For critical damped response : $\frac{\text{G}_{\text{m2}}}{\text{C}_\text{L}} = \frac{4\text{G}_{\text{m1}}}{\text{C}_\text{C}} \rightarrow \text{G}_{\text{m2}} = 8\ \text{G}_{\text{m1}} = 1\ \text{mS}$

19 | $A_{V_2} \geq 31 \rightarrow g_{m6} \times R_{out2} = g_{m2} \times r_{o6} \,||\, r_{o7} \geq 31$

20 | $r_{o6} \geq 49.76K\,\text{Ohm} \;@\; V_{GS6} = 380\,\text{mV}$



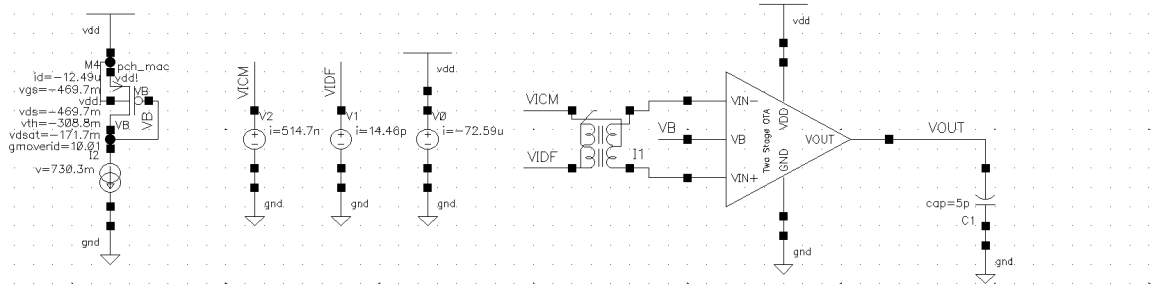


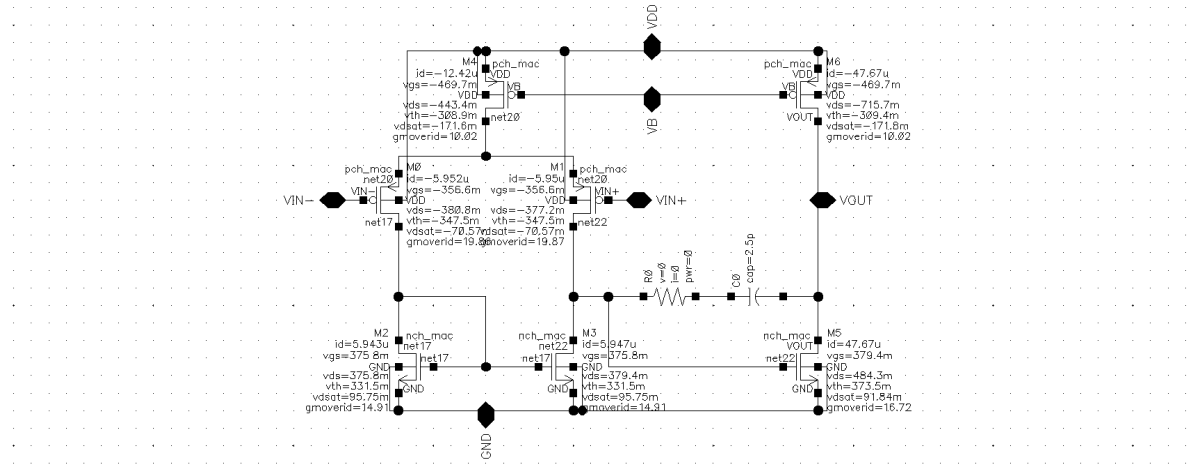
- Sizing Summary

Sizing Summary					
M	M1,2	M3,4	M5	M6	M7
Rule	1st stage input stage	Active load of 1st	Current mirror of 1st stage	2nd stage input device	Current mirror of 2nd stage
L	4 um	1.2 um	400 nm	240 nm	400 nm
W	134 um	3.56 um	2.51 um	7.12 um	9.537 um

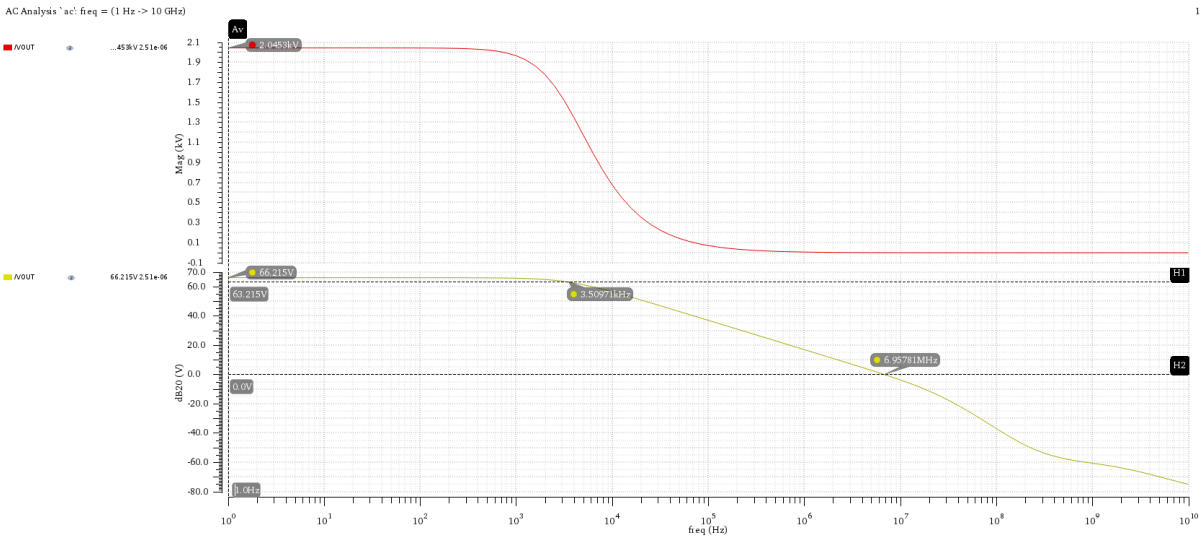
- Results

1. TB and DC Operating Point



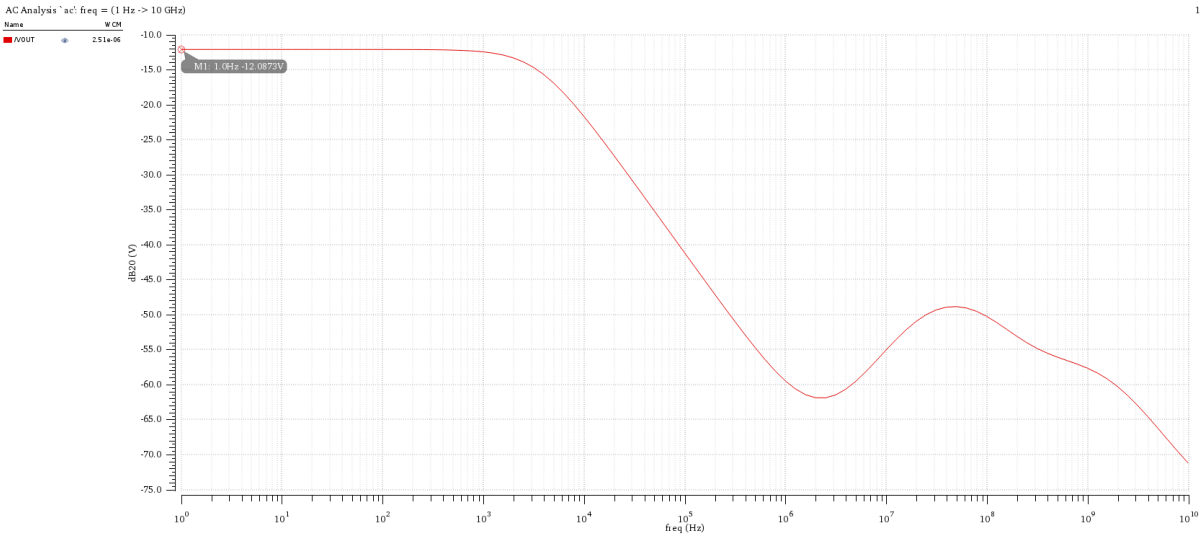


2. Differential Small Signal Analysis

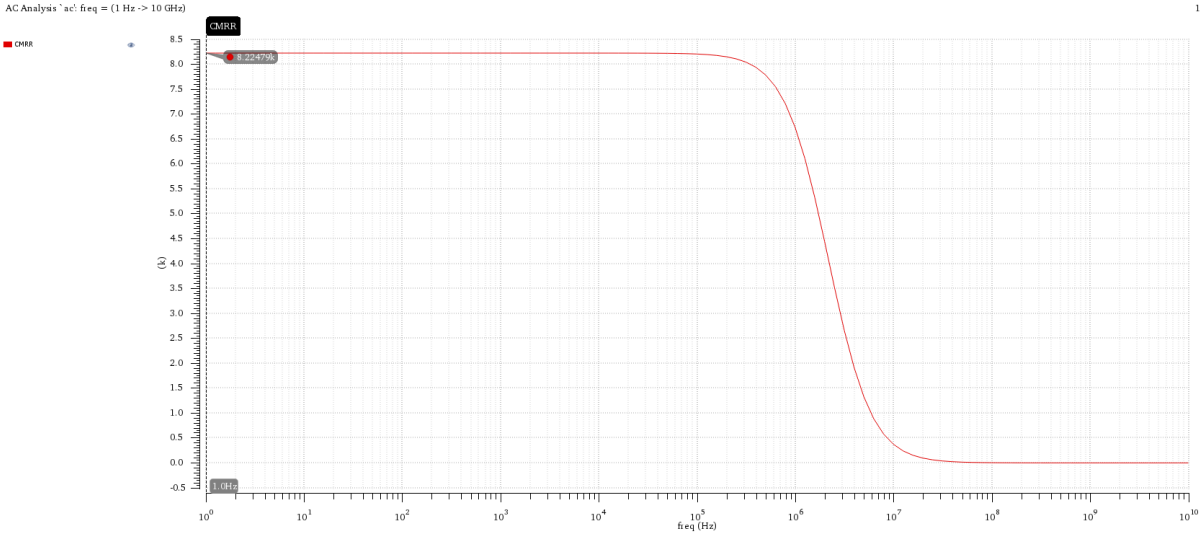


3. Common Mode Small Signal Analysis

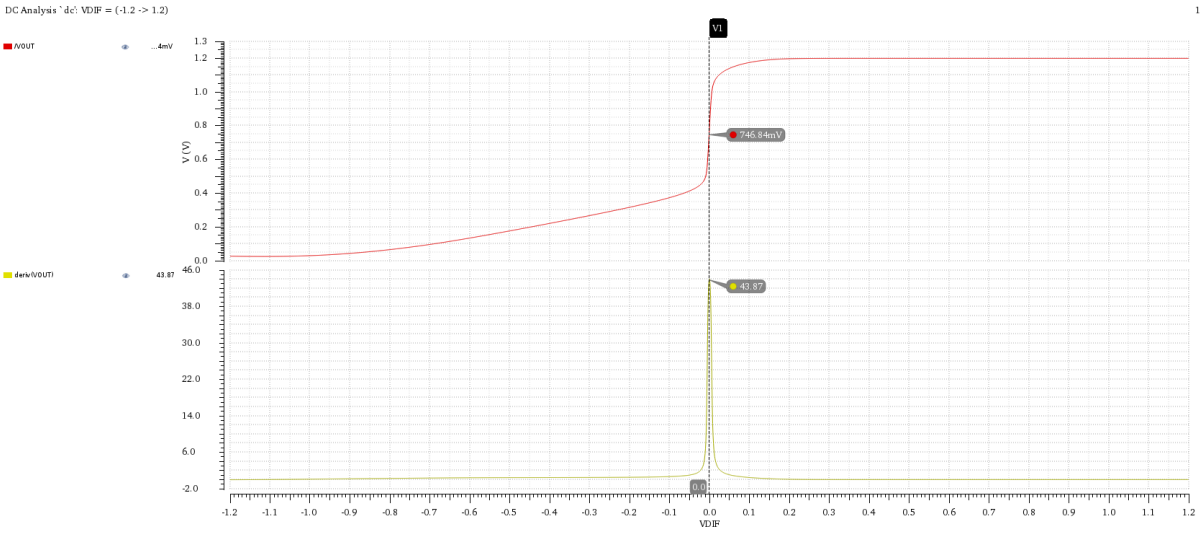
- AVCM



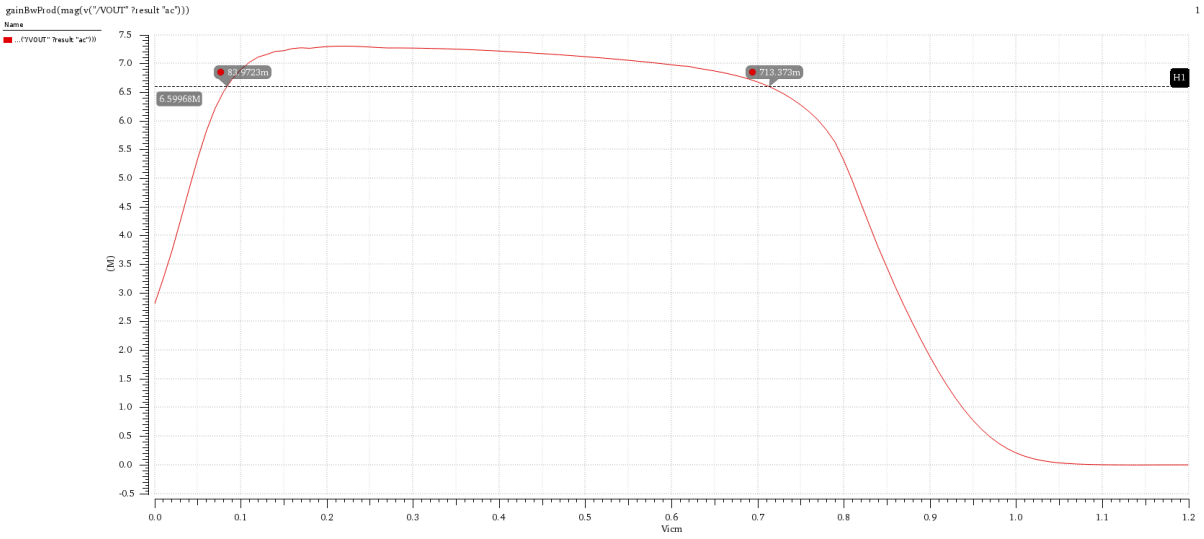
- CMRR



4. Differential Large Signal Analysis



5. Common Mode Large Signal Analysis



6. STB Analysis