Spec.			
5T - OTA			
Supply Voltage	1.2 V	Power Consumption	≤ 30 uW
Open loop DC voltage gain	≥36 dB	Reference current	10 uA
CMRR @ DC	≥50 dB	Linear Range	90 mVpp
BW	≥100 kHz	Load	2 pF

- Steps

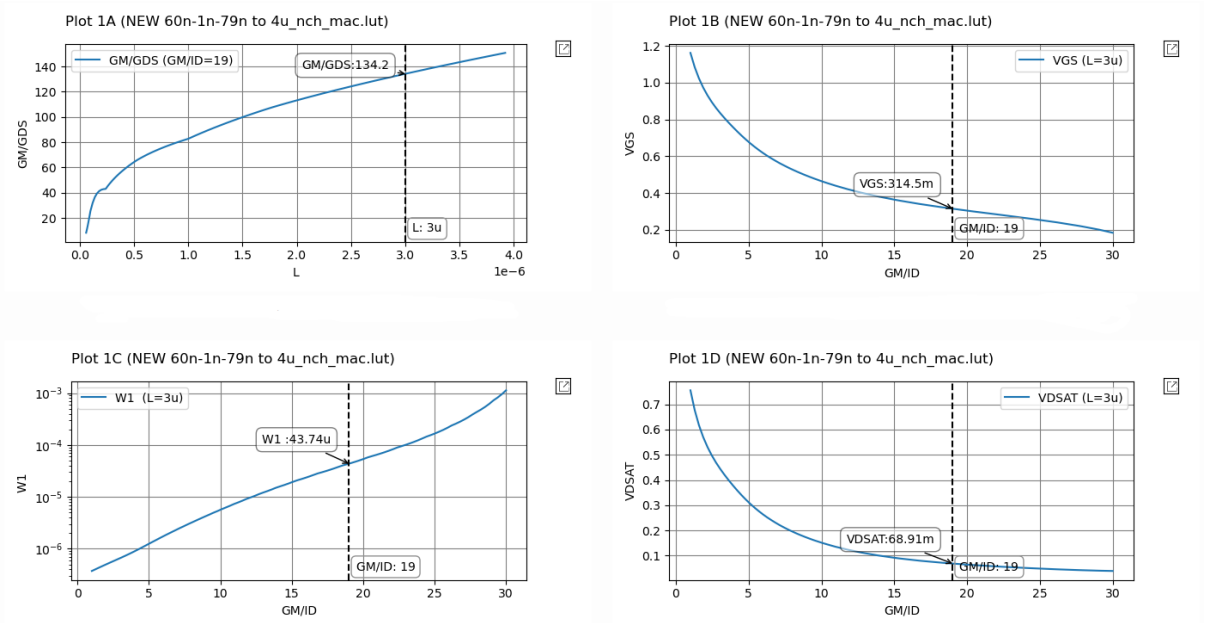
- Design of input transistors

01 | $P_{cons} = V_{DD}\, I_{ss} \leq 30\ uW \rightarrow I_{ss} \leq 25\ uA$

02 | $GBW = \frac{g_{m1}}{2\pi C_L} \geq 6.4\ MHz \rightarrow g_{m1} \geq 80.5\ uS \rightarrow \left(\frac{g_m}{I_D}\right)_1 \geq 6.44 \rightarrow \left(\frac{g_m}{I_D}\right)_1 = 19 \rightarrow g_m = 237.5\ uS$

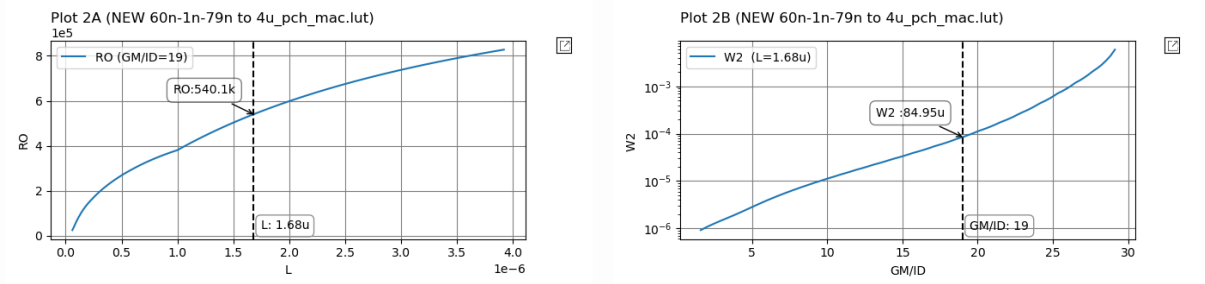
03 | $A_v = g_m R_{out} = 64 \rightarrow Rout = r_{o1} || r_{o2} = \frac{r_o}{2} \rightarrow r_o = 539\ k\Omega \rightarrow \left(\frac{g_m}{g_{ds}}\right)_1 \geq 128$

04 | $L_1 = 3\ um, V_{GS1} = 314.5\ mV, W_1 = 43.74\ um, V_{Dsat1} = 68.91\ mV$



- Diode connected load

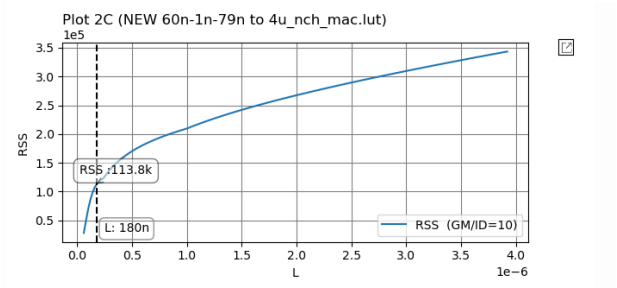
05 | $r_{o2} = 539\ k\Omega$, assume $g_{m1} = g_{m2} = 237.5\ us \rightarrow \left(\frac{g_m}{g_{ds}}\right)_2 = 19 \rightarrow L_2 = 1.68\ um, W_2 = 84.95u\ um$

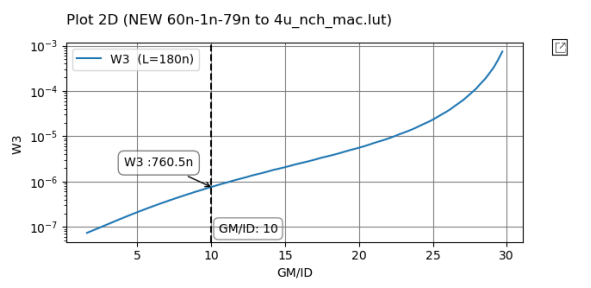


- Current mirror

06 | $A_{VCM} = \frac{1}{2g_m R_{ss}} = (50 - 36)\ dB = 0.1995 \rightarrow R_{ss} = 10.6\ k\Omega$

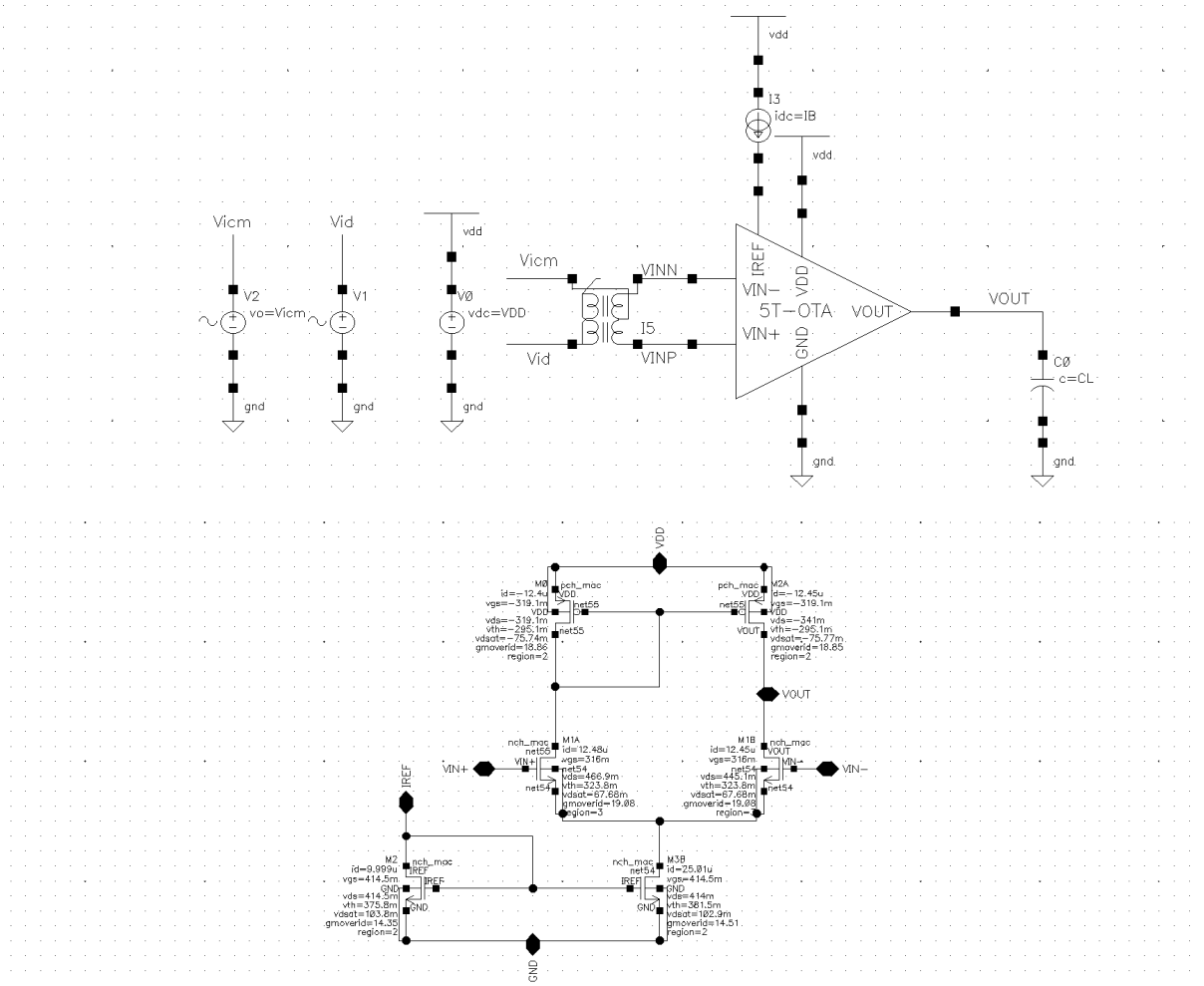
07 | Assume M_3 biased in SI (gmoverid = 10) $\rightarrow L_3 = 180\ nm, W_3 = 760.5\ nm$



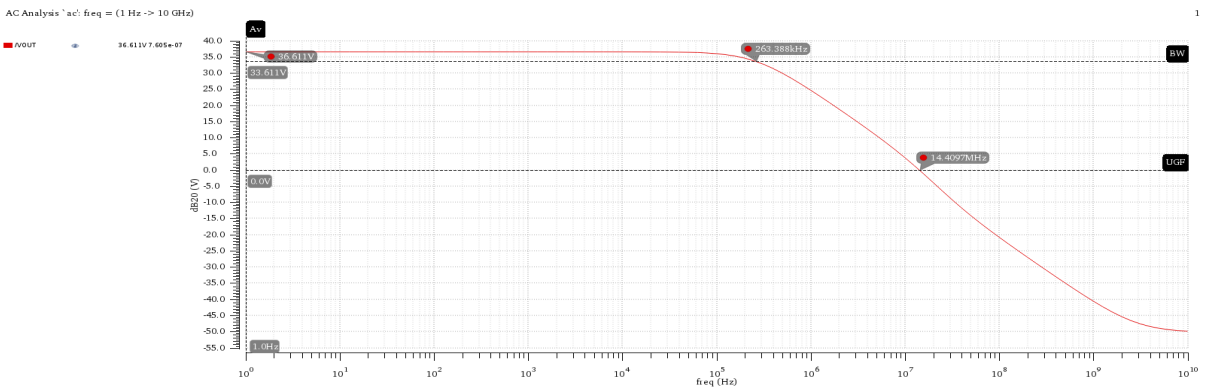


- Simulation Results

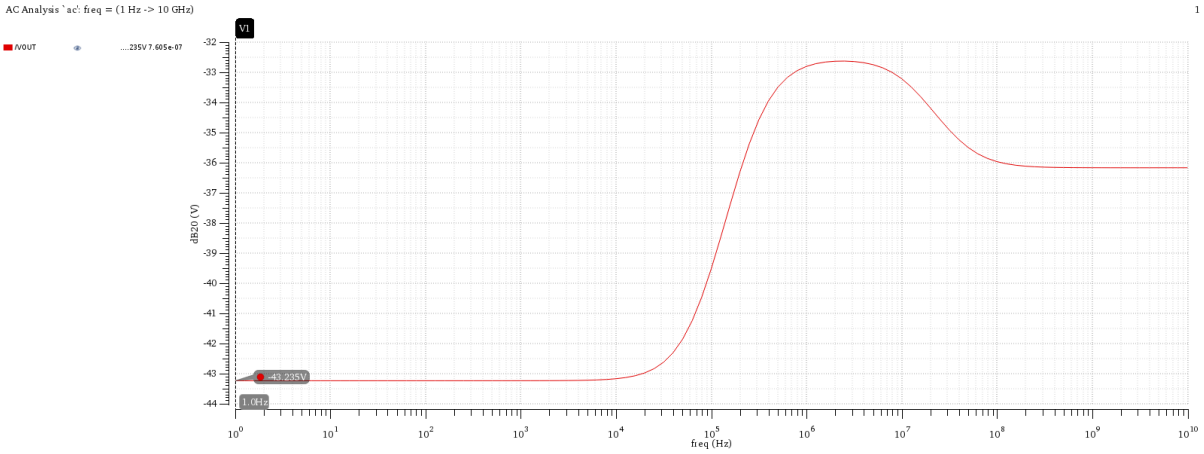
1. DC operating points and Circuit Test Bench



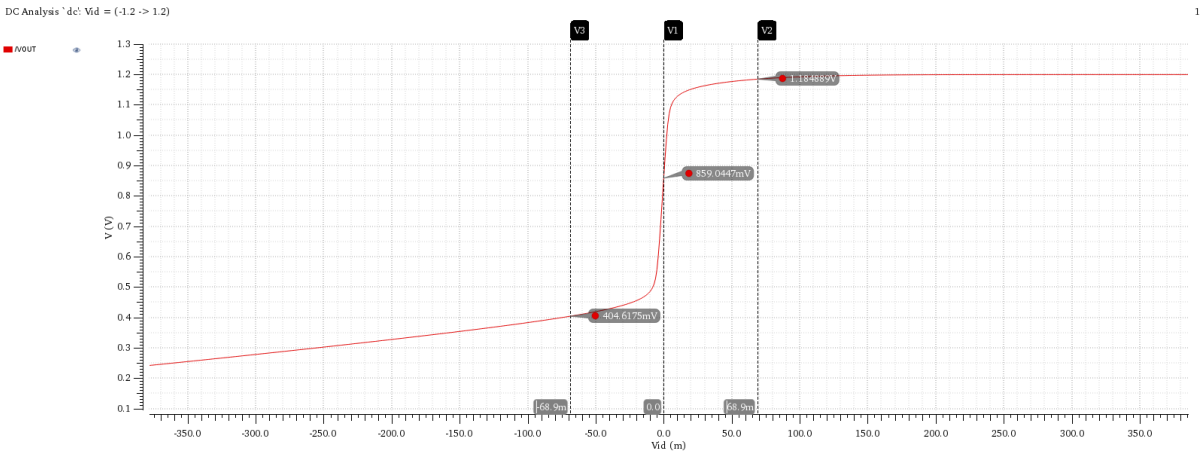
2. Diff Small Signal Analysis



3. CM Small Signal Analysis



4. Diff Large Signal



5. CM Large Signal