Analog Integrated Systems Design

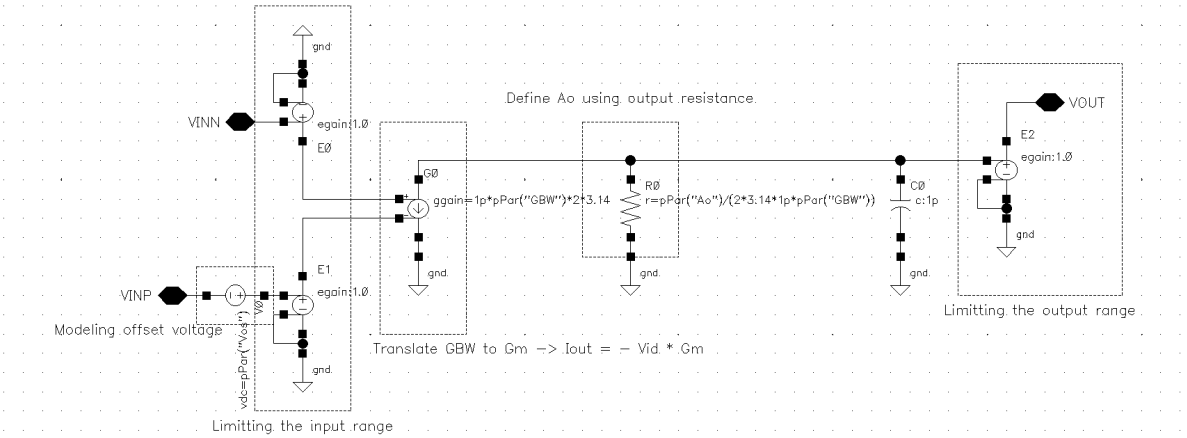
LAB No.6 - Capacitive Digital-to-Analog Converter

- **Objective**

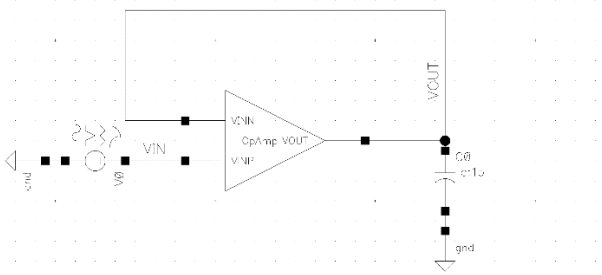
  - To be able to model an op-amp with different types of imperfection.
  - To be familiar with the simulation and characterization of digital-to-analog converters.
  - To be familiar with the operation of capacitive DACs.

- **PART 1: Single-ended Output Op-amp Behavioral Model**

  01 | Create the schematic shown below to model a single-ended output op-amp with finite gain, finite input range, finite output range, and finite GBW. Use vccs and vcvs from analogLib

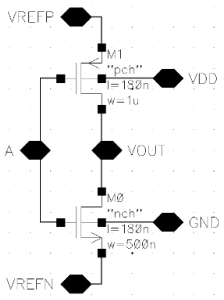


  02 | Create a simple testbench to verify your op-amp. An example testbench is shown below. Set the input as a sinusoidal signal (FIN, VDC, VPK). Run transient analysis for 4/VAR("FIN") conservative (four input cycles).

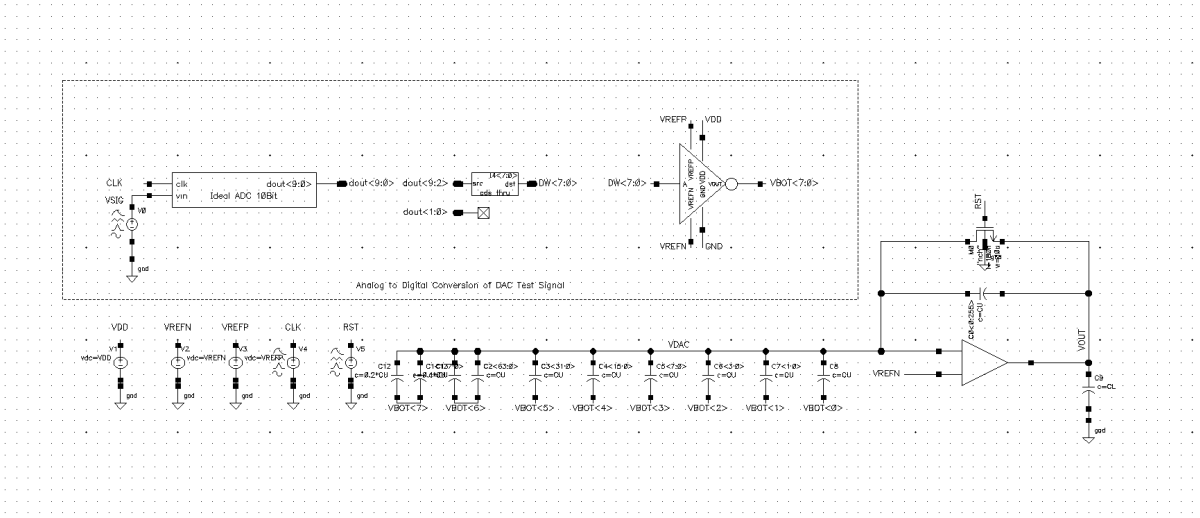


- **PART 2: Capacitive DAC (Ramp Test)**

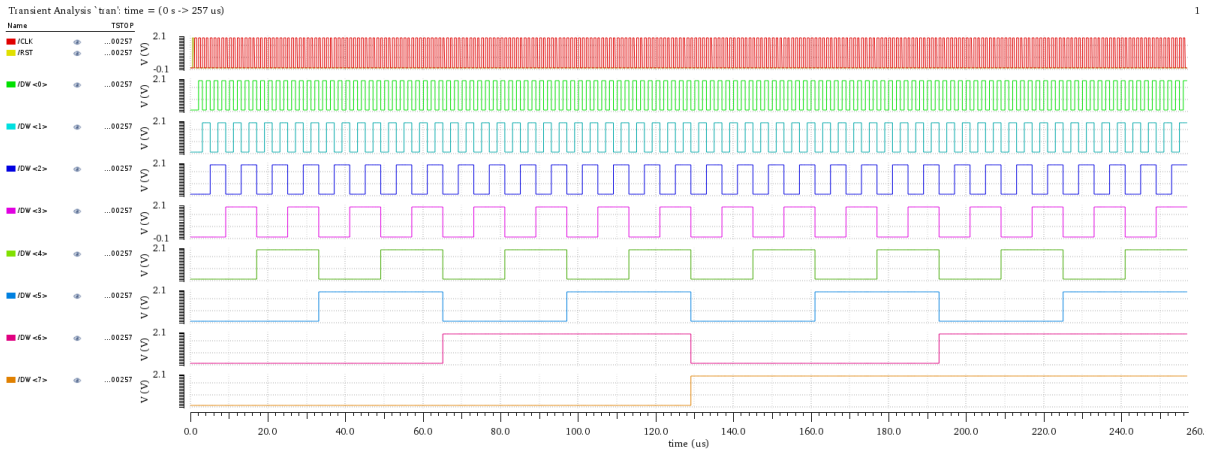
  03 | Create a schematic for a bottom plate switch. It is similar to a digital inverter, but the bottom and top rails are defined by VREFN and VREFP instead of GND and VDD.



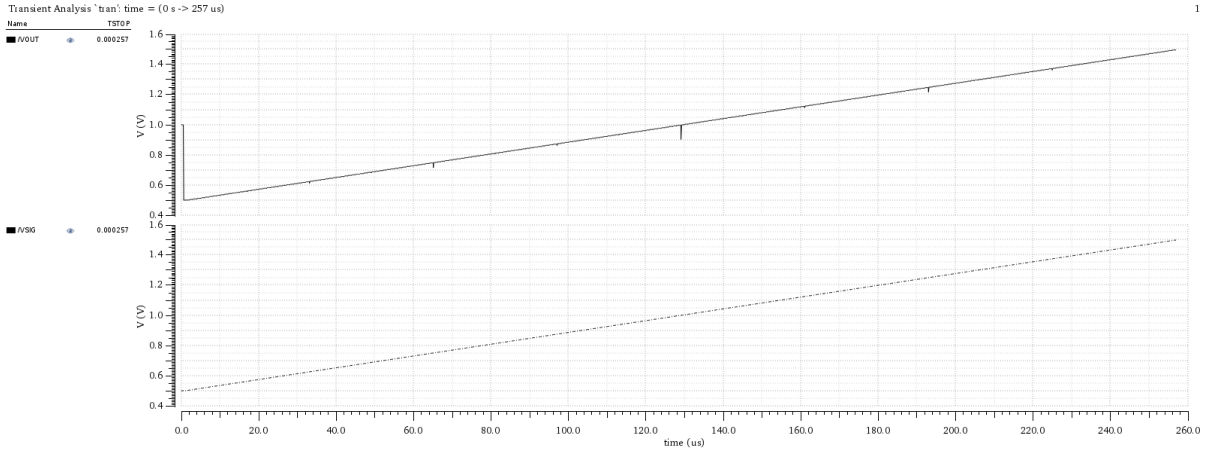
04 | Create the schematic of the capacitive DAC shown below.



05 | Set transient analysis and Plot the transient waveforms and verify correct input stimulus.



06 | Plot DAC output and verify correct DAC operation. Observe the glitches in the DAC output.

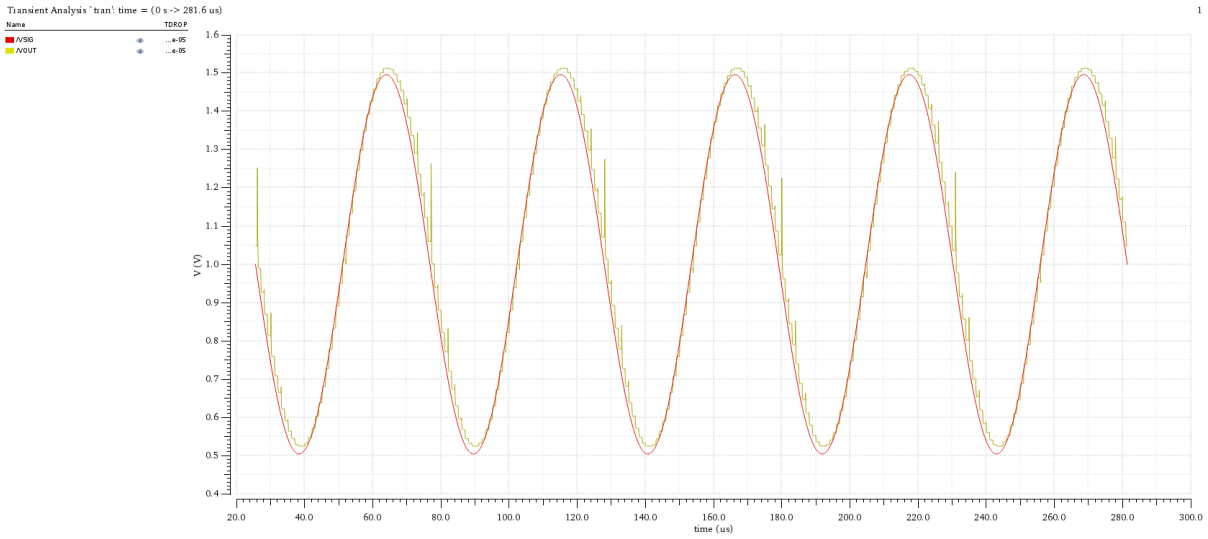


07 | Export the transfer function to a table and copy the data to Excel or MATLAB. Plot the DNL and the INL An example MATLAB code is shown.

```
dvout = vout(2:end)-vout(1:end-1);
lsb = mean(dvout)
dnl = dvout/lsb - 1;
inl = cumsum(dnl)
subplot(211); plot(dnl); axis tight; ylabel('DNL (LSB)');
subplot(212); plot(inl); axis tight; ylabel('INL (LSB)');
```

- **PART 3: Capacitive DAC (Sine Wave Test)**

01 | Modify the input signal source, Plot transient waveforms.



02 | Plot the FFT of the DAC output to measure the ENOB and other performance parameters.