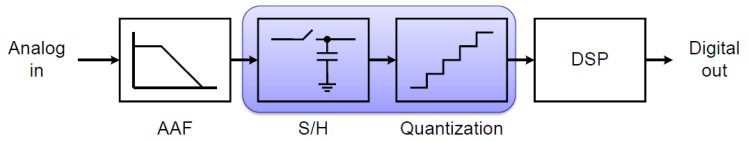
Analog Systems Design

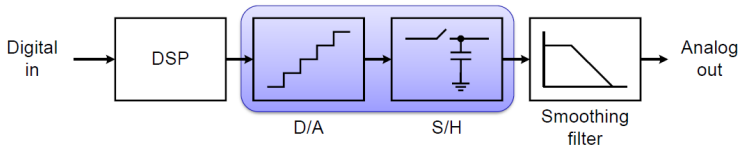
5. Data Converters Specifications 2 (AC characteristics)

1. ADC Vs DAC

   - ADC



   - DAC



   - Signals could be **Unipolar** : 0 to FS or **Bipolar** : -FS to FS

2. Dynamic AC Specifications

   - Signal to quantization noise ratio

     1) Is the ratio between the signal power and the quantization noise power (assuming the quantization noise is uniformly distributed from 0 to fs/2)

$$SQNR = 10\log\left(\frac{Signal\ Power}{Quantization\ Power}\right) = 20\log\left(\frac{V_{sigrms}}{V_{Qnrms}}\right)$$

$$Signal\ Power = \frac{\left(\frac{2^N V_{LSB}}{2}\right)^2}{2} = \frac{2^{2N} V_{LSB}^2}{8}$$

$$Quantization\ Power = \frac{V_{LSB}^2}{12}$$

$$SQNR = 10\log\left(\frac{Signal\ Power}{Quantization\ Power}\right) = 10\log\left(\frac{3}{2}2^{2N}\right)$$

$$\boldsymbol{SQNR = 6.02 \times N + 1.76 \quad [dB]}$$

     2) If only part of the spectrum is useful, some quantization power can be filtered out (digital filtering). Select a bandwidth (BW) out of the available spectrum (0 to fs/2)

$$SQNR = 10\log\left(\frac{Signal\ Power}{Quantization\ Power \times \frac{BW}{f_s/2}}\right)$$

$$SQNR = 6.02 \times N + 1.76 + \mathbf{10\log\left(\frac{f_s/2}{BW}\right)}$$

     3) Harmonic distortions means that the output signal for an input at f_O will be at f_O and its multiples

     Harmonics are at $|\pm kf_S \pm nf_O|$; n = order of the harmonic, k = 0,1,2,3,…

     Remember the only part of the spectrum that has a physical meaning is 0 → fs/2

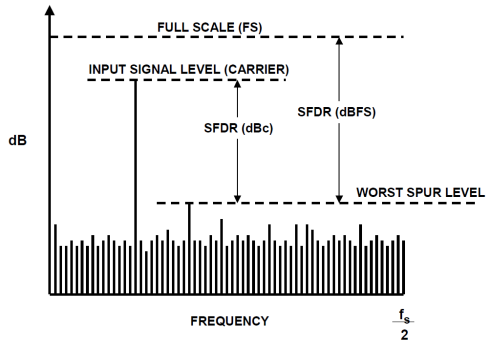
- SNR, SINAD (SNDR), and ENOB
  1) SNR : Signal to noise ratio (without the harmonic distortions)
     The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other components, excluding the first 5 or 7 harmonics and DC

  2) SINAD (SNDR): Signal to noise and distortion ratio (with harmonics)
     The ratio of the rms signal amplitude to the mean value of the root-sum-squares (RSS) of all other components, including the first 5 or 7 harmonics and excluding DC

  3) ENOB : the effective number of bits for a data converter

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02}\ \text{dB}$$

- SFDR : Spurious free dynamic range
  1) SFDR is the ratio of the rms signal amplitude to rms value if the peak spurious spectral component over the bandwidth of interest
  2) If it measured relative to input signal SFDR will be measured by dBc (c is referred to carrier or input signal) and if it measured relative to full scale it will be in dBFS



- Summary

  - ❑ Signal-to-noise ratio

$$SNR = 10\log\left(\frac{Signal\ Power}{Random\ Noise\ Power}\right)$$

  - ❑ Total harmonic distortion

$$THD = 10\log\left(\frac{P_{distortion}}{P_{signal}}\right) = 20\log\left(\frac{V_{distortion}}{V_{signal}}\right)$$

  - ❑ Signal-to-noise-and-distortion ratio (SNDR or SINAD or THD+N)

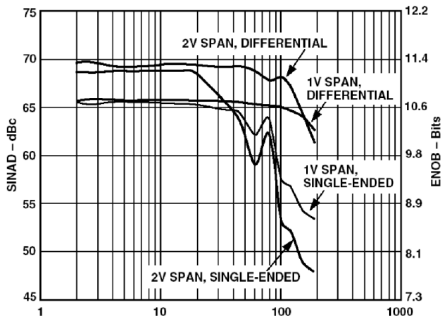
$$SNDR = SINAD = 10\log\left(\frac{Signal\ Power}{Power\ of\ all\ unwanted\ signals}\right)$$

  - ❑ Spurious free dynamic range (SFDR) (spurious signal = unwanted)

$$SFDR(dBc) = 10\log\left(\frac{Signal\ Power}{Power\ of\ highest\ spurious\ signal}\right)$$

  1) A good 8 bit ADC will have ENOB around 7 5 bit (0 5 bit loss).
  2) A good 12 bit ADC will have ENOB around 11 bit (1 bit loss).
  3) For high frequency, undersampling ADCs, and high resolution ADCs, the ENOB loss can be much higher (may be $>$ 4 bit)

- SINAD/ENOB Example
  - ❑ AD9226 12-bit, 65-MSPS ADC SINAD and ENOB
    - SINAD/ENOB degrades as frequency increases
    - 2V better than 1V (ideally by 6 dB, but limited by distortion)
    - Differential better than SE at high frequency



- ADCs Figures of Merit
  1) Different ADCs have different resolution, speed, power consumption, etc.
  2) How to compare them together?
     Use a normalized " figure of merit (FoM) to compare the most important specs combined together (**1**. Resolution: ENOB or SNR - **2**. Speed: BW or fs - **3**. Power consumption)
  3) Speed Vs Power
     Assume we want to double the speed of a thermal noise limited circuit.
     - This means GBW must be doubled. → If the capacitance (noise) is constant, this means Gm must be doubled. → Current is doubled as well.

     Power consumption is doubled.
     - Conclusion: Power consumption is proportional to speed (bandwidth or fs)

     --- The ratio $fs/Power$ tends to be constant.

     --- This can be a good FoM (for a constant SNR).
  4) ENOB vs Power
     Assume we want to increase ENOB of a thermal noise limited design by 1 bit.
     - $2^{ENOB} = \frac{V_{REF}}{LSB} = \frac{V_{REF}}{\sqrt{kT/C}} \rightarrow 2^{ENOB+1} = 2 \times \frac{V_{REF}}{\sqrt{kT/C}} = \frac{V_{REF}}{\sqrt{kT/4C}}$
     - The capacitance is quadrupled.
     - To maintain same speed (GBW), G_m must be quadrupled.
       - Current is quadrupled as well.
       - Power consumption is quadrupled.

     Conclusion: Adding one more bit means quadrupling the power.
     - The ratio $\frac{Power}{2^{ENOB}}$ does not seem to be a good FoM.
     - But it is the most widely used ADCs FoM in the literature!

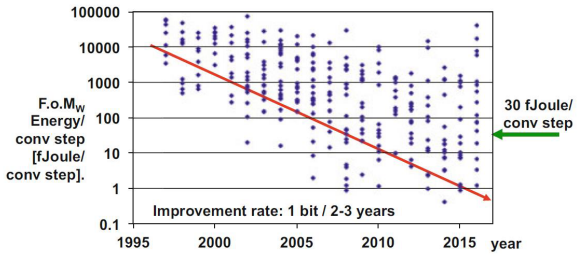
- Walden Figure of Merit FoM_W

$$FoM_W = \frac{P_{ADC}}{2^{ENOB} \times f_S}$$

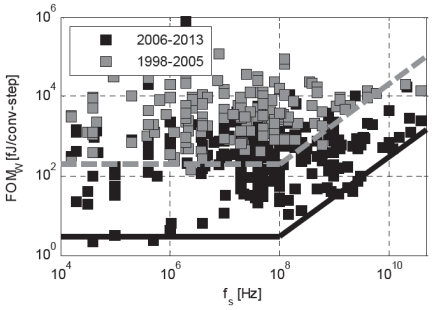
  1) Empirical formula , but fits well with practical ADCs
     - It was good FoM @ 90s But not all ADCs are thermal noise limited
  2) Better used to compare ADCs of the same resolution or low resolution
  3) Unit of FoM_W is fj / conversion-step

- State of art in industry is around 100 fj/step
- State of art in academia is less than 1 fj/step

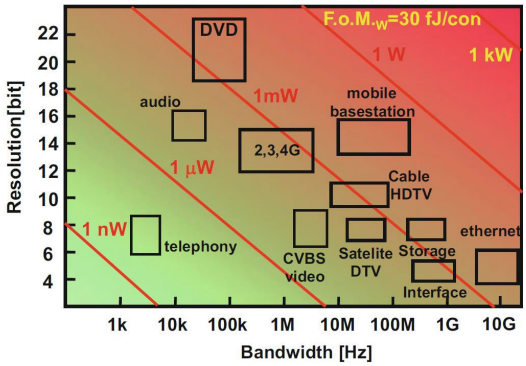
4) Note that the lower is the better for FoM_W
5) ISSCC papers from 1997 to 2016
   - State of the art ADCs have FoM better than 1 fJ/Step!



6) ISSCC and VLSI Symp . papers from 1998 to 2013
   - Clear trend towards better energy efficiency
   - State of the art ADCs have FoM better than 1 fJ/Step



7) Power Consumption Estimation
   - FoM_W can be used to get a quick estimate of power consumption
   - Ex: Assume the ADC has $FoM_W = \frac{P_{ADC}}{2^{ENOB} \times fs} \sim \frac{30fJ}{Step} \rightarrow P_{ADC} \sim \frac{30fJ}{Step} \times 2^{ENOB} \times fs$



- Schreier figure of Merit FoM_S

1) SNR vs Power
   - Assume we want to increase the ENOB of a thermal noise limited design by 1-bit
   - SNR will increased by 6 dB → SNR will be quadrable
   - If ENOB increased by 1-bit → C will be quadrable → for same GBW, Gm will be quadrable → Current will be quadrable → Power will be quadrable
   - So, Conclusion is Power consumption is proportional to SNR
   - The ratio $\frac{SNR}{Power}$ tends to be constant.
   - This can be a good FoM (for a constant speed).

2) $\mathrm{FoM_S}$

$$\mathrm{FoM_S} = 10\log\frac{\mathrm{SNR}\times\frac{f_s}{2}}{P_{ADC}} = \mathrm{SNR_{dB}} + 10\log\frac{\frac{f_s}{2}}{P_{ADC}}$$

- It can be shown that min ADC power is limiting the max $\mathrm{FoM_S}$

$$P_{ADC,minimum} = 16\times kT\times\frac{fs}{2}\times \mathrm{SNR} \rightarrow \mathrm{FoM_{S,maximum}} = 10\log 116\,kT \approx 192\mathrm{dB}$$

- Schreier FoM best fits thermal noise limited designs.
  - ADCs with high resolution (> 14 bit) and modest speed.
  - Use SNDR (SINAD) instead of SNR to include distortion effects.
- Note that for $\mathrm{FoM_S}$, the higher the better

3) ISSCC and VLSI Symp . papers from 1997 to 2015 (after 2010 in red)

- Best practical ADCs are > 10 dB away from the limit.