Analog Integrated Circuits

lec 10: Current mirror.

① Why a Current Source?

1 a Current Source is an ideal Load
- → Set DC bias point accurate
- → Infinite R_{out} (ac O.C)
- → No DC Voltage drop.
- → Small Chip area.

↓

Simply a Large resistor

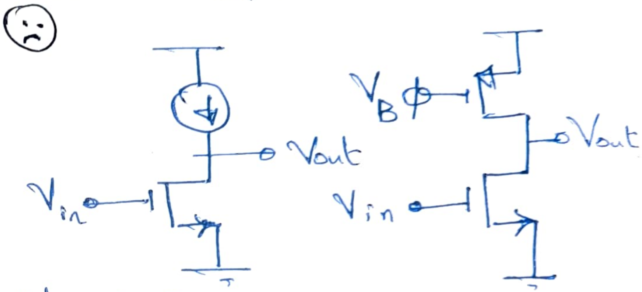
Without Large resistors drawbacks.

but. Current Source is practically implemented using a MOSFET

↓

Finite $R_{out} = r_o$ and Subtract V_{ov} from the Voltage headroom ☹

② Sink and Source Currents.

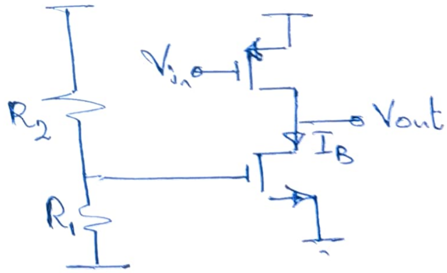


- use PMOS to Source Current (from VDD)
- use NMOS to Sink Current (to GND)

③ Bad Current Source. (where's V_B Comes?)

$$I_B = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_B - V_{TH})^2$$

$$= \frac{\mu C_{ox}}{2}\frac{W}{L}\left(\frac{R_1}{R_1+R_2}V_{DD} - V_{TH}\right)^2$$



Why is Bad?

- Sensitive to PVT
  - → VDD Varies
  - → V_{TH} may Vary ± 50mV (Process Var.)
  - → μ Varies with Process and Temp.
- even if V_B is stable, I_B will not be stable still → depends on V_{TH}, μ, C_{ox} ...

Solution!

1 make a golden ref. Circuit that generate Current I_B insensitive to PVTs → not study how. Just assume it's there.

2 make Copies of this Current.

How to Copy (Mirror) Currents

④ How to Copy (mirror) Current?

- We normally use transistors to Convert V to I

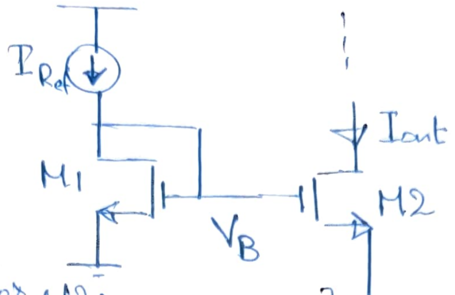
Now. We need to Convert I to V → IReff to VB

↓

using diode Connected transistor (M1)

Will Convert IReff to VB

then (M2) Convert VB to Iout back.



if the to transistors are matched

↳ they will have Same Current.

$$\frac{I_{out}}{I_{Reff}} = \frac{\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_B - V_{TH})^2}{\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_B - V_{TH})^2} = \frac{(W/L)_2}{(W/L)_1}$$

Iout is insensitive to PVT Variations

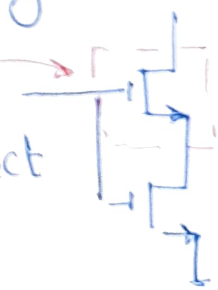
But VB may Change due to PVT Variations.

⑤ Scale Currents up and down

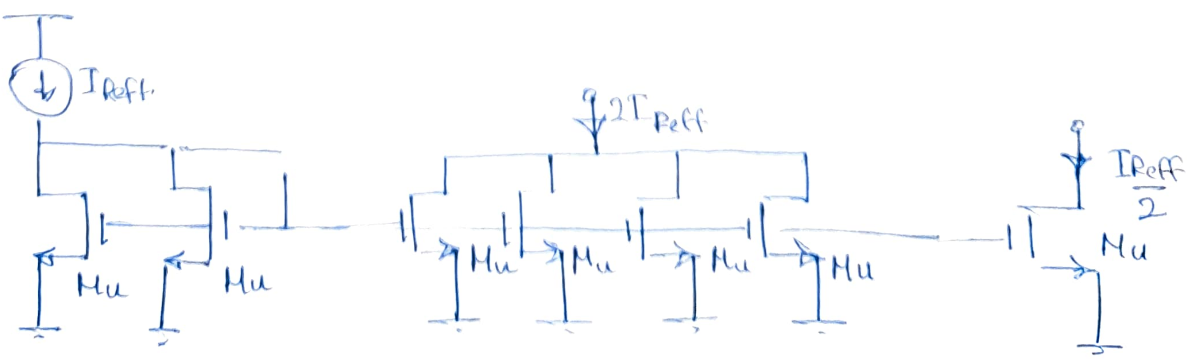
- Currents Can be scaled up or down by Connecting unit transistors in

1 Parallel (accurate)

2 Series (not as accurate) → because body effect



Always use matched unit transistors.



⑥ V_{DS} dependance

- dependance of I_D on V_{DS} introduce two types of errors.

  1. M2 has finite R_{out} → $\frac{\Delta V_{out}}{\Delta I_{out}}$, if V_{out} varies
  ∴ I_{out} will vary

  2. even if V_{out} does not vary, $V_{DS1} \neq V_{DS2}$

- We usually scale W (unite transistors) and keep L equal, so $\lambda_1 \simeq \lambda_2$

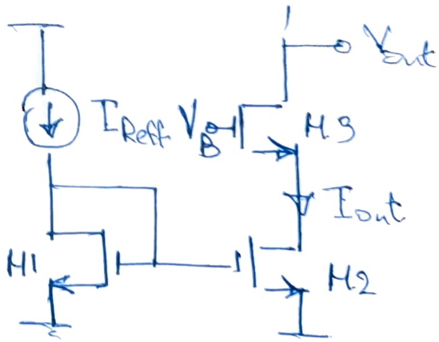
How to solve V_{DS} dependance?

⑦ Cascode current mirrors.

- Boosting R_{out} using cascode will reduce ΔI_{out}

  ∴ $\Delta I_{out} = \frac{\Delta V_{out}}{R_{out}}$

- But still $V_{DS1} \neq V_{DS2}$ a static error in mirroring ratio.



* Set $V_B = V_{GS3} + V_{GS1}$

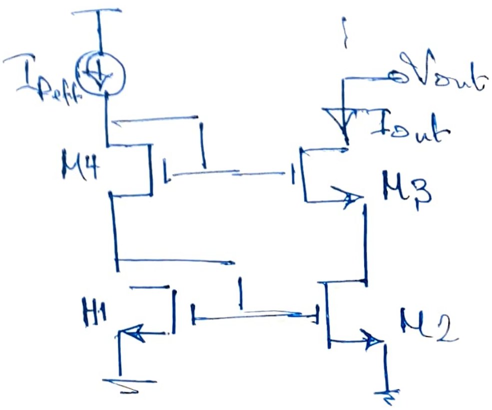
→ $V_{DS2} = V_{DS1} = V_{GS1}$

- But how to generate V_B?

  ↳ using a diode connection

- if M3 and M4 has same V_{GS}

  ∴ M1 and M2 will have same V_{DS}



\# note: mirroring is done by M1 and M2 and the role of M3 and M4 is to guarantee → $V_{DS1} = V_{DS2}$

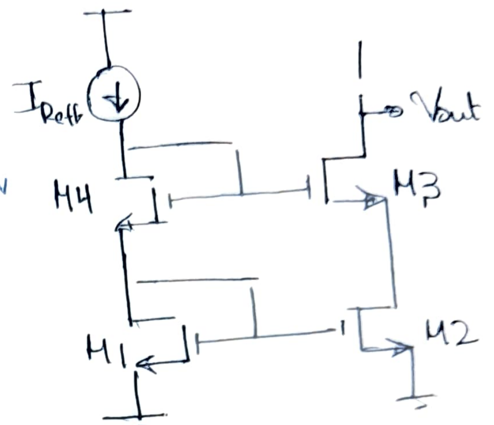
\# if V_{GS} and V_{DS} are equal.
Current will perfectly mirrored even if the transistors are NOT* in saturation

⑧ Compliance range.

- Compliance range is: V_{out} range where the Current Source behaves as a Current Source

- Quiz.

Assume $V_{TH1,2} = 0.4V$ and $V_{TH3,4} = 0.45V$ (body effect) and $V_{ov} = 0.1V$, Calculate the Current Source Compliance range.



∴ $V_{out\,min} = -V_{TH3} + V_{GS3} + V_{GS1}$

$= -V_{TH3} + V_{TH3} + V_{OV} + V_{TH1} + V_{OV}$

$= V_{TH1} + 2V_{OV}$

$= 0.4 + 0.2 = \underline{0.6}$

↓

Bad range ☹

- this Problem is due to Large $V_{DS2} = V_{TH1,2} + V_{OV}$
- the $V_{TH1,2}$ here has no need.
- Solution is --

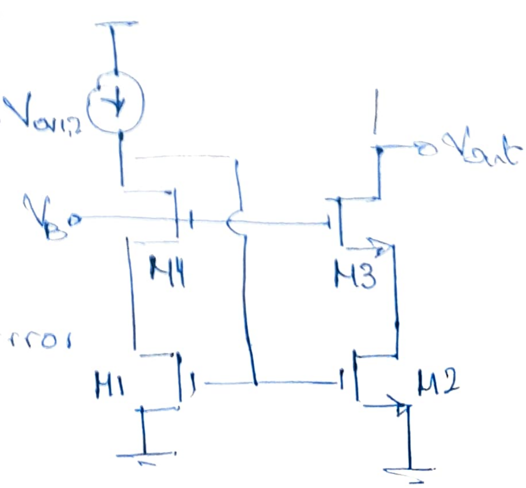
instead of making $V_{DS2} = V_{DS1}$

We make $V_{DS1} = V_{DS2.min}$

But How?

⑨ Wide Swing Current mirrors?

* $V_{TH3,4} + V_{OV3,4} + V_{OV1,2} < V_B < V_{TH3,4} + V_{TH1,2} + V_{OV1,2}$
- as Long as V_B is in the Valid range, M1→4 Will be In Sat
- A.k.a. low Voltage Current mirror

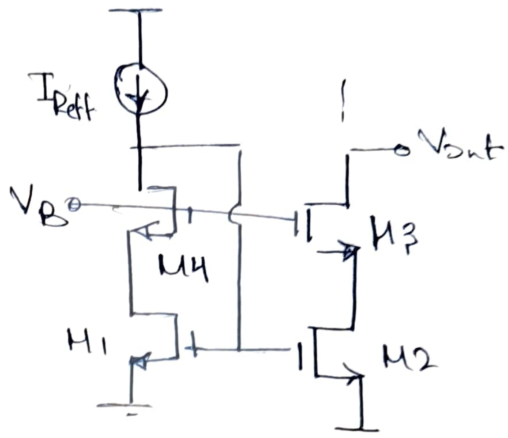


- Quiz.

Assume: $V_{TH1,2} = 0.4\,v$, $V_{TH3,4} = 0.45\,v$, $V_{ov} = 0.1\,v$

V_B is set 50mV above its minimum Value.

Calculate the Compliance range



∴ $V_{B\,min} = V_{GS3} + V_{DS2}$

$= V_{TH3,4} + V_{ov} + V_{ov}$

$= 0.65\,v$

∴ $V_B = 0.7$

∴ $V_{out} = -V_{TH3,4} + V_{GS3} + V_{DS2}$

$= -V_{TH3,4} + \cancel{V_{GS3}} + V_B - \cancel{V_{GS3}}$

$= 0.7 - 0.45 = 0.25$ #

How to Generate V_B

(10) The magic Battary.

- Assume M1-M4 have the same $\frac{W}{L}$: $V_B > V_{TH3,4} + 2V_{ov\,1-4}$

$V_{ov5} > 2V_{ov\,1-4} \longrightarrow L_5 > 4L_{1-4}$

- Never select $V_B = V_{B\,min}$ ($L_5 = 4L_{1-4}$)

↳ need to drive M1 and M2 a bit more into Sat

↳ account for body effect of M3 and M4

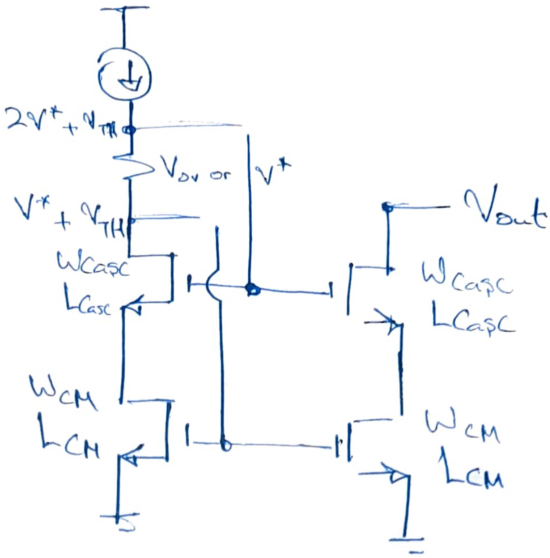
(11) Super Cascode (Regulated)

- Feedback keeps $V_{DS1} = V_{DS2}$ and boosts R_{out}
- $R_{out} \approx r_{o,super}(1 + g_{m,super} R_s) = r_{o3}(A_s g_{m3} r_{o2}) \sim A_s(g_m r_o^2)$
- Since both V_{GS} and V_{DS} are equal the mirror works even if M1 and M2 are not in Saturation.

12) Wide Swing (Improved)

* $V_R = V^*$

* $V_{out_{min}} = -V_{TH} + V_{TH} + 2V^*$
$= 2V^*$



* to design

- assume $L_{CM} = 3L_{min}$
- L_{casc} depends on
  R_{out} & output swing &
  isolation → if not required use L_{min}

- assume $V_{DS1,2} = V^* \longrightarrow V_{GS\,CM}$
- from $CMIR_L \longrightarrow V^*_{casc}$ ✓
- $R_{SS} = (g_m r_o)_{casc} * r_{oCM}$
- $r_{oCM} = \dfrac{V_A}{I_{CM}} \longrightarrow (g_m r_o)_{casc}$ ✓ $\longrightarrow L_{casc}$ ✓
- $I_{Ref} * R = V_{GS\,casc} + V^*_{CM} - V_{GS\,CM} \longrightarrow R$ ✓