Analog Integrated Systems Design

Lecture 09
Digital-to-Analog Conversion (1)

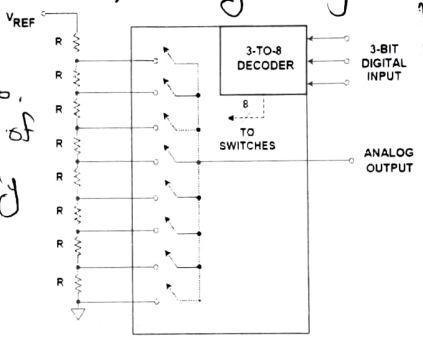
Dr. Hesham A. Omran

Integrated Circuits Laboratory (ICL)
Electronics and Communications Eng. Dept.
Faculty of Engineering
Ain Shams University

Resistor String (Ladder) DAC Unary.

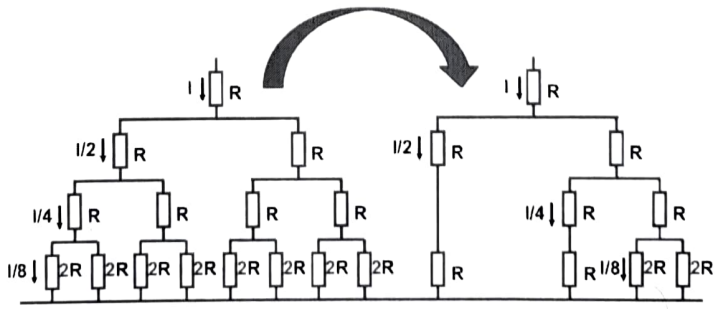
- Simply a voltage divider using 2^N identical unit resistors
- No. of switches = 2^N (**every** unit element needs a switch)
  - This is an example of a **unary** (thermometer) DAC → 1 unary as it depends on unit elements
- Monotonicity is guaranteed
- The decoder is a bit complex → 3 and the no. of Switch is Large So, routing of this no. of Switches is Very Very difficult. ☹

2 → no Way Voltage on Unit element (m+1) to be lower than Voltage on unite element (m) ☺



R-2R Ladder DAC Binary.

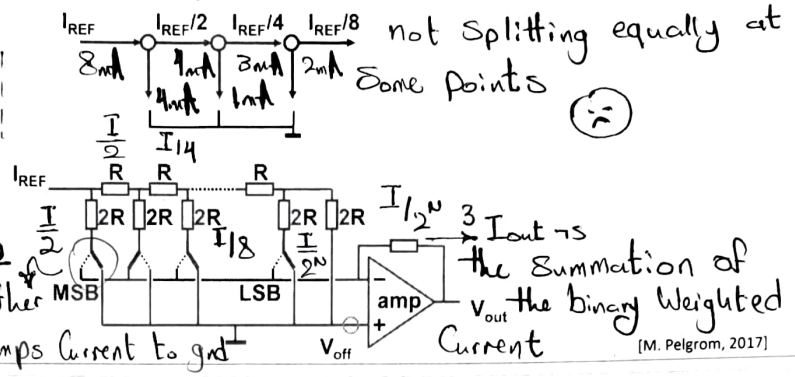
- Current splits equally at each level → Binary weighted currents
- At each node, looking downward the equivalent impedance is R
  - Each branch can be replaced by a resistance R with no effect on current splitting
- Current splits equally at each node between the "R" branch and the "2R" branch



R-2R Ladder DAC

- Current splits equally at each node
  - The binary weighted currents are combined by switches
- No. of switches ~ N → not complex at routing.
- No complex decoder is required
- Monotonicity is NOT guaranteed → Assume Iref = 8mA and Current is not splitting equally at some points

010 → 3mA
011 → 5mA
100 → 4mA
101 → 6mA
110 → 7mA

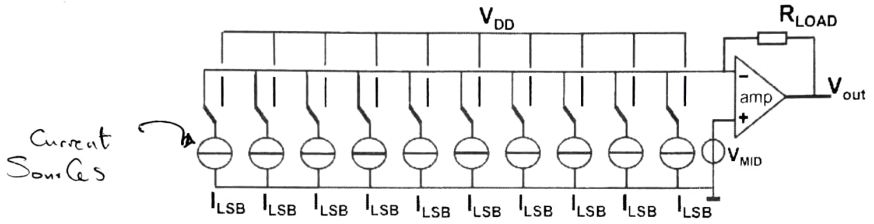


2 → A two-Way switch either dumps Current to gnd or to the output

3 → Iout is the summation of the binary Weighted Current

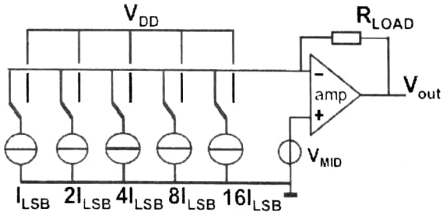
Current Domain DAC

- Unary implementation: 2^N switches, monotonic, complex decoder



- Binary implementation: ~ N switches, monotonicity not guaranteed

note that in binary of DACs for matching we use 2^N switches but the benifit is the routing of switches

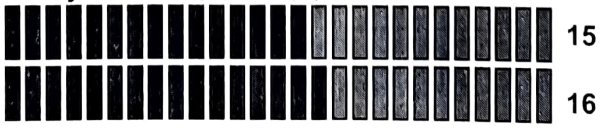


Unary (thermometer) Implementation

- No. of elements = 2^N
  - Unit elements can be resistors, capacitors, currents, etc
- No. of switches = 2^N (**every** unit element needs a switch)
- Monotonicity is guaranteed
- A.k.a. **thermometer code**

$$B_u = \sum_{i=0}^{i=2^N-1} b_i = b_0 + b_1 + b_2 \ldots + b_{2^N-1}$$

Unary series: 1,1,1,1,1,1,1...

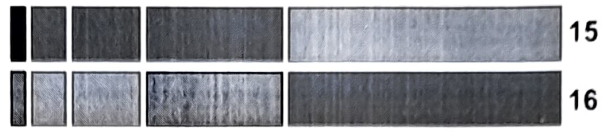


Binary Implementation

- No. of elements ~ N
  - Note that large elements are still composed of small matched unit elements
- No. of switches ~ N (**several** unit elements share the same switch)
- Monotonicity is NOT guaranteed
  - Worst case error occurs at mid-scale transition

$$B_b = \sum_{i=0}^{i=N-1} b_i 2^i = b_0 + b_1 2^1 + b_2 2^2 \ldots + b_{N-1} 2^{N-1}$$

Binary series: $2^0, 2^1, 2^2, 2^3, 2^4 \ldots 2^{N-1}$



Unary vs Binary

Unary, every time element is added even @ mid-scale

0	-
1	Δ_0
11	$\Delta_0+\Delta_1$
111	$\Delta_0+\Delta_1+\Delta_2$
1111	$\Delta_0+\Delta_1+\Delta_2+\Delta_3$
11111	$\Delta_0+\ldots+\Delta_4$
111111	$\Delta_0+\ldots+\Delta_5$
1111111	$\Delta_0+\ldots+\Delta_6$
11111111	$\Delta_0+\ldots+\Delta_6+\Delta_7$
111111111	$\Delta_0+\ldots+\Delta_8$
1111111111	$\Delta_0+\ldots+\Delta_9$
11111111111	$\Delta_0+\ldots+\Delta_{10}$
111111111111	$\Delta_0+\ldots+\Delta_{11}$
1111111111111	$\Delta_0+\ldots+\Delta_{12}$
11111111111111	$\Delta_0+\ldots+\Delta_{13}$
111111111111111	$\Delta_0+\ldots+\Delta_{14}$

3 errors are mainly due to mismatch

0000	-
0001	Δ_0
0010	Δ_1
0011	$\Delta_0+\Delta_1$
0100	Δ_2
0101	$\Delta_0+\Delta_2$
0110	$\Delta_1+\Delta_2$
0111	$\Delta_0+\Delta_1+\Delta_2$
1000	Δ_3
1001	$\Delta_0+\Delta_3$
1010	$\Delta_1+\Delta_3$
1011	$\Delta_0+\Delta_1+\Delta_3$
1100	$\Delta_2+\Delta_3$
1101	$\Delta_0+\Delta_2+\Delta_3$
1110	$\Delta_1+\Delta_2+\Delta_3$
1111	$\Delta_0+\Delta_1+\Delta_2+\Delta_3$

Binary → 2 mid-scale are use a fully new different glow.

Static DAC Errors

- Static DAC errors mainly due to component mismatch
- Mismatch can be systematic or random
- Systematic mismatch (can be reduced by good design and layout)
  - Edge effects in arrays
  - Process gradients
  - Contact resistance
  - Finite current source output resistance
- Random mismatch
  - Doping, lithography, etc.
  - Often Gaussian distribution (central limit theorem)

Random Mismatch

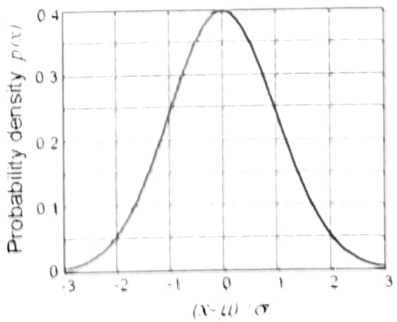
MOS transistors	$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}}$	$A_{VT} = 1\,\text{mV}\mu\text{m/nm}$ [74, 91]
MOS transistors	$\frac{\sigma_{\Delta\beta}}{\beta} = \frac{A_\beta}{\sqrt{WL}}$	$A_\beta = 1\text{–}2\,\%\,\mu\text{m}$ [74, 91]
Bipolar transistors (BiCMOS)	$\sigma_{\Delta Vbe} = \frac{A_{Vbe}}{\sqrt{WL}}$	$A_{Vbe} = 0.3\,\text{mV}\mu\text{m}$ [90]
Bipolar SiGe		$A_{Vbe} = 1\,\text{mV}\mu\text{m}$ [99]
Diffused/poly resistors	$\frac{\sigma_{\Delta R}}{R} = \frac{A_R}{\sqrt{WL}}$	$A_R = 0.5/5\,\%\,\mu\text{m}$
Plate, fringe capacitors	$\frac{\sigma_{\Delta C}}{C} = \frac{A_C}{\sqrt{C\text{ in fF}}}$	$A_C = 0.3 - 0.5\,\%\sqrt{\text{fF}}$ [78]
Small capacitors < 2 fF		$A_C = 0.7\,\%\sqrt{\text{fF}}$ [82]

Guidelines for Matched Components

1	Matching components are of the same material, have the same form, dimensions, and orientation
2	The potentials, temperatures, pressures, and other environmental factors are identical
3	Currents in components run in parallel, not anti-parallel, or perpendicular
4	Only use cross-coupled structures if there is a clear reason for that (e.g., temperature gradient). Identify the heat centers
5	Avoid overlay of wiring on matching components.
6	Use star-connected wiring for power, clock, and signal
7	Apply symmetrical (dummy) structures up to 20 μm away from sensitive structures
8	Keep supply and ground wiring together and take care that no other circuits dump their return current in a ground line
9	Check on voltage drops in power lines
10	Stay 200 μm away from the die edges to reduce stress from packaging
11	Tiling patterns are automatically inserted and can lead to unpredictable coupling, isolation thickness variations, and stress. Do not switch off the tiling pattern generation, but define a symmetrically placed tiling pattern yourself

Normal Distribution

$$p(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(x-\mu)^2}{2\sigma^2}}$$



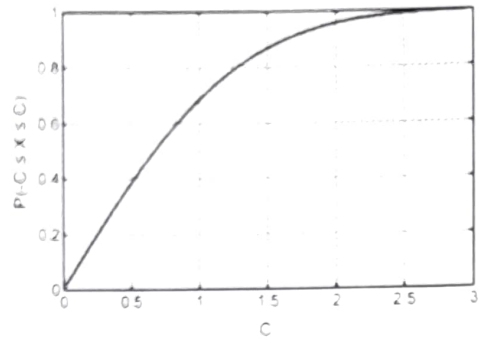
where:
μ is the expected value and
standard deviation: $\sigma = \sqrt{E(X^2) - \mu^2}$ RMS
$\sigma^2 \rightarrow$ variance

$E \rightarrow$ mean or Expectation

Yield

- Probability calculated numerically by erf (error function)
  - $C = X/\sigma$ is known as confidence interval

$$P(-C \le X \le +C) = \frac{1}{\sqrt{2\pi}} \int_{-C}^{+C} e^{-\frac{x^2}{2}} dx = \mathrm{erf}\left(\frac{C}{\sqrt{2}}\right)$$



Yield

- Probability calculated numerically by erf (error function)
  - $C = X/\sigma$ is known as confidence interval

X/σ	P(-X ≤ x ≤ X) [%]	X/σ	P(-X ≤ x ≤ X) [%]
0.2000	15.8519	2.2000	97.2193
0.4000	31.0843	2.4000	98.3605
0.6000	45.1484	2.6000	99.0678
0.8000	57.6289	2.8000	99.4890
1.0000	68.2689	3.0000	99.7300
1.2000	76.9861	3.2000	99.8626
1.4000	83.8487	3.4000	99.9326
1.6000	89.0401	3.6000	99.9682
1.8000	92.8139	3.8000	99.9855
2.0000	95.4500	4.0000	99.9937

Normal Distribution Example

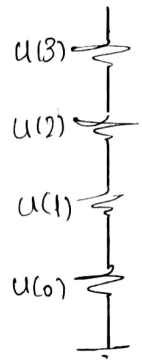
- Measurements show that the offset voltage of a batch of operational amplifiers follows a Gaussian distribution with σ = 2mV and $\mu = 0$

  μ → Average or Mean

- Find the fraction of opamps with |Vos| < 6mV
  - X/σ = 3 ➔ 99.73 % yield
- Find the fraction of opamps with |Vos| < 400uV:
  - X/σ = 0.2 ➔ 15.85 % yield

Unary DAC DNL

- Assume the value of the m-th unit element in a unary array is $u(m)$
  - Due to variations: $u(m) = u + du$
  - The standard deviation of mismatch is σ_{du}
  - Expectation (mean): $E[u(m)] = u$ (no systematic errors)
  - Standard deviation: $\sigma[u(m)] = \sigma_{du}$
  - Normalized std deviation: $\sigma_{\frac{du}{u}} = \frac{\sigma_{du}}{u}$



- For any transition in the unary N-bit DAC
  - $DNL = \frac{u(m)}{u} - 1$ (actual / ideal)
  - $E[DNL] = 0$
  - $\sigma[DNL] = \sigma_{DNL} = \sigma_{\frac{du}{u}}$

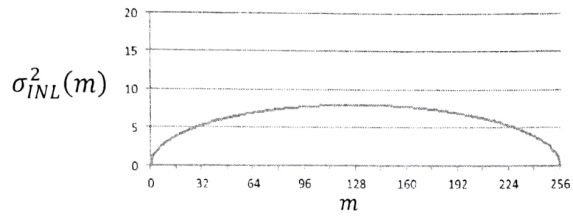
- The DNL is independent on no. of bits!

Unary DAC INL

- It can be shown that

$$\sigma^2_{INL}(m) = \frac{m(2^N - m)}{2^N}\sigma^2_{\frac{du}{u}}$$

(m: your location on the array)



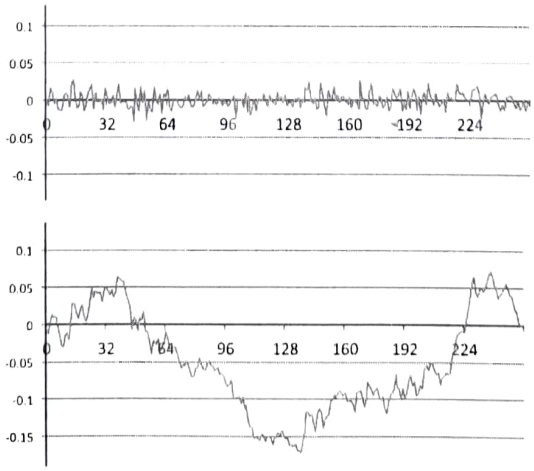
- Max σ_{INL} occurs at mid transition: $m = \frac{2^N}{2} = 2^{N-1}$

$$\sigma^2_{INL} = 2^{N-2}\sigma^2_{\frac{du}{u}} \quad \rightarrow \quad \sigma_{INL} = 2^{\frac{N}{2}-1}\sigma_{\frac{du}{u}}$$

- σ_{INL} depends on no. of bits

Unary DAC DNL/INL Example

- Note that max σ_{INL} occurs at mid-transition (statistical result)
  - But max INL for every DAC is not necessarily at mid-transition



Unary DAC DNL Example

- Assume a unary N-bit resistor string DAC
- If $\frac{\sigma_{dR}}{R}$ = 1%, what DNL spec goes into the DAC datasheet so that 99.73 % of all converters meet the spec?
  - 99.73 % yield ➔ X/σ = 3
  - DNL spec = 3 × σ_{DNL} = 3 × 1% = 3% = $\pm 0.03\ LSB$
  - Independent of N?!
- There is a flaw in this example. Why?

Unary DAC DNL Example

- For N-bit unary DAC we have 2^N elements
- For the DAC to pass the DNL spec, every element must pass
- P(all elements pass spec) = P(each element passes the spec)^2^N
- 0.9973 = P_{new}^2^N ➔ $P_{new} = (0.9973)^{\frac{1}{2^N}}$
  - N = 8-bit: $P_{new} = 0.99995708$
  - N = 16-bit: $P_{new} = 0.99999929$
- calculate modified confidence intervals using MATLAB
  - N = 8-bit: C = $\sqrt{2}$*erfinv(P_{new}) = 4 ➔ DNL spec = $\pm 0.04\ LSB$
  - N = 16-bit: C = $\sqrt{2}$*erfinv(P_{new}) = 5 ➔ DNL spec = $\pm 0.05\ LSB$
- For complex DAC architectures, running Monte Carlo simulations in MATLAB may be easier than deriving yield expression

Binary DAC DNL

- Worst case transition occurs at mid-scale
  - 100…0 → 011…1

$$DNL = \frac{(u_{2^{N-1}} + u_{2^{N-1}+1} + \cdots + u_{2^N-1}) - (u_1 + \cdots + u_{2^{N-1}-1})}{u} - 1$$

- All DAC elements are involved in the transition

$$\sigma^2[DNL] = \sigma^2_{DNL} = (2^N - 1)\,\sigma^2_{\frac{du}{u}}$$

$$\sigma_{DNL} \approx 2^{\frac{N}{2}}\,\sigma_{\frac{du}{u}}$$

Binary DAC INL

- Max σ_{INL} same as in unary (at mid-transition)

$$\sigma_{INL}^2 = 2^{N-2}\sigma_{\frac{du}{u}}^2$$

$$\sigma_{INL} = 2^{\frac{N}{2}-1}\sigma_{\frac{du}{u}}$$

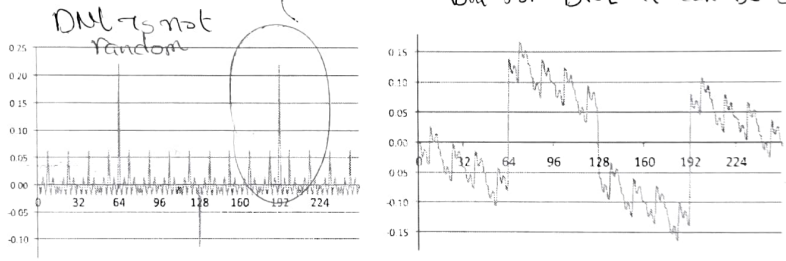
Binary DAC DNL/INL Example

- The DNL plot is symmetric
- Worst case DNL occurs at binary transitions

$$2^{N-1}, 2^{N-1} \pm 2^{N-2}, 2^{N-1} \pm 2^{N-2} \pm 2^{N-3}, \ldots$$

- The INL shows a repetitive pattern

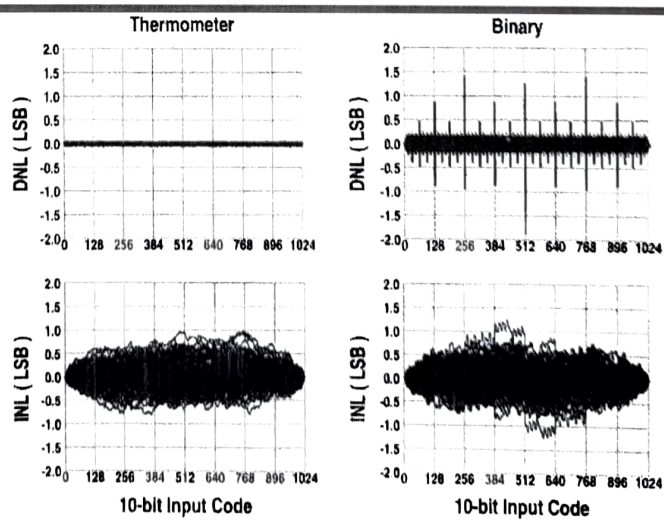
Note that the worst case is a mid-scale but for DNL it can be something else



Unary vs Binary

Ref: C. Lin and K. Bult, "A 10-b, 500-MSample/s CMOS DAC in 0.6 mm2," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1948 - 1958, December 1998.

Note: σ_ε=2%



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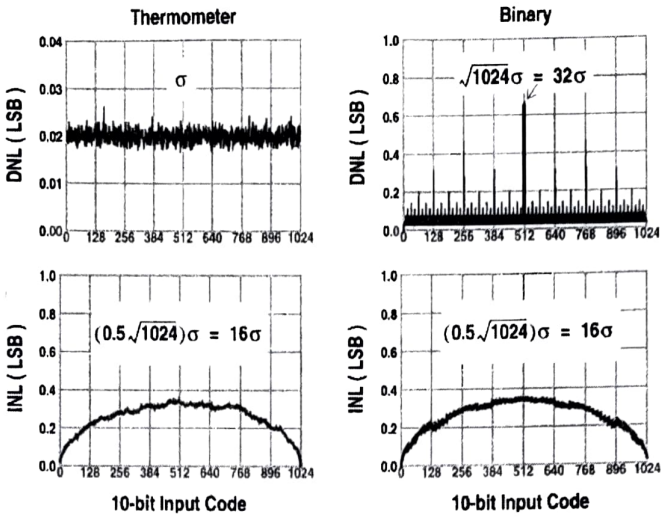
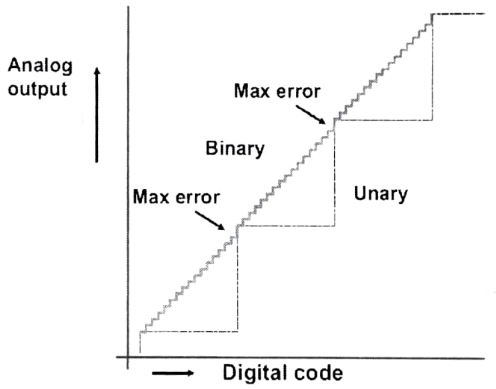
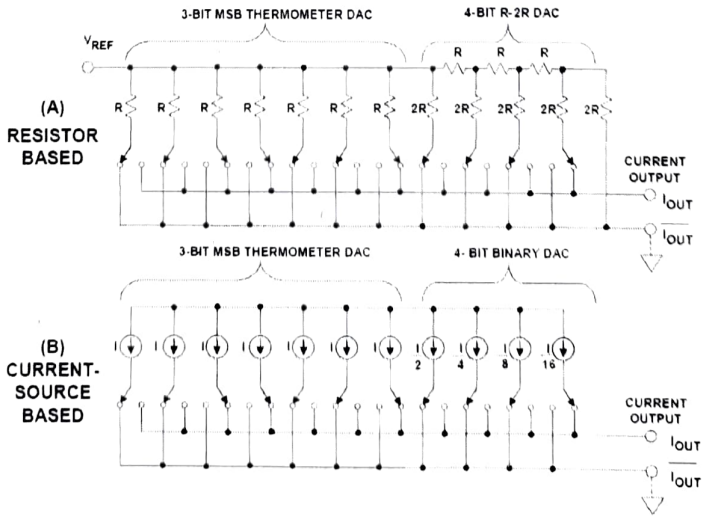


Segmentation

- Use unary for MSBs (N_{unary}) and binary for LSBs (N_{binary})
- The unary steps must have the accuracy of an LSB
- Binary errors will appear "periodically" over all unary sections



Segmented DAC



Segmented DAC DNL

- Use unary for MSBs (N_{unary}) and binary for LSBs (N_{binary})
- Worst case occurs when LSB DAC turns off (N_{binary}) and one more MSB DAC element turns on
  - Same as binary weighted DAC with $(N_{binary} + 1)$ bits

$$\sigma^2[DNL] = \sigma_{DNL}^2 = (2^{N_{binary}+1} - 1)\,\sigma_{\frac{du}{u}}^2$$

$$\sigma_{DNL} \approx 2^{\frac{N_{binary}+1}{2}}\,\sigma_{\frac{du}{u}}$$

Segmented DAC INL

- Max σ_{INL} same as in unary (at mid-transition)

$$\sigma_{INL}^2 = 2^{N-2}\sigma_{\frac{du}{u}}^2$$

$$\sigma_{INL} = 2^{\frac{N}{2}-1}\sigma_{\frac{du}{u}}$$

Same as Unary and Binary

DNL/INL Summary

	σ_{INL}	σ_{DNL}	No. of switches
Unary (thermometer)		$\sigma_{\frac{du}{u}}$	$2^N - 1$
Segmented	$2^{\frac{N}{2}-1}\sigma_{\frac{du}{u}}$	$2^{\frac{N_{binary}+1}{2}}\sigma_{\frac{du}{u}}$	$2^{N_{unary}} - 1 + N_{binary}$
Binary		$2^{\frac{N}{2}}\sigma_{\frac{du}{u}}$	N

Example: N = 12, $\sigma_{du/u} = 1\%$

	σ_{INL} (LSB)	σ_{DNL} (LSB)	No. of switches
Unary (thermometer)	0.32	0.01	4095
Segmented (6u+6b)		0.11	63 + 6
Segmented (5u+7b)		0.16	31 + 7
Binary		0.64	12

DAC Architectures

	Unary	Binary
Voltage	Resistor string *Flash ADC*	R-2R *Low-performance DAC*
Current	Current matrix	Current splitting
	High bandwidth DAC	
Charge/capacitor	Capacitor bank *Low power DAC*	Capacitor bank
Time	PWM, ΣΔ mod *Low bandwidth DAC*	Limited by distortion

In italic the main application area is indicated